Anodic Oxide Rear Contact Schemes for Silicon Solar Cells

By

Jie Cui

School of Photovoltaic and Renewable Energy Engineering

University of New South Wales

Sydney, Australia

A thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

August 2014

PLEASE TYPE

THE UNIVERSITY OF NEW SOUTH WALES
Thesis/Dissertation Sheet

Surname or Family name: Cui

First name: Jie Other name/s:

Abbreviation for degree as given in the University calendar: Ph. D

School: School of Photovoltaic and Renewable Energy Engineering Faculty: Engineering

Title: Anodic Oxide Rear Contact Schemes for Silicon Solar Cells

Abstract 350 words maximum: (PLEASE TYPE)

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An initial study explored the effects of patterning by laser and chemical etching on the properties of local back surface fields (LBSF) regions formed by aluminium alloying. Chemical etching resulted in 2 - 3 µm thicker LBSF regions and reduced Kirkendall void formation. This understanding inspired the development of a new inkjet etching patterning technique for patterning anodic aluminium oxide (AAO), a proposed new low cost dielectric for silicon solar cells. Point openings diameters of 20 – 30 µm and LBSF regions that were up to 7 µm deep were realised in 600 nm AAO layer. However, properties associated with the clip anodisation process used to form the AAO layer limited the reliability of this patterning process. A novel light-induced anodisation (LIA) technique was developed to address the limitations of clip anodisation. Anodic silicon dioxide (SiO_2) layers formed using LIA achieved comparable effective minority carrier lifetimes to thermal SiO_2 with a low density of interface states (D_{it}) of 6×10^{11} eV^{-1} cm^{-2} and leakage currents that were six orders of magnitude lower than thermal SiO_2. The D_{it} of AAO layers formed by LIA of aluminium were measured to be as low as 1×10^{10} cm^{-2} eV^{-1}, a value which is lower than any reported aluminium oxide layer deposited by other deposition techniques. Cells fabricated with SiO_2/AAO rear passivation layers achieved open circuit voltages of 660 mV, a value that is comparable to that achieved by cells passivated with the industrial standard of aluminium oxide/silicon nitride thus highlighting the potential of this new low-cost AAO passivation layer and the novel LIA process to reduce the manufacturing cost of rear-passivated silicon solar cells.

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“Think independently and conduct conforms to thinking.”

Liang Shu-Ming (1893-1988)
A thinker, philosopher and neo-confucianist

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Abstract

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Acknowledgement

First and foremost, I would like to thank my supervisor, Dr. Alison Lennon, for her advice and encouragement, for always making herself available for discussion and especially for her positive and enthusiastic approach to research. Her hardworking attitude and her endless excitement for solar cells provide me immeasurable encouragements. Thank you for providing me the interesting topic and guiding me through the arduous but exciting journey of research. I'm also grateful to my co-supervisor Prof. Stuart Wenham. Thank you for always being open and supportive whenever I have inquires, for generously providing all kinds of resources to my research and for making those fruitful discussions. Your immense knowledge in solar cells and innovative ideas made my PhD research an enjoyable experience.

There are so many colleagues at SPREE, UNSW who have generously provided help and made my research an ongoing delight. I would like to mention a few in particular. Xi Wang is an incredibly talented workmate, who inspired and assisted me in the development of the light-induced anodisation technique, which is the backbone of this thesis. Dr. Ziv Hameiri taught me the fundamental theories of effective minority carrier lifetime measurement and helped me with a lot of contactless *C-V* measurements, which made the arguments in the anodic oxide characterisation much more profound. Alex To spent tremendous efforts in exploring the inkjet patterning technique at the early stage. His undergraduate thesis formed the base of the work in Chapter 4. Additionally, I'm grateful that I met Jack Colwell on the second day when I first came to Australia. He chose to work with me for 'taste of research' and again for his 4^{th} year thesis. All of his talented work was turned into good publications and some of them contributed a lot to the writing of this thesis. Many thanks to all of you.

I would also like to thank Dr. Malcolm Abbott for his valuable discussions and his vast knowledge in cell characterisation and analysis. A special thank you to Ned Western for many ideas he shared with me and for his help in the time consuming DLTS measurement. A thank you to Mattias Juhl, the expert in QSS-PL, for his patient explanation of the theories (quite a few times!) and method of data analysis. Thanks to Dr. Ly Mai and Dr. Adeline Sugianto for answering me many questions in solar cell fabrication. Thank you to Nino Borojevic for helping me with numerous PECVD

depositions. Thanks also to Yu Yao for sharing her rich experience in metal plating and providing me advice in doing a proper research. I really enjoy the days that you are around.

The support I received was also from colleagues outside UNSW and I would like to thank them all here. Prof. Robert Opila provided me enormous help in characterising and analysing the anodic SiO_2. Dr. Nick Grant at ANU organised the lab for my experiments there and helped with the *C-V* measurements. My good friend Licheng Liu from SERIS contributed a lot in our formal and informal discussions and joined me with the fabrication of AJE-patterned PERC cells. Johan Beckers and Jurgen Bertens organised the trial of anodisation with their industrial tool. Additionally, special thank you to Renate Egan, Rhett Evens and Scott Partlin at Suntech R&D Australia for making the linkage grant meetings and reviewing my papers at the early stage of my PhD.

Then, of course, there is Alison's patterning/plating/anodisation group. Thanks to all the group members for making discussions and sharing ideas like a family. I miss so much our regular group activities at Alison's and Ouyang's places.

Thank everybody in the LDOT team, Mark Silver, Kian Chin, Bernhard Vogl, Alan Yee, Nick Shaw, Lawrence Soria and others for keeping the lab running smoothly. Thanks also to Jill Lewis and Kimberly Edmund for their help from the administration side.

Thank the staff at Electron Microscope Unit. My project is heavily relied on EMU's equipment and your help.

Beyond the relationship as colleagues, I would like to thank all my friends at work. Particularly, Bernhard Mitchell, Chaowei Xue, Ned Western, Oliver Kunz, Zi Ouyang, Craig Johnson, Brett Hallam, Alison Wenham, Catherine Chan and Doris Lu (of course, there are much more), are thanked for their accompany in our wonderful cycling trips, bushwalks and snow trips, which recharged me in between the hard works. Moreover, thank the active members in our 'lunch group' on WeChat, your ideas, chat and jokes made the lunch an absolute highlight of the day, every day!

I’m also grateful to the co-founders of intoPV.com, Yang Li, Zhongtian Li, Zhong Lu and Yu Yao. I always learn a lot from discussions in our lively weekly meetings in the Friday afternoons. Hope we can make this platform bigger and more successful!

I’d also like to specially thank my proofreaders Oliver, Ouyang, Xi, Jack and Licheng for making time to critically read through all or part of my thesis chapters.

A huge and deeply thank you to my partner Yang Xie, who has shared a lot of time with me as the closest person during the writing of this thesis. Because of you, Sydney feels like a home. Your endless love and support has given me a powerful perspective to tackle any upfront challenges.

And finally, deeply heartfelt thanks to my parents, who have always been there for me, no matter if I’m in Urumqi, Hangzhou or Sydney. Mum and Dad, I cannot express enough gratitude for the love and support that you have generously given to me for the past of my life. I hope I can make you proud in the end. I love you all!

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Chapter 1 Introduction

November 18, 2006 is a meaningful day for Alaxi, who is a farmer living in Chagan Mo'ergen village in the rural area of Xinjiang, north western China, because it is on this day that he has access to the electricity provided by the solar photovoltaic (PV) power plant built next to his village. The nights under gas lamp and candles become history, instead his house is now lit by electricity and he is planning to buy a TV to learn more about the outside world. Alaxi isn't the only lucky one, with the five local small scale solar PV power plants, 200 families in neighbouring villages move into a modern life. The local school, which used to close very early during winter due to lack of electricity, now operates the same as their counterparts in the city, moreover TV, DVDs and speakers are used to assist teachers in the class.

Alaxi's story is a snapshot of how solar PV power changes people's lives. In fact, the *energy poverty* that Alaxi experienced is becoming one of the major challenges of the human race. Approximately 28% of people in developing countries currently lack access to electricity, compared to a staggering 70% or more in the world's least-developed countries and in sub-Saharan Africa [1]. In most cases, this is due to the high cost of distributing electricity to rural areas via a conventional power grid. The International Energy Agency (IEA) estimates that 1.4 billion people will still lack access to electricity in 2030 unless new approaches and policies are adopted to adapt electrification programmes [1]. As a result the standard of living of these communities is strongly limited, not only in terms of having limited access to a modern lifestyle with electrical lighting, cooking, heating and cooling, but due to the lack of communication with the 'outside' world via modern technologies, such as telephone, TV and Internet. Lack of electricity also hinders the quality of education and medical service that people can receive.

Additionally, energy poverty is not the only big issue that human beings need to address. As shown in Figure 1-1, taking only those government policies and measures that had been enacted or adopted by mid-2012 into consideration, the world primary energy demand will exceed 18,000 million tonnes of oil equivalent (Mtoe) by 2035, with over 80% contribution from fossil fuels [2]. Hence, without major policy changes,

human beings will face three other major challenges: energy security, energy access and climate change.

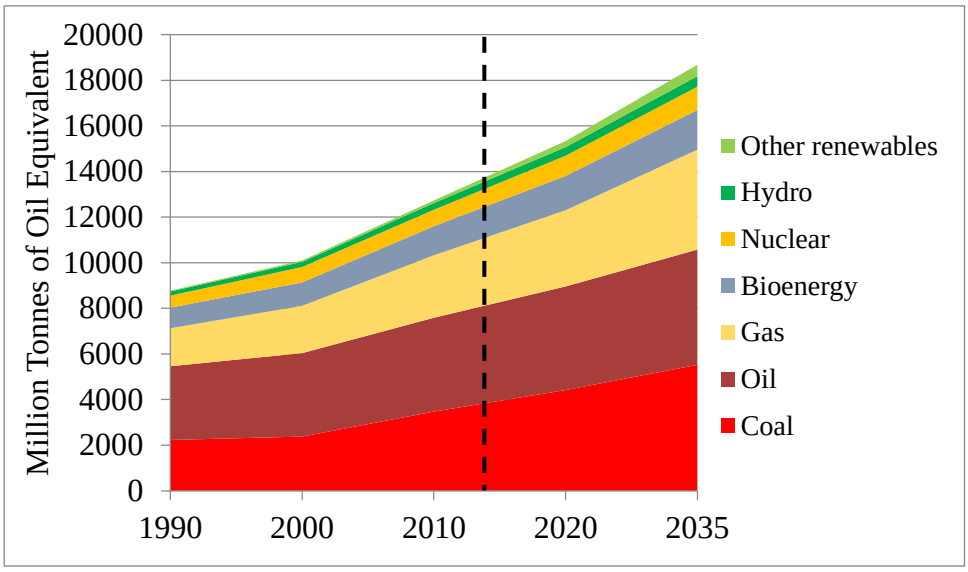

Figure 1-1 World primary energy demand in Mtoe under current policies scenario. The vertical dashed line indicates the current status in 2014 (data reproduced from [2]).

Taking climate change as an example, the decade 2001-2010 was the warmest decade since instrumental global average surface temperatures first became available in 1850. Shown in Figure 1-2, the mean global temperature of this decade increased by 0.88 °C since the first decade of the past century (1901-1910), with the warmest year ever being 2010 [3]. Increased global surface temperature impacts severely on both the ecosystem and human communities. From 1980 to 2010, the number of natural disasters, predominantly meteorological and hydrological disasters, was doubled. There were 370,000 lives lost owing to extreme climate conditions, including heat, cold, drought, storms and floods, representing an overall increase of 20% compared to the previous decade, 1991-2000 [3]. Therefore global warming must be addressed, and providing clean, efficient, affordable and reliable energy services to all human communities is indispensable for future global prosperity.

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Figure 1-2 Decadal global data of combined surface-air temperature over land and sea-surface temperature (°C). The horizontal grey line indicates the long-term average value (14.0°C) computed based on the 1961–1990 base periods [3].

Renewable energy is energy that comes from resources which are naturally replenished on a human timescale. It is widely accepted as a clean and sustainable alternative to fossil fuels and nuclear energy. It includes resources, such as wind power, solar PV, concentrating solar thermal power, solar hot water/heating, biomass power and heat, biofuels, geothermal power and heat, hydropower and ocean energy. Figure 1-3 illustrates a comparison of global energy consumption share in 2009 and 2011. In 2011, 19% of the global energy consumption came from renewable resources, which was increased from 16% in 2009. Traditional biomass, which is used primarily for cooking and heating in rural areas of developing countries, accounts for approximately 9.3% of the total share in 2011, reduced by 0.7% absolute from 2009 [4, 5]. The application of 'modern' renewable resources, such as wind, solar and biomass, however is growing fast.

Although renewable energy provides an alternative energy solution to fossil and nuclear fuels, most sources place restrictions on local natural resources. For example, hydropower requires access to rivers, ocean energy can only be harnessed at the coast, and wind and geothermal resources are only abundant in specific regions. Solar energy is an exception, with its wide accessibility and reliability. The world's overall solar energy potential absorbed by Earth's atmosphere, oceans and land masses is around 5.6 GJ m^{-2} every year [6]. The energy from the sun that falls on the earth in one hour is more than that used by the world's population in one year [7]. In the past decade, both residential, commercial and utility scale applications of solar PV as well as solar thermal energy experienced a dramatic growth, with the average growth rate of solar PV and concentrating solar thermal capacity being 60% and 43%, respectively from 2007-2012, significantly higher than growth of any other renewable resources (refer to Figure 1-4).

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Figure 1-3 Comparison of renewable energy share of global energy consumption in (a) 2009 [4] and (b) 2011 [5].

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Figure 1-4 Average annual growth rates of renewable energy capacity and biofuels production, 2007-2012 [5].

Generation of electricity by directly harnessing the sunlight makes solar PV systems a reliable, clean and sustainable renewable energy approach for human beings. Properly designed and manufactured solar PV systems can be easily transported and deployed to where electricity is required. They can be deployed at any scale (from mW to GW) and PV panels can operate in the field with an industrial standard guarantee of 25 years. Although energy storage is required due to the mismatch between solar electricity generation and the demand, stand-alone off-grid system solutions are increasingly acknowledged to be the cheapest and most sustainable options for rural areas in much of the developing world [4].

1.1 Motivation

In the past four decades (1976-2014), the average selling price of solar PV modules decreased with a learning rate of about 21% for every doubling of cumulative module shipments [8]. The price reduction is primarily due to cost reductions in the manufacturing processes [9]. Despite the expansion of solar PV generation by 50% per year worldwide over the last decade due to significantly reduced cost and increased demand, this energy source only accounted for 0.4% of global electricity generation in 2012 and is projected to share 2.6% of the total electricity generation in 2035 by IEA [10]. The major barrier to solar PV is still its relatively high electricity generation cost, which is analysed by two parameters: grid-parity and levelised cost of electricity (LCOE). Grid-parity, defined as the lifetime generation cost of the electricity from solar PV being comparable with the electricity prices for conventional sources on the grid, has long been considered as the turning point for solar dominance in the share of energy sources [11]. Although it has been estimated that grid-parity events will be on going around the world, with about 75-90% of total global electricity market reaching grid-parity by 2020 [12], it is the LCOE that is of interest to the customer and that value is more often used when comparing electricity generation technologies or considering grid-parity for emerging technologies such as solar PV [13]. Currently the LCOE of 1 kWh of electricity from a solar PV system in the United States is $US 0.16 for commercial use and $US 0.29 for residential use, which is still much higher than the comparative LCOE from fossil fuels of $US 0.04 and $US 0.08, respectively [14].

Therefore further lowering of the LCOE must be realised to make solar PV a competitive alternative to fossil fuels. There are two approaches to realise further cost

reduction: (i) directly reduce the cost of manufacturing; or (ii) increase the efficiency of the devices fabricated while maintaining the manufacturing cost. Since high efficiency solar cells are typically associated with higher quality materials and additional processes, the cost is almost always increased. This thesis is motivated by the first approach. As silicon solar cell manufacturing continues to move towards rear locally-contacted cell designs [8, 15] in an aim to increase cell efficiency, new surface passivation and local contact formation approaches are required. The industrial passivated emitter and rear cell (PERC) has noticeable limitations, such as the cost of the chemical vapour deposited aluminium oxide (AlO_x) rear passivation layer and silver paste, as well as performance degradation and yield losses due to void formation in the local contact regions. Therefore, development of new rear local contact schemes featuring lower-cost dielectrics, such as anodic oxides, that can be formed at low temperatures with high throughput and can be effectively and reliably patterned, are of significant importance.

1.2 Thesis Objectives

This thesis examines possible cost-effective improvements in rear local contact formation for silicon solar cells that could be used in manufacturing, with special focus on the formation of anodic oxide dielectric layers and patterning of these layers. It first investigates currently-available dielectric patterning techniques and assesses their impact on the formation of aluminium-alloyed local contacts. Based on the identified limitations of those patterning processes, a new dielectric patterning process which exploits the porous morphology of anodic aluminium oxide (AAO) and uses inkjet printing is presented. Finally, a new light-induced anodisation (LIA) technique which allows fast and uniform anodisation of *p*-type silicon, or metal layers deposited on *p*-type silicon surfaces over large areas is presented. The study is limited to the characterisation of test structures and the fabrication of prototype solar cell devices that could demonstrate the future potential of the developed anodisation and dielectric patterning processes.

1.3 Thesis Outline

This thesis consists of two major parts. The first part (chapter 3 and 4) discusses the dielectric patterning and rear local contact formation, while the second part (chapter

5 and 6) describes the development of the LIA technique and its application to the formation of anodic oxides for silicon solar cells.

Chapter 2 reviews the design of rear local contact solar cells, such as laboratory high efficiency PERC and passivated emitter and rear locally diffused (PERL) cells, in order to identify the high efficiency attributes of these cell designs. Then several industrial PERC/PERL cell designs are reviewed to evaluate the strengths and limitations of such cells. It is found that three processes: (i) dielectric deposition; (ii) patterning; and (iii) local contact formation, are critical in improving the cell performance. Consequently, each of these processes is reviewed in detail. Special attention is paid to anodic oxides as the passivation dielectric and inkjet/aerosol jet chemical patterning techniques, which can effectively pattern anodic oxides without compromising the surface passivation.

Chapter 3 investigates the dielectric patterning and rear local contact formation. This chapter begins with a study of local contact formation through laser scribing, boron laser doping and aerosol jet etching (AJE) of patterned silicon dioxide (SiO_2)/ silicon nitride (SiN_x) dielectric stacks. The physical properties of metal contact regions, such as spreading limit of silicon in aluminium, local back surface field (LBSF) thickness, line widening and void formation are investigated and compared. Following these investigations, the fabrication of AlO_x/SiN_x passivated PERC cells with rear contacts formed through AJE patterning of the rear dielectric is described and a detailed electrical characterisation and loss analysis are presented.

Chapter 4 describes the development of an inkjet patterning technique which effectively patterns AAO. Successful patterning of point openings are demonstrated on polished, planar and textured substrates. Then, the formation of LBSF regions through inkjet patterned AAO is studied. The chapter concludes with a demonstration of the limitations of the existing anodisation technique identifying the difficulties associated with performing the process using an industrial in-line tool.

In Chapter 5, the development of a novel anodisation technique, LIA, which can be used to anodise *p*-type silicon surfaces, is described. The LIA process addresses the limitations identified in the conclusion of Chapter 4. The low temperature anodic formation of SiO_2 is of significant importance to commercial-grade silicon wafers (e.g., multi-crystalline silicon) which are ideally not subjected to high temperature thermal oxidation processes. The growth dynamics of anodic SiO_2 as well as the optical and

electrical properties are investigated. Future applications of anodic SiO_2 in silicon solar cells are discussed with applications in contact passivation, epaxially-grown silicon passivation and barriers for metal-plating and potential-induced degradation (PID) being identified.

Based on the successful development of LIA of silicon, Chapter 6 investigates the LIA of aluminium. First, it briefly explains the mechanism of AAO formation by LIA and then explores improvements in surface passivation achieved by removing a laser pattering step and optimising the post anodisation anneals. Second, the silicon/SiO_2/AAO interface quality and the AAO composition are investigated. Finally, the fabrication of novel AAO-passivated PERC cells is described. The AAO acts as an effective surface passivation dielectric enabling cell open circuit voltages (V_{oc}) of 660 mV to be achieved. A loss analysis with identified limitations is presented and possible solutions are identified that could improve cell performance.

The thesis concludes with a summary of important results, original contributions and suggestions for possible future work in Chapter 7.

Chapter 2 Literature Review

The key driver for silicon PV technology development is now clearly cost. Recent significant reductions in manufacturing cost have been largely attributed to 'economies-of-scale' benefits, however maintaining the current PV downward cost trajectory will require innovations that either directly reduce the cost of processing or increase the efficiency of devices manufactured. Passivation of the surfaces of silicon wafers results in higher efficiencies by increasing V_{oc}. In this Chapter, the design of rear local contact solar cells is reviewed with special focus on high efficiency PERC and PERL cells, which are of special interest of this thesis. Then it explores the commonly-used dielectrics in rear local contact cells, such as thermally-grown SiO_2, SiO_2/SiN_x, AlO_x/SiN_x. Furthermore, anodic oxides that are newly introduced for solar application are reviewed, including anodic SiO_2 and AAO. Focus is then moved to the patterning techniques of the dielectrics and the mechanism of the local contact formation, with special tension paid to two methods of forming local contact through AAO.

2.1 Rear Local Contact Solar Cells

Although screen-printed solar cells have dominated the PV market over the last 30 years [16], the limitations of this cell design become more pronounced with the PV industry moving towards higher efficiency and thinner substrates. To further improve the cell voltage, the full area aluminium back surface field (BSF) on the rear surface of screen-printed solar cell must be replaced by a dielectric passivated surface with metal contacts only formed locally through patterned features. In the past three decades, laboratory-based research has resulted in the development of cell structures with rear local contacts, such as PERC, PERL, emitter wrap through (EWT), metal wrap through (MWT) and interdigitated back contact (IBC) solar cells. The PERC and PERL cells were developed based on the structure of screen-printed cells with two extra steps: rear passivation dielectric deposition and patterning. Both of these two cell structures demonstrated cell efficiencies over 21% [17, 18]. In recent years, enormous effort has been directed into simplifying the PERC structure with industrially-viable processes with cell efficiencies exceeding 20% on large area, commercial-grade wafers being demonstrated by a number of research institutes and companies [19-25]. It is estimated

that PERC cells will comprise 50% of the crystalline silicon PV market share by 2024 [8] because of its compatibility to the current screen-printed cell process. This section reviews the PERC and PERL solar cell design. It evaluates the advantages and limitations of each cell structure and discusses the aspects that can be adopted in the design of commercially-produced solar cells.

2.1.1 The PERC Solar Cell

The PERC solar cell was first reported by Blakers *et al.* in 1989 [17]. It is a laboratory design cell structure which includes many high-efficiency solar cell attributes. Figure 2-1 presents a schematic of the PERC structure.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-1 Schematic diagram of PERC solar cell [17].

The well-passivated surfaces and high bulk lifetime contributed to the high cell V_{oc}. The cells were fabricated using high-quality float zone (FZ) wafers which had a bulk lifetime in excess of 300 μs in the finished cell therefore enabling high V_{oc} values. The cell V_{oc} was further improved by growing a passivation oxide layer on the rear surface, which was structurally different from the previously-reported passivated-emitter solar cell (PESC) [26]. The oxide layer grown using chlorine-based processing [27, 28] that not only provided superior surface passivation, but also acted as an effective displaced rear reflector with the rear aluminium which increased the internal reflection of 1.1 eV photons to above 97%. The rear metal contacts were formed through a photolithographically patterned array of holes with diameter of 200 μm in the passivation oxide layer. The use of a heavily-doped substrate of 0.2 Ω cm reduced the rear contact resistance (R_c) and allowed the contact spacing to be larger than the cell thickness.

The high cell J_{sc} was attributed to the advanced light trapping designs which included a double-layer antireflection coating (ARC) and inverted-pyramids. The latter not only reduced the reflection on the front surface, but also enhanced the light trapping in combination with the displaced rear reflector [29].

Cell fill factors (*FF*) were determined by the series resistance (R_s) losses, either represented as emitter resistance or bulk resistance, due to the lateral current flow in both of these regions. Since the cell emitter is lightly-doped apart from the contact areas

underneath the front metal contacts, the R_s loss in the emitter was more pronounced than that in the bulk.

Table 2-1 compares the electrical characterisation of PESC and PERC solar cells under standard test condition (STC), which is AM 1.5 spectrum, 100 mW cm^{-2}, 25 °C. The dramatic increase in V_{oc} and J_{sc} are due to the rear passivation oxide layer and the inverted-pyramid light trapping scheme, respectively, which results in 3.7% absolute higher efficiency for the PERC cell. However, the fabrication process for the PERC cell involves three photolithographic processes and three high temperature oxidation processes, the latter being required for inverted-pyramids etching, selective emitter diffusion and surface passivation. These additional processes results in a complex cell fabrication sequence, a lengthy processing time and high processing costs, all of which make the cell design unsuitable for mass production. However, the superior performance of the PERC design indicates the design criteria for commercial high efficiency solar cells, which are selective emitter, effective light trapping and high quality rear surface passivation.

Table 2-1 Electrical characterisation of PESC and PERC solar cells (AM 1.5 spectrum, 100 mW cm^{-2}, 25 °C. The PESC has a full area aluminium-silicon rear contact.

	Resistivity (Ω cm)	Area (cm^2)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF* (%)	η (%)	Ref
PESC	0.2	4	653	36	81.1	19.1	[26]
PERC	0.2	4	696	40.3	81.4	22.8	[17]

2.1.2 The PERL Solar Cell

Built on the success of PERC solar cell, the 24% efficient PERL solar cell was first reported in 1990 [30] and the efficiency was improved to 25% in the late 1990s [31, 32]. The PERL solar cell held the world record for the most efficient single-junction silicon solar cell since 1990 until 2014 [33]. Figure 2-2 shows a schematic diagram of the PERL solar cell structure.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-2 Schematic diagram of PERL solar cell [34].

The major difference between the PERL and PERC cell design is the local boron diffusion in the rear contact area [30]. The *p*+ region reduces the effective

recombination rate at the rear contacts by suppressing the concentration of minority carriers at the metal interface. In doing so, two constrains of the PERC cell were removed. First, the sheet resistance of boron-diffused contact area was 20 Ω/□, therefore wafers of higher resistivity could be used without rectifying current flow at the rear contact. Second, the point contact spacing was able to be reduced from 2 mm of PERC cell to 250 μm in the PERL cell [34], which decreased the cell lateral series resistance, enabling a much higher *FF*.

Improvement in the cell V_{oc} from 696 to 706 mV was realised by further reducing the metal/silicon interface. The front contact line width was reduced from 2.5 to 2 μm and the rear point contact diameter is reduced from 200 μm × 200 μm to 10 μm × 10 μm [34]. The reduced contact areas reduce the recombination at the contact, which contributes to higher V_{oc}.

The very high J_{sc} of PERL cell is attributed to its nearly perfect blue and red response and effective light trapping. Reflection loss at the front surface is minimised to 3.5% using narrow metal fingers, inverted pyramids and a MgF_2/ZnS double-layer ARC [34]. The excellent red response is a consequence of using 400 - 450 μm thick high lifetime FZ substrates, with high quality rear surface passivation. Furthermore, the effective light-trapping scheme, comprising inverted pyramids arranged in a "tiler's pattern" and the dielectrically-enhanced metallic rear aluminium reflector [32], increases the path length of long wavelength light in the cell by up to 40 times [35].

Table 2-2 summaries the performance parameters of PERL cells fabricated on magnetic Czochralski (MCz) and FZ substrates. Both cells demonstrate an efficiency greater than 23%. Compared to PERC cells, the further improvements in cell performance are due to: (i) minimised metal-silicon contact area; (ii) local heavy diffusion under both the front and rear contacts; and (iii) improved light trapping by using a double-layer ARC. Similar to PERC cells, however, the PERL cell is a laboratory high efficiency cell structure which required five photolithographic processes and eight high temperature processes [36]. The increased complexity of the process over that of the PERC is primarily due to the introduction of a local boron diffusion on the rear surface.

The high temperature oxidation steps, used in the fabrication of the first PERC and PERL cells, are not suitable for commercial-grade Czochralski (Cz) silicon wafers, as high temperature processing can result in dissolution and precipitation of impurities,

including oxygen [37, 38], and also may exacerbate some crystal defects which may form due to high ingot pulling rates [39-41]. Furthermore, the cleanliness requirement for the growth of high-quality oxide films is difficult to achieve in an industrial environment [15] thereby increasing the chance that furnaces may become contaminated with impurities that are driven into wafers during the high temperature processing. Therefore, appropriate processes to realise the high efficiency attributes must be developed for industrial high efficiency solar cells. Some of these attempts will be discussed in the next section.

Table 2-2 Electrical characterisation of PERL solar cells (AM 1.5 spectrum, 100 mW cm-2, 25 °C.)

	Resistivity (Ω cm)	Area (cm^2)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF* (%)	η (%)	Ref
PERL MCz	5.2	4	702	41.2	81.1	23.5	[31]
PERL FZ	1.0	4	706	42.7	82.8	25.0	[32]

2.1.3 Industrial PERC/PERL Solar Cells

This section reviews some high efficiency PERC and PERL cells designs that have been implemented in manufacturing, with a view to summarising the strengths and identifying the main limitations of these cell structures regarding further cost reduction.

Table 2-3 summarises the most efficient industrial PERC/PERL solar cells developed by companies and research institutes in the past four years. Cell efficiencies in the range from 19.9% to 21.4% have been reported and most of the efficiencies are independently confirmed. A detailed study of these cell designs highlights four aspects of major changes from the laboratory PERC and PERL solar cells, namely, light trapping, surface passivation, dielectric patterning and metallisation. The techniques of the last three aspects will be reviewed in detail in the following sections of this chapter.

Table 2-3 The best 1-sun light *J-V* results of industrial PERC/PERL solar cells on 156 mm *p*-type Cz silicon and cast mono silicon wafers.

Institute, Cell technology	Year	Wafer type	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF* (%)	η (%)	Ref
Q-cells, Q.antum	2011	Cz-Si	652	38.9	79.9	20.2[a]	[20]
Centrotherm, Centaurus	2012	Cz-Si	---	---	---	19.9[a]	[23]
Suntech,	2012	Cz-Si	674	39.3	73.9	19.7[a]	[21]

Pluto-PERC							
Suntech, Pluto-PERL	2012	Cz-Si	665	40.9	74.4	20.3 [a]	[21]
ISFH, PERC	2012	Cz-Si	655	39.0	78.8	20.1 [a]	[22]
SCHOTT, PERC with SE	2013	Cz-Si	656.3	38.86	79.2	20.2 [a]	[24]
SCHOTT, PERC with SE	2013	Cast-mono	653.9	38.51	78.9	19.9 [a]	[24]
Imec, p-PERL	2014	Cz-Si	665.2	38.6	79.9	20.5 [a]	[25]
Hyundai, PERL	2014	Cz-Si	670.5	40.15	79.41	21.4	[42]

[a] independently confirmed.

Random pyramids resulting from alkaline texturing are commonly-used for arguably all the investigated high efficiency solar cells, due the simplicity and maturity of that texturing process. Although inverted pyramids arranged in a 'tiled pattern' provide excellent light trapping, the gain in J_{sc} is outweighed by the process complexity, the cost of growing the thick thermal oxide mask and cost of photolithographic defined patterning. Moreover, the double-layer ARC is replaced by the SiN_x, deposited by plasma enhanced chemical vapour deposition (PECVD), which not only acts as an effective ARC but also passivates the surface through field-effects [43] and hydrogenation [44].

Alternative dielectrics have been developed for rear surface passivation, because the thermal oxidation process is not a practical industrial viable as discussed in Section 2.1.2. The alternative dielectric ideally meets the following requirements: (i) provides effective surface passivation; (ii) is deposited at low temperatures; (iii) is stable at high temperatures and withstands aluminium firing; and (iv) have a low cost. Therefore, dielectric stacks deposited by PECVD, such as SiO_2/SiN_x [24, 25], AlO_x/SiN_x [22, 25], silicon oxynitride (SiO_yN_x)/SiN_x [23] and SiN_x only [21] are used to passivate industrial-sized wafers. Additional dielectric stacks have been investigated in laboratory studies, namely PECVD amorphous silicon/SiO_y, $SiO_y/SiN_x/SiO_y$ and silicon carbide (SiC_x) [19].

The photolithography patterning process for the front and rear local metal contacts must be eliminated. Alternative patterning technologies with: (i) high resolution; (ii) high processing throughput; and (iii) the ability of *in-situ* patterning without masking, are desirable. Consequently, laser patterning techniques, including

laser ablation [22-25], boron laser doping [21, 45] and laser firing [20], are widely used in the design of industrial PERC/PERL solar cells, with laser ablation being the most widely-used option.

For the front emitter surface, screen-printed silver or plated nickel/copper/(silver) are used as metal contacts for the selective or homogenously-diffused emitter. For the rear surface, local contact formation can be categorised into several general approaches. The first involves screen-printing of aluminium paste on the laser-patterned rear dielectric and firing at high temperatures to form the aluminium-silicon alloyed LBSF. The other approach is to first create the $p+$ regions by using either boron laser doping [45] and then evaporating or sputtering a capping aluminium layer to increase the lateral conductivity. A further alternative is to use laser-fired contacts (LFC) [46].

It is worthwhile noting that the names PERC and PERL are often used interchangeably for rear-passivated local contact solar cells. This is because that most of the cells feature a $p+$ region underneath the rear metal contacts (formed either by aluminium alloying or laser doping). This is similar to the laboratory-fabricated PERL cell where the rear $p+$ regions are formed by local boron diffusion, hence the 'rear locally diffused', rather than laser doping or aluminium alloying. Therefore, for the purpose of disambiguation, in this thesis cells are named PERC if the rear $p+$ regions are formed by aluminium alloying or laser doping rather than masked local boron diffusion.

2.1.4 Summary

The laboratory PERC and PERL solar cells were reviewed and the high efficiency attributes that can be adopted in the design of commercially-produced PERC solar cells were identified. It was concluded that further improvement of cell performance over that achieved by the standard screen-printed cell with an aluminium BSF cell can be achieved with: (i) improved light trapping including ARC and a displace rear reflector; (ii) selective emitter; (iii) effective rear surface passivation; (iv) limited metal-silicon contact fraction; and (v) high bulk lifetime. Unfortunately, many of these attributes require additional processes from that required for standard screen-printed cells or higher quality (and hence more expensive) wafers, which hinders adoption in mass production in the near future.

A selection of PERC solar cells which were considered to be industrial was reviewed. It was shown that alternative processes, such as, alkaline texturing, PECVD surface passivation, laser patterning, metal plating and aluminium-alloyed metallisation, may enable higher efficiency PERC cells on commercial-grade silicon wafers.

2.2 Dielectrics for Rear Contact Design

In the previous section, it was shown that effective rear surface passivation was key to improving cell V_{oc} and hence efficiency. Recombination at a surface can be reduced by: (i) reducing the carrier concentration of one polarity carrier at the surface (e.g., achieved by introducing a BSF [47] or a floating junction [48] or using a dielectric with stored charge [49]); and (ii) reducing the density of surface states (D_{it}) (realised by a number of different methods including immersion in hydrofluoric acid (HF) [50, 51] or iodine/ethanol [52, 53], or by hydrogenation [54-57]). In order to evaluate the strengths and weaknesses of different passivation dielectrics, this section reviews the properties of five passivation dielectrics: SiO_2, SiN_x, SiO_2/SiN_x, AlO_x/SiN_x and anodic oxides. These dielectrics will be used in the following chapters as rear surface passivation dielectrics for the fabrication of PERC solar cells.

2.2.1 Thermally-Grown SiO_2

Thermally-grown SiO_2 (hereafter thermal SiO_2) was widely used in the semiconductor and microelectronics industry especially in the fabrication of metal-oxide-semiconductor (MOS) devices in the integrated circuits [49, 58]. The silicon/SiO_2 interface has demonstrated the lowest reported D_{it} of all investigated dielectrics for silicon, making it the desirable option for applications where a low D_{it} is the main requirement [49]. The use of SiO_2 to electronically passivate silicon solar cell surfaces was firstly reported by Fossum *et al.* in 1979, where both the cell V_{oc} and J_{sc} were improved on *n*+-*p* and *p*+-*n* solar cells due to reduced surface recombination [59]. Then in the following two decades, a high quality thermal SiO_2 layer was extensively used in the design of high efficiency solar cells. This section reviews the properties of the thermal SiO_2 with respect to the growth mechanism, interface quality and its limitations in application.

2.2.1.1 Thermal Oxidation

Thermal oxidation is performed in a clean quartz tube furnace at temperatures in the range of 800 - 1200 °C. An ultra-pure oxidising agent [i.e., oxygen (dry oxidation) or water (wet oxidation)], passes through the wafers at high temperatures and is responsible for the growth of the SiO_2. The mechanism of the SiO_2 growth can be described by the 'Deal-Grove' model [60] which states that for short times the growth rate is proportional to the growth time, *t*, whereas for long oxidation times it is proportional to $t^{1/2}$. The model assumes that the oxidation reaction occurs at the interface between the oxide and the silicon. This displacement of the interface to clean regions within the wafer is one of the main reasons for the excellent quality of thermally grown silicon/SiO_2 interfaces [49]. The oxide growth rate can be influenced by several process related parameters: (i) wet oxidation has a faster growth rate than dry oxidation [61]; (ii) heavily-doped silicon surface (> 10^{20} cm^{-3}) results in a faster oxidation rate; and (iii) an oxide grows 20 - 30% faster on (111)-oriented surfaces than (100)-oriented surfaces [58]. Furthermore, the quality of thermal SiO_2 surface passivation can be improved by adding a few percent of trichloroethane (TCA) into the main stream of oxygen [27, 28]. The chlorine is known to remove metallic impurities from the furnace and the wafer surface due to the formation of metal chlorides.

2.2.1.2 Properties of the Silicon/SiO_2 Interface

The quality of the silicon/dielectric interface is characterised by D_{it} defined as density of states within the forbidden gap E_g of silicon. The density of silicon atoms at the surface is 7×10^{14} cm^{-2}, corresponding to a D_{it} of 1×10^{13} cm^{-2} eV^{-1} on non-passivated silicon surface [49]. The D_{it} of a silicon/SiO_2 interface can be as low as 1×10^{9} cm^{-2} eV^{-1} [62].

Low D_{it} values can be achieved in a number of ways. First, low values can be achieved by oxidation at high temperatures (1100 - 1200 °C) or hydrogenation of dangling bonds by either annealing in the forming gas (4% hydrogen in argon) with the bare oxide or with the oxide covered by an layer of aluminium in a process referred to as *alneal* [63]. In an *alneal*, the source of hydrogen is reported to be due to a corrosive reaction between residual water molecules in the oxide and aluminium, which results in larger density of atomic hydrogen within the oxide [49]. The use of (100)-oriented surfaces can result a D_{it} values that are three to four times lower than that for (111)-oriented surface [49]. This suggests that a (100)-oriented planar rear surfaces may

be beneficial for PERC cells. Finally, although the D_{it} is independent of the doping density (and doping type) when doping concentration is lower than 10^{16} cm^{-3}, with doping concentration exceeding 10^{17} cm^{-3}, it increases linearly with doping [64].

Another important measure of the interface quality is the charge density, including density of the fixed charge, Q_f; mobile charge, Q_m; and charge associated with interface traps, Q_{it} [58, 65]. The Q_f is a sheet of positive charge located very close (< 2 nm) to the interface and is typically a constant. A thermally-grown silicon/SiO_2 interface typically has a Q_f of 5 - 20 × 10^{10} cm^{-2} and Q_f is not influenced by illumination conditions. For a well-prepared silicon/SiO_2 interface, the Q_{it} and Q_m are negligible compared to Q_f [49], therefore only Q_f is considered in this thesis.

2.2.1.3 Limitations of Thermal SiO_2

Although thermal SiO_2 is widely used in the design of high efficiency laboratory solar cells due to its low D_{it}, its use has some limitations. Process wise, as discussed in Section 2.1.2, thermal oxidation requires high temperatures and long processing times, therefore requiring a significant thermal budget. Commercial-grade silicon wafers (e.g., Cz, multi-silicon, quasi-mono silicon) are ideally not subjected to the high temperatures due to the degradation of bulk lifetime by oxygen precipitation in Cz [43, 66] or impurities driving into bulk silicon from grain boundaries in the multi-silicon wafers [67]. Moreover, redistribution of dopants results in boron depletion and phosphorus accumulation at the *p*- and *n*-type silicon surfaces [68], a problem which is more pronounced when a thick oxide layer (> 500 nm) is grown [69].

In terms of surface passivation, thermal SiO_2 provides excellent passivation for high resistivity *p*- and *n*-type silicon surfaces, however the passivation quality for low resistivity *p*-type surfaces is limited [70]. Furthermore, the oxide layer does not contain hydrogen, therefore passivation of interface defects relies on a hydrogen source from either forming gas or from an *alneal*. Finally, the low refractive index, n_r (1.46 [71]), of SiO_2 is too low to be used as an effective ARC on the front surface. In conclusion, a dielectric layer which can be formed at low temperatures and provide effective passivation to silicon surfaces is desirable for commercial grade silicon solar cells. The next section reviews one of the most practical dielectric in this category, namely, SiN_x.

2.2.2 PECVD SiN_x

Silicon nitride films were first successfully used in semiconductors for a large variety of electronic devices in 1965 [72]. Its application to silicon PV was first reported by Hezel and Schorner in 1981 [73]. A metal-insulator-semiconductor inversion-layer (MIS-IL) solar cell was developed using the high interface charge of amorphous hydrogenated SiN_x, which provided effective surface passivation and acted as a good ARC [74, 75]. In the past decade, SiN_x has been investigated by many research groups [72, 76, 77] and PECVD SiN_x ARC was arguably used for all silicon solar cells manufactured in 2013. This section reviews the properties of SiN_x dielectric layers with a special focus on the deposition techniques, properties of silicon/SiN_x interface and associated hydrogen passivation.

2.2.2.1 Deposition Techniques

Silicon nitride can be deposited by three chemical vapour deposition (CVD) processes: (i) atmospheric pressure CVD (APCVD); (ii) low pressure CVD (LPCVD); and (iii) plasma enhanced CVD (PECVD). As summarised in Table 2-4, the PECVD method is advantageous and extensively used in the PV industry because the SiN_x can be formed at temperatures less than 500 °C. The low temperature deposition addresses issues associated with the use of high processing temperatures (i.e., bulk lifetime degradation, dopant redistribution, wafer cleaning and throughput [49]), therefore only PECVD SiN_x is discussed below.

Table 2-4 Deposition technologies for SiN_x.

	Precursor	Temperature (°C)	Pressure (Torr)	Ref
APCVD	SiH_4, NH_3	700-1000	760 (1 atm)	[78, 79]
LPCVD	SiH_2Cl_2, NH_3	700-800	0.01-1	[80, 81]
PECVD	SiH_4, NH_3, N_2	< 500	0.01-1	[82]

There are two types of PECVD reactors, namely direct and indirect. Most industrial PECVD deposition of SiN_x is achieved by direct PECVD. In this process, the wafers are directly in the high frequency plasma of 13.56 MHz. However, this method has drawbacks of: (i) surface damage; (ii) being a slow process; and (iii) complex handling [83]. This limits to some extent the potential of the process to achieve low-cost mass production. In the alternative remote PECVD method the wafer is located outside the plasma and hence there is virtually no surface damage. Moreover, advantages like

directional deposition; high deposition rate; simple handling; and compatibility to deposit on thinner (< 200 μm) and larger (> 200 cm^2) wafers [83], make remote PECVD attractive to silicon PV research and manufacturing. Therefore in this thesis, the remote PECVD system was employed to deposit SiN_x for both ARC and surface passivation proposes.

2.2.2.2 Properties of the Silicon/SiN_x Interface

Determination of the interface quality of the silicon/SiN_x interface by D_{it}, Q_f and capture cross-sections, σ_n and σ_p, is rather difficult because of the high leakage current, especially in silicon rich layers, which can result in hysteresis of capacitance-voltage curves [49]. Albeit the difficulty in measuring D_{it}, studies have consistently shown a moderate D_{it} value at the midgap in the range of 1 - 50 × 10^{11} cm^{-2} eV^{-1} [75, 79, 84-86]. It has been shown that a lower D_{it} can be obtained with higher deposition temperatures [75] or with increased film thickness [86]. The Q_f of SiN_x is reported to be in the range of 2 - 3 × 10^{12} cm^{-2} [77, 79, 85-87]. During the SiN_x deposition, a very thin (< 2 nm) native SiO_x layer is converted to a silicon oxynitride (SiO_yN_x) layer, which results in a similar interfacial quality to a silicon/SiO_2 interface [72, 77, 88]. The Q_f increases with the SiN_x film thickness up to 20 nm due to the transfer of electrons from the SiN_x to the silicon wafer [85, 86], and post deposition annealing nearly halves the Q_f [75, 87]. Owing to dangling bond defects at the silicon/SiO_yN_x interface, the positive charge resides in both the thin SiO_yN_x film and a layer of ~ 20 nm within the SiN_x [49].

2.2.2.3 Hydrogen Passivation

Silicon nitride films contain a high concentration of hydrogen (1 to 2.1 × 10^{22} cm^{-3}) within the film [89, 90]. The hydrogen, both in the atomic and molecular form, can be released in a post deposition annealing process and diffuses into the silicon wafer [87]. Improved surface passivation is obtained with free hydrogen atoms (obtained from breaking weak N-H bonds by annealing) passivating dangling bonds at the silicon/SiN_x interface or within the bulk [91]. This process is referred to as hydrogen passivation. However, excessive annealing can result in the breaking of Si-H bonds, which creates new dangling bonds and therefore degrades passivation [92-94]. Additionally, the Si-N bond density is regarded as a fundamental indicator of the passivation quality of the SiN_x film by Weeber *et al.* [95, 96], with 1.3 × 10^{23} cm^{-3} being identified as an optimum bond density for high quality surface passivation [97]. High effective minority carrier lifetime (τ_{eff}) after annealing was reported on SiN_x films with this bond density [96, 98,

99]. Higher or lower Si-N bond density results in either slow diffusion of hydrogen in the film [96, 98] or fast release of molecular hydrogen, which limits its ability to passivate dangling bonds [100].

Recently, it has been reported that hydrogen plays a role in deactivating boron-oxygen (B-O) defects in *p*-type Cz or upgraded metallurgical grade (UMG) [101, 102]. Hallam *et al.* proposed an enhanced hydrogenation process which reportedly manipulates the charge states of hydrogen [57, 101]. The hydrogen passivation of certain defects is reversible with further thermal treatment without charge states control [57].

In summary, although significant improvements in τ_{eff} have been demonstrated by hydrogen passivation in presence of a hydrogen-containing film like SiN_x, the diffusion and passivation properties of hydrogen in silicon are rather poorly understood with many conflicting results in the literature.

2.2.3 SiO_2 and SiN_x Dielectric Stack Passivation

Given the low D_{it} of the silicon/SiO_2 interface and the advantages of low deposition temperature and high content of hydrogen in the PECVD SiN_x, it is reasonable to investigate the use of SiO_2/SiN_x dielectric stacks for passivation. This section briefly reviews properties of SiO_2/SiN_x stacks on the *p*-type silicon, since it is used as a barrier layer for rear local contact formation in Chapter 3 and a surface passivation layer to establish a benchmark in Chapter 6.

The SiO_2/SiN_x dielectric stack combines the advantages of both improved silicon/SiO_2 interface quality and better field-induced passivation by strong positive charge in the SiN_x [103]. One advantage of using SiN_x as a rear passivation dielectric is because it withstands high temperature firing [104]. Rohatgi *et al.* demonstrated an effective (rear) surface recombination velocity, S_{eff} , of ~ 10 cm s^{-1} on a 1.3 Ω cm *p*-type Cz substrate [105] by growing a rapid thermal oxide (RTO) layer under a direct PECVD SiN_x. They also showed a high temperature anneal at 730 °C after deposition significantly improved the passivation quality of the dielectric stack. Furthermore, the improved thermal stability of SiO_2/SiN_x compared to SiN_x was independently reported by Rohatgi *et al.* [106] and Schmidt *et al.* [91]. Thinner SiO_2 layers (10 - 40 nm) in the dielectric stack were found to result in improved surface passivation. Larionova *et al.* attributes the improvement to the parasitic consumption of atomic hydrogen by dangling

bonds in the thick SiO_2 layer during the hydrogen inward diffusion [107]. This conclusion is of great importance in guiding the experimental work of this thesis, where a 17 ± 1 nm thermal SiO_2 was grown under the SiN_x for improved surface passivation.

2.2.4 AlO_x and SiN_x Dielectric Stack Passivation

Between 2006 and 2008, AlO_x emerged as an effective material to passivate the surface of *p*-type silicon. These layers contain negative charges and are usually applied in combination with a PECVD SiO_x or SiN_x capping film [108, 109]. One significant benefit of the AlOx/SiNx dielectric stacks is that the stored negative charge at the silicon interface of these layers induces an accumulation layer of majority carriers in *p*-type silicon thereby eliminating any risks associated with shunting form a formed inversion layer or injection-dependent surface recombination velocities (*SRV*) [110].

In early work, the AlO_x film was deposited by plasma-assisted atomic layer deposition (ALD) [108, 111, 112], however comparable results were soon achieved using PECVD [113]. The PECVD deposition of AlO_x is advantageous because it can potentially be combined with the deposition of SiN_x in one system but different chambers. When applied to PERC solar cells with low front surface and bulk recombination, it can lead to efficiency gain of up to 1% [15]. Therefore, the AlO_x/SiN_x dielectric stack was used for the fabrication of AJE patterned PERC solar cells in Chapter 3.

2.2.5 Anodic Oxides

Anodic oxides represent alternative passivating dielectrics for silicon solar cells. These oxides can be formed in solution at room temperature (RT) and are able to be grown using in-line wet chemical baths similar to those currently used for texturing and etching in silicon solar cell manufacturing. High processing throughputs may be potentially achieved by transporting wafers with minimal handling in multiple lanes through these baths. This section reviews the formation and property of anodic SiO_2 and AAO, which provide background information for the patterning and anodisation technique development in Chapter 4 - 6.

2.2.5.1 Anodic SiO_2

Anodic oxidation of silicon was first reported as early as in 1957 by Schmidt *et al.* [114]. In the process, a voltage was applied across two electrodes immersed in an electrolyte, where one electrode is usually made of metal (mainly platinum) and the

other is the silicon wafer to be oxidised. In early studies, organic electrolytes were used for growing thick anodic SiO_2 layers [115], whilst pure water was more often used due to its low level of impurities, which may be incorporated into the growing anodic SiO_2 layer [116-118]. In arguably all early studies, a high voltage of 100 - 200 V was required to grow oxide of 20 - 40 nm thick. Anodic SiO_2 has been studied in terms of: (i) different solvents [119]; (ii) different alternating current (AC)/direct current (DC) anodisation methods [120]; and (iii) annealing conditions [121-123], largely for the fabrication of ultrathin gate oxides. Applications of anodic SiO_2 layers have typically focussed on small-area electronic applications where the ability of the anodic oxide to minimise leakage currents in gate oxides has been paramount.

In the past decade, anodisation of silicon in low concentration HNO_3 at low voltage was reported [124, 125]. Grant *et al.* demonstrated the use of such anodic SiO_2 layers for silicon surface passivation to achieve *SRV* of less than 40 cm s^{-1}, which is similar to that attainable with a high quality thermal SiO_2 [126, 127]. The deposition of an equivalent oxide using PECVD has been estimated to require 150 times more energy and significantly higher equipment costs than anodic SiO_2 layers [128]. Albeit the effective surface passivation demonstrated on small area devices and the significant potential in cost saving, the existing process of growing anodic SiO_2 has some drawbacks: (i) anodisation requires electrical contact to the substrate and the use of conductive clips requires that a portion of the substrate is not immersed in the electrolyte; and (ii) anodisation rate is low. Therefore, a new anodisation technique with improved oxide uniformity on large surface area and faster anodisation rate was developed as part of this thesis project and is described in Chapter 5.

2.2.5.2 Anodic Aluminium Oxide

Porous AAO formation was first described in 1941 [129], with subsequent progress in understanding comprehensively reviewed in [130, 131]. There have been numerous applications of AAO. In the metal industry, it is generally used as a protection layer of metal parts due to its excellent corrosion resistance [132, 133]. In nanofabrication, however most applications exploit the porous properties of AAO for patterning/templating functions [134-136].

The electrical properties of the AAO layers have been investigated in terms of stored charge [137-140] and ionic conduction [130]. However, the use of these layers to passivate silicon surfaces had not been considered until the work of the Lu *et al.*

where AAO layers, formed by anodising aluminium layers on the surfaces of the silicon wafers over an intervening dielectric, were shown to reduce the saturation current density to as low as 8 fA cm^{-2} for phosphorus-doped emitters [140]. One of the key advantages of the AAO layer is that it can be formed at RT and atmospheric pressure by anodising a thin aluminium layer in the diluted acidic electrolyte. Early in this study there was no concern regarding the effect of the AAO porosity on its ability to passivate surfaces. However, it was found later in the work of this thesis that the volume expansion coefficient of aluminium and silicon during anodisation are different. This is discussed and addressed in Section 4.5.2.3. Due to above mentioned advantages, AAO is investigated as an alternative low temperature rear surface passivation layer.

2.2.6 Summary

Most commonly-used dielectrics for rear contact design were reviewed. Although thermal SiO_2 results in the lowest D_{it}, its application is predominately limited by the prolonged high temperature and strict cleanliness requirements of the thermal oxidation process. Silicon nitride layers deposited by PECVD and the dielectric stack of SiO_2/SiN_x and AlO_x/SiN_x are widely used in the PV industry as they can be deposited at temperatures below 500 °C and they are beneficial due to field-induced passivation and hydrogen passivation. The concerns associated with the PECVD process are the high maintenance cost of the expensive CVD reactors, the use and treatment of the toxic precursor gases and the limited processing throughput. Therefore, the recent developments in anodic oxide surface passivation, by either anodic SiO_2 or AAO, is of particular interest to this thesis. This leads to the exploration of patterning of AAO layers in Chapter 4 and electrochemical formation of anodic oxides in Chapter 5 and 6.

2.3 Patterning Techniques

Dielectric patterning is critical for fabricating high efficiency solar cells. From the high efficiency attributes outlined in Section 2.1.4, it is concluded that an ideal dielectric patterning technology for industrial solar cells should fulfil the following requirements: (i) high patterning resolution up to 2 µm; (ii) does not substantially degrade the surface passivation; (iii) be able to pattern SiO_2/SiN_x, AlO_x/SiN_x or anodic oxides; (iv) compatible with surface with variable roughness (e.g., polished, planar and textured surfaces); and (v) be cost-effective. Moreover, the technique should be

compatible with patterning 156 mm × 156 mm industrial-sized silicon wafers at a high throughput.

This section contains a review of dielectric patterning techniques. It starts with photolithography, which is a mature technology from the semiconductor industry and a technique used to achieve high efficiency in laboratory solar cells. The focus then moves to alternative patterning methods that have been developed for industrial cell structures. For each technique, the strengths and weaknesses compared to the abovementioned requirements are outlined.

2.3.1 Photolithography

Photolithography is a pattern transfer process that uses light to transfer a geometric pattern from a photomask to a light-sensitive 'resist' on the substrate. The steps involved in the photolithography process are: photoresist application; soft baking; mask alignment; exposure and development; and hard baking. Figure 2-3 illustrates the process flow for a typical photolithography process. It starts with coating of the dielectric and substrate with a thin uniform resist layer. Then a soft-baking removes almost all the solvents from the resist coating, which improves the photosensitivity of the resist. The substrate is then exposed to ultraviolet (UV) light through a photomask. If multiple photolithographic steps are involved, each mask must be aligned to the previous pattern. Depending on the type of resist used, either positive or negative, the exposure to UV light can result in the resist becoming either more soluble or more difficult to dissolve in the developer. Therefore in the following developing process, the unwanted resist is removed, exposing the dielectric underneath. The final step of photolithography is hard baking in order to harden the resist and improve its adhesion to the wafer surface. Finally, after immersed etching and removal of the resist from the substrate, the pattern in the photomask is transferred to the dielectric on the substrate surface.

Figure 2-3 A flow chart for the photolithography process depicting the process flow for both positive and negative resist (adapted from [71])

The key advantage of photolithography is its ability to achieve high resolution patterning, with sub-micron features being etched in the dielectrics by this technique [141]. Therefore it is extensively used in the fabrication of complex integrated circuits.

A modern CMOS wafer may go through the photolithographic cycle up to 50 times [142]. Another advantage is the high precision mask alignment. The PERL cell benefits from these advantages by reducing the front metal-silicon contact line width down to 2 μm and aligning the metal contacts to the heavily-diffused regions [36].

Although photolithography acts as a backbone of the fabrication of the laboratory high efficiency solar cells, it has some drawbacks that hinder its application in commercial PV manufacturing. The costs of photolithography arise from: (i) expensive mask aligners, which need to be maintained in a clean room; (ii) high usage of resist and high resist wastage in the spin-coating processes; (iii) requirement for large volumes of etching solutions including, fluoride-based etching solution, resist developer and stripper; and (iv) high cost in the waste treatment.

In conclusion, photolithography is suitable for integrated circuit fabrication, where a large number of devices are fabricated on a single wafer. It is not suitable for commercial PV manufacturing because of the high cost per wafer.

2.3.2 Laser Patterning Techniques

In the past two decades, laser processing has been widely adopted in high efficiency solar cell designs. The applications of laser include: (i) edge isolation [143]; (ii) contact isolation [144-146]; (iii) laser ablation to enable metal contact through dielectrics [23-25, 147-150]; (iv) laser drilling for EWT [151] and MWT [152]; and (v) LFC [46, 153]. This section contains a review of the patterning techniques using lasers for the purpose of local contact formation.

2.3.2.1 Laser Scribing

Laser scribing is a common method employed in patterning dielectric layers in commercial solar cells. Typically long wavelength (e.g., 1064 nm) Nd:YAG lasers are used to scribe through the dielectrics, removing the dielectric material and creating deep grooves (40 – 50 μm) in the bulk silicon. In 1988, Green and Wenham developed the buried contact solar cells (BCSC), using laser scribing to create openings on the surface [147, 148]. Compared to photolithography, the laser scribing is relatively fast and simple in process. The expensive processes, such as resist application, mask alignment, baking and developing are completely removed. Therefore a variety of BCSC such as double-side buried contact (DSBC) solar cell and the interdigitated backside buried contact (IBBC) solar cell using laser scribing were developed later [154-156].

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-4 Schematic diagram of BCSC featuring laser-scribed buried-contacts [149].

The down side of laser scribing, however, is the potential for laser-induced damage of the silicon crystal during scribing. An alkaline etching process can be used after laser scribing to remove the laser induced damage [149]. However, the cost and complexity of the process are increased, because the cleaning process after alkaline etching is rather critical as a selective diffusion is performed afterwards to from the selective emitter in BC cells. Alternatively, laser scribing can be performed using a shorter wavelength laser with lower power. In doing so the laser damage is significantly reduced and the damage is found to be dissolved during high temperature aluminium alloying. The local contact formation through this approach is studied in Chapter 3.

2.3.2.2 Laser Ablation

Laser ablation is the process whereby the dielectric is removed from the silicon surface by irradiation with a narrow laser beam. Short wavelength (e.g., UV) lasers with narrow pulse width (e.g., ns or ps) are usually used due to their shallower absorption depth and hence lower risk of damaging the silicon substrate. The advantage of laser ablation is its ability to achieve very small patterned features. Spot sizes of 1 μm [157] and grooves as narrow as 6 μm [158] have been reported. This is a much higher resolution than required by commercial PV manufacturing. Additionally, laser ablation is a non-contact process, therefore it is widely used as a rear dielectric patterning technique in fabricating commercial-viable PERC solar cells with cell efficiencies exceeding 20% being reported [22-25].

A common drawback of laser scribing and laser ablation is that they only pattern the dielectric whilst the selective emitter or $p+$ region in the contact area need to be formed by either a high temperature diffusion [159] or by high temperature aluminium alloying.

2.3.2.3 Laser Doping

Numerous attempts have been made to form a selective emitter or rear local contact using a single diffusion step [160-162], with laser-doped selective emitter (LDSE) developed at the University of New South Wales (UNSW) being a promising approach. The laser doping technique, also termed as ‘laser-induced diffusion’, was initially used to form a homogenous emitter across the entire wafer surface [163-165].

Venture *et al.* appear to be the first to report the use of laser doping to form a heavily-doped selective emitter for solar cells [166, 167]. In late 1990s, Wenham *et al.* started work on LDSE with a self-aligned metallisation scheme [168, 169]. In this cell structure, a homogeneous emitter is phosphorus-diffused followed by the deposition of a SiN_x ARC. A phosphorus dopant source was applied on to the wafer surface and the selective emitter was then formed by laser scribing through the dopant source, which simultaneously patterned the dielectric and melted the underlying silicon driving in the phosphorus dopants into the molten silicon. The front metal contact was obtained by self-aligned electroplating of nickel and copper [170].

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-5 Schematic diagram of the double-side LDSE solar cell [171].

Later improvements in LDSE included use of a 532 nm continuous wave (CW) laser which reduced the stress in the silicon due to thermal cycling induced by a pulse laser [172] and use of light-induced plating (LIP) of nickel and copper for front metallisation. Sugianto *et al.* reported cell efficiency of 18.5% on small area (40 mm × 40 mm) of commercial grade Cz silicon wafers [173], which has been further improved by Hallam *et al.* to 19.3% on 125 mm × 125 mm Cz silicon wafers [174]. Hameiri *et al.* then explored the formation of $p+$ region by laser doping using a boron dopant source [175]. Recently, Lee *et al.* reported an efficiency of 21.4% using the LDSE technology using a B-O defect regeneration process to increase the V_{oc} to 674.6 mV [42]. The boron laser doping process is studied with regard to doping local contact regions in Chapter 3 and is used for fabricating AAO-passivated PERC solar cells in Chapter 6.

2.3.2.4 Laser Fired Contacts

Alternatively, local $p+$ contacts can be created by LFC, which was developed at Fraunhofer ISE by Schneiderlochner *et al.* [46, 153]. With LFCs, an aluminium layer is first deposited and then localised aluminium alloying is realised by a fast scanning of laser over the evaporated aluminium. As a result, aluminium is alloyed into the silicon base, resulting in a beneficial $p+$ region with diameter of 80 µm and depth of 2 µm. Cell efficiencies up to 22% were demonstrated with thermal SiO_2 surface passivation [46]. Laser fired contacts eliminate: (i) the need to open contact holes in the passivating layer; and (ii) the sintering step after aluminium deposition.

The disadvantage of LFCs is the limited improvement on lower quality materials [153]. Moreover, the laser beam needs to travel 10 m during contact formation on a 125 mm × 125 mm wafer [176], which lifts the bar for the laser system design to fulfill the requirement of high throughput and reliable patterning for mass production.

2.3.3 Chemical Etching Techniques

Apart from physical patterning techniques, such as laser patterning, the dielectric layer can be chemically removed by applying an appropriate etchant. The typical techniques of chemical etching include: (i) screen printing etching paste; (ii) inkjet etching; and (iii) AJE. This section reviews these chemical etching techniques.

2.3.3.1 Screen-Printing Etching Paste

The technique of screen-printing etching paste was first reported by Kuebelbeck *et al.* [177] and Bahr *et al.* [178]. The etching pastes typically contain phosphoric acid and therefore need to be heated after deposition to initiate the etching reaction [179]. The advantage of etching paste is: (i) the patterning process does not result in degradation of τ_{eff} [180]; and (ii) the availability of suitable printing equipment, making it easy to be implemented commercially. However, due to the use of high temperatures for etching and the low resolution of screen printing, the variation in the etched line width is significant. Bahr *et al.* showed line widths of 85 µm could be achieved after heat treatment at 300 - 400 ° for 90 s [178], however Urrejola *et al.* reported line widths exceeding 100 µm [181]. Etching at RT can be achieved, however at a cost of incorporating corrosive fluoride-based etchants such as ammonium bifluoride (NH_4HF_2) [182]. Additionally, new mask needs to be developed for any new patterns, which further increases the cost and complexity of the process. In conclusion, screen-printed etching paste was considered of limited potential for PV mass production.

2.3.3.2 Inkjet Etching

In recent years the inkjet etching became an emerging dielectric patterning technique for the solar PV industry. Indirect and direct etching using inkjet technology were developed by Utama [183] and Lennon [179], respectively.

Figure 2-6 shows the indirect etching technique developed by Utama *et al.* in 2008 [184]. A thin layer of novolac resin is applied on both surfaces of the silicon substrate. Droplets of diethylene glycol (DEG) are selectively deposited by an inkjet printer on to the resin layer. The DEG plasticises the resin such that the printed region

becomes permeable to dielectric etchant such as HF. The resin not in contact with DEG maintains its resistance to the etchant. The substrate is then immersed in HF which etches the dielectric under the printed region. Finally, the resist is removed from the substrate surface which exposes the silicon surface in the pattered area of dielectric.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-6 Process flowchart of indirect inkjet dielectric patterning (reproduced from [183])

Alternatively, the direct etching technique was introduced by Lennon *et al.*[185], in which two inactive chemicals polyacrylic acid (PAA) and ammonium fluoride (NH_4F) are delivered by spin coating and inkjet printing, respectively. The active etchant HF is only formed *in-situ* in the reaction of PAA and NH_4F and etches the underlying dielectric layer. A schematic process flow for direct etching is shown in Figure 2-7. The direct etching technique is advantageous over indirect etching, because: (i) only a very low concentration of HF is forming *in-situ*; (ii) PAA is a water soluble chemical and hence the residue of chemical can be easily rinsed off after etching; and (iii) the patterning resolution is improved with line width of 25 µm being reported.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-7 Schematic diagram showing the process flow for direct etching method by inkjet printing [185].

Compared to laser patterning, inkjet etching does not introduce process-induced damage and hence no degradation in τ_{eff} during patterning. Although only limited information is published, the First Solar's Tetrasun high efficiency Cz silicon cells are using inkjet patterned dielectrics for metal plated contacts [186].

2.3.3.3 Aerosol Jet Etching

The direct etching technique has been implemented using an aerosol jet printer by Lennon *et al.* and it is referred to as AJE [187]. Figure 2-8 shows the aerosol jet printing process. The mist of NH_4F is generated in an ultrasonic atomiser and carried by nitrogen to the deposition tip. When exiting the tip, the sheath gas surrounds the material and prevents it from contacting the inner surface of the tip. The focused aerosol beam size is less than 10 µm, which potentially increases the patterning resolution. Similar to inkjet direct etching, the AJE process is safer compared to immersion etching in HF. Rodriguez *et al.* demonstrated lines openings as narrow as 20 µm can be

patterned using AJE in a 75 nm thick dielectric layer, including thermal SiO_2, PECVD SiN_x, SiO_yN_x and AlO_x [188].

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-8 A schematic of the aerosol jet printing process [189].

Recently, Rodriguez *et al.* applied the AJE process to patterning the front SiN_x ARC on a 156 mm × 156 mm commercial wafers [190]. It showed that the AJE process was not sensitive to the alkaline textured surface (with roughness of ~ 1 μm) and well-defined lines with uniform 40 μm width were etched with ultrasonic spray coated PAA. Current limitations of the AJE process include: (i) low throughput, patterning time of a 156 mm × 156 mm wafer is ~ 40 min; and (ii) the mist generation is sensitive to the environment. Albeit having the above mentioned limitations, the AJE process is considered to be a novel alternative technique to laser patterning and a useful comparative chemical etching method. Therefore the local contact formation through AJE-patterned dielectrics and fabrication of PERC solar cells are explored in Chapter 3 as a comparison to laser patterning techniques.

2.3.4 Summary

The main limitations of photolithography are high equipment maintenance cost and high process cost including associated chemicals and waste treatment. Therefore it was considered not suitable for mass production, although being fundamental process of many laboratory high efficiency solar cells. Laser patterning techniques, including laser scribing, laser ablation, laser doping and LFC, are widely used in the commercial solar cell fabrication due to their relatively simple process and high throughput. However the laser systems are also of high cost and the laser-induced defects can result in a penalty in terms of surface passivation. These drawbacks can limit cell performance, especially for multi-crystalline silicon cells.

Patterning the dielectric layers using chemical etching techniques, especially inkjet etching or AJE, is promising and represents a useful comparison with laser patterning. Due to the self-limited reaction of etching, only dielectric in the desired pattern is removed, leaving the silicon substrate intact. Studies demonstrated that minimum line openings width of 25 and 20 μm in 75 nm SiN_x were achieved by inkjet etching and AJE, respectively. Therefore, Chapter 3 of this thesis investigates the local

contact formation and fabrication of PERC solar cells through AJE-patterned dielectric layer. In Chapter 4, a new inkjet patterning technique is developed for patterning AAO.

2.4 Local Contact Formation

A key high efficiency attribute of the laboratory PERC/PERL cell is the reduced recombination by rear surface passivation and the limited metal/silicon contact area. In commercially-produced solar cells, the latter can be achieved by either forming rear local back surface field (LBSF) regions through openings in a passivating dielectric layer. This section firstly reviews the mechanism of local contact formation and then discusses the existing local contact formation techniques through AAO, a dielectric of interest to this thesis.

2.4.1 Mechanism of Local Contact Formation

The concept of passivating the rear surface of silicon solar cells by using an alloy-through back contact process was first introduced by Mandelkorn and Lamneck in 1972, where aluminium diffused high-low junctions were used to repel the minority carriers from the back surface. This high-low junction was then commonly referred to as a 'back surface field' [47]. In 1990, Zhao *et al.* introduced the PERL cell which featured a passivated rear surface with a 'local back surface field', formed by local diffusion through a photolithographically-patterned thick thermal SiO_2 layer [18]. In recent years, a considerable amount of literature has been published on combining the PERC structure and screen-printed metallisation, with a SiO_2/SiN_x or AlO_x/SiN_x dielectric stack replacing the thick oxide layer [108, 109]. The mechanism of forming a LBSF through patterned dielectric layers is therefore being extensively studied [191-195].

2.4.1.1 Aluminium-Silicon Alloying

A contact formation model, which is based on aluminium-silicon alloying for a full area BSF [196], was proposed by Grasso *et al.*[191]. Figure 2-9 shows the mechanism of the LBSF formation at 900 °C. The alloying process can be summarised in the following six steps.

(1) An interface of aluminium and silicon is established in the local openings and organic solvent is removed from the aluminium paste by heating.

(2) The alloying process starts with the melting of the aluminium at 660 °C. Silicon begins to dissolve in the aluminium and an aluminium-silicon liquid is formed at the interface. According to the phase diagram of the aluminium-silicon binary system [197] (see Figure 2-10), the concentration of silicon in the aluminium-silicon liquid is 17% at 660 °C (point 2) and this concentration gradient is a driving force for the silicon dissolution.

(3) Further increase in the firing temperature (from point 3 to 4) results in excessive dissolution of silicon into aluminium. Due to the presence of the native oxide on the outer surface of the aluminium paste, the volume of the paste is kept constant during firing [198]. Therefore the same volume of aluminium is transported towards the silicon surface to compensate the silicon out diffusion. The maximum concentration of silicon in the aluminium paste is determined by the peak firing temperature (e.g., 35% silicon in aluminium at 900 °C).

(4) During the cooling step (from point 4 to 5), silicon segregates out from the aluminium-silicon liquid as the solubility of silicon in aluminium decreases, and the matter transport process in step (3) is reversed. The segregated silicon grows epitaxially on the silicon substrate and simultaneously the aluminium is incorporated into the silicon according to the temperature dependent solid solubility. This forms an aluminium-doped LBSF. In the inter-diffusion process between aluminium and silicon, the rates at which the two types of atoms diffuse are not the same. Therefore during fast cooling, the high generation of vacancies may cause the nucleation and formation of voids due to the Kirkendall effect [199]. Furthermore, the uniformity and continuity of LBSF regions can be improved by intentionally increasing the concentration of silicon into the aluminium paste [194].

(5) When the temperature is reduced to the eutectic temperature of 577 °C (point 6), the remaining aluminium-silicon liquid solidifies in an aluminium-silicon alloy of eutectic composition (e.g., 12.2% silicon in aluminium).

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-9 Schematic depicting the mechanism of LBSF formation [191].

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-10 The aluminium-silicon binary system phase diagram [196].

2.4.1.2 Thickness of Aluminium

Prior studies have noted the importance of the thickness of the screen-printed aluminium layer in determining the thickness and uniformity of the full area BSF. Insufficient thickness of aluminium results in a thin liquid aluminium-silicon layer which serves as source of silicon during the epitaxial growth of the *p+* layer. This results in the formation of a discontinuous BSF and hence a strongly increased *SRV* [196]. On the other hand, medium to thick aluminium layers fired at high peak temperatures (e.g., > 850 °C) leads to an agglomeration of the liquid aluminium-silicon into islands. A relationship between firing temperature and the aluminium thickness is shown in Figure 2-11. The agglomeration results in a significant variation in the BSF thickness with thick BSF forming underneath the islands and thin BSF in the adjacent areas [200]. Moreover, thicker aluminium layers are also more sensitive to the temperature ramp-up profile during the pre-fire baking step. A slow ramp-up to the baking temperature is desirable to avoid the build-up of cavities in the paste due to volatilisation of solvents which may remain in the paste [196].

For LBSF regions, however, the sensitivity of its formation to the thickness of aluminium paste has not been reported. Although efforts were made to optimise the aluminium paste for forming thick and uniform LBSF regions, there have been no reports showing the solution to the agglomeration issue. The assumption is that the thickness of aluminium will also affect the LBSF formation in a similar manner to the full area BSF.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-11 Highest peak firing temperature and corresponding screen printed aluminium thickness (measured after firing) where the agglomeration of liquid aluminium-silicon can be avoided [200].

2.4.1.3 Spreading of Silicon in Aluminium

During firing, more silicon diffuses into the aluminium than aluminium into the silicon, due to the higher solubility of silicon in aluminium [201]. Once in the aluminium, the silicon diffuses laterally to regions adjacent to the contact openings, forming a visible dark-grey region along the line contact. Urrejola *et al.* [202] suggested that, after firing, the width of the dark-grey region indicates the spread limit of the diffused silicon in the aluminium, S_{limit}, and it only depends on the firing temperature

but not the line opening width. The spread of silicon in a screen-printed aluminium layer is reported to be a diffusion-limited process, which increases by 1.5 ± 0.06 μm K^{-1} with increasing peak temperature in the rage of 750 - 950 °C. It was found that by reducing the contact spacing and overlapping the spread silicon in aluminium, the aluminium layer saturates faster and the probability of forming a thick LBSF increases [203]. Therefore Urrejola *et al.* concluded the design of contact spacing should be equal to or smaller than the S_{limit} for forming thick LBSF.

2.4.1.4 Line Opening Width and Spacing

Although the line width does not affect the spread of silicon in aluminium, it is found to influence the geometry of the local contact [192]. Figure 2-12 shows that a homogeneous LBSF is found to form in narrow lines (e.g., 80 μm). With line widths exceeding 100 μm, deep alloying occurs at the edges of the linea with the width of these regions being ~ 50 μm each. The alloyed regions formed in lines openings with even wider line widths (e.g., more than 250 μm) start to separate from each other, leaving a planar surface similar to the full area BSF in the centre of the line [192].

The line spacing determines the probability of the Kirkendall void formation. It was found that the void percentage increases significantly with increasing line spacing [204]. It was hypothesised that the diffusion of silicon in aluminium was determined by the amount of aluminium mass on each side of the dielectric openings. Larger spacing increases the aluminium to silicon volume ratio, thereby further reducing the boundaries for the diffusion of silicon into aluminium. A high concentration of silicon atoms was found away from the contact area, implying the increased amount of trapped silicon in the matrix during cooling, which led to the vigorous formation of the voids with large line spacing [204].

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-12 Cross sectional scanning electron microscopy (SEM) image showing the change of contact geometry with increased line spacing [192]. The white line in (a) to (c) indicates the extent of the LBSF region in silicon. (d) shows the silicon surface after removal of the fired aluminium.

2.4.1.5 Kirkendall Void Formation

The formation of voids, instead of eutectic regions, in the contact area is commonly observed when high temperature firing is performed. These voids are believed form due to the Kirkendall effect, which describes the inter-diffusion of two solids with different diffusion rates in their solid counterparts. The diffusion mechanism of the two solids is better described as interstitial rather than substitutional. The formation of vacancies makes room for atoms to move in the other solid. At high temperatures, the inter-diffusion process of aluminium and silicon generates a high density of vacancies, which may coalesce in the melt, causing the nucleation and formation of Kirkendall voids [205].

Fast cooling is reported to be another cause of Kirkendall voids [202]. As shown in Figure 2-13, the change of aluminium-silicon liquid follows the path A-B in the case of slow cooling and results in a eutectic region with 12.2% silicon in aluminium. However fast cooling can be described by the path A-C, where silicon is trapped in the aluminium-silicon liquid, forming a hypereutectic. This results in a void at the aluminium/silicon interface. Therefore in the experiments reported in this thesis, samples patterned using different methods were fired together with the same firing temperature profile, to eliminate the error introduced by variations in the cooling rate.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 2-13 Aluminium-silicon phase diagram showing the effect of cooling rate (reproduced from [197]). The path A-B reflects the slow cooling path, whereas path A-C reflects fast cooling.

2.4.2 Local Contact Formation through AAO

Several local contact formation schemes through an AAO rear passivation layer have been proposed due to its potential to be used as an effective surface passivation. The section contains a brief review of these techniques in order to evaluate their strengths and limitations.

2.4.2.1 Self-Patterned Localised Contact

As discussed in Section 2.3, the difficulty for commercially available technologies is patterning localised contacts with low cost, high-throughput, and robust processing, especially when closely-spaced small-area openings are required. Lu *et al.*

proposed a technique using self-patterning AAO layers to enable localised metal contacts and surface passivation simultaneously [206]. Local contacts were formed by depositing and firing the capping aluminium layer deposited on top of an AAO layer on a textured silicon substrate. After firing at 750 °C, metal contacts were formed at the peaks and valleys of the alkaline-textured silicon surface and the specific contact resistivity was estimated to be ~ 6 mΩ cm^2.

Although the self-patterned contact formation can eliminate the need to deliberately pattern the dielectric and the contact fraction can be manipulated by varying the anodisation conditions and the surface morphology, process control was difficult. The contact spacing closely depended on the surface texturing, which may vary from batch to batch in an industrial environment. However, most importantly, cell V_{oc} values were limited by the formation of thin LBSF regions.

2.4.2.2 Laser Scribing Using AAO as Dopant Source

Alternative local contact formation through AAO was reported by Lu *et al.* [207], in which laser scribing is performed through a SiO_2/SiN_x/AAO dielectric stack, creating an aluminium-doped *p*+ region in the laser-scribed lines. In this method, the 600 nm AAO layer acted as *p*-type dopant source. The resulting *p*+ regions extended more than 10 µm into the silicon and the concentration of electrically-active dopant exceeded 10^{20} cm^{-3} for the first 6 - 7 µm [207]. Advantages of this technique are the elimination of boron dopant source, which is harmful to human health [208] and the simplicity of the process. However the inherent drawback of this technique is the use of a triple-layer stack of thermal SiO_2, PECVD SiN_x and AAO. The cost reduction achieved from removing boron dopant source can be overwhelmed by increased cost in thermal oxidation and SiN_x deposition. Therefore a potential solution to improve is to eliminate the SiN_x layer and replace the thermal SiO_2 by anodic SiO_2. In process reported by Lu *et al.* [207], the intervening SiN_x layer was necessary in order to prevent residual aluminium in the AAO firing through the intervening dielectric layer (i.e., as described for the method discussed in Section 2.4.2.1)

2.4.3 Summary

The mechanism of forming local contact by aluminium-silicon alloying was reviewed. Aluminium-doped LBSF regions are formed by epitaxial growth of silicon at the silicon/eutectic interface. The uniformity and thickness of the LBSF regions are determined by the contact size, spacing, thickness of the aluminium and firing

temperatures. The LBSF regions can be characterised by the S_{limit} of silicon in the aluminium, thickness and the percentage of Kirkendall void formation. At the end of this section, two recently-reported approaches of forming local contact regions through AAO layers were also reviewed. Poor process control of the self-patterned contacts and the complex process of the laser scribing contacts are identified as major limitations of these processes. Therefore, a new dielectric patterning and metallisation technique via AAO is purposed in Chapter 4 and the fabrication of AAO passivated PERC cells are discussed in Chapter 6.

2.5 Chapter Summary

The design of a high efficiency PERC/PERL solar cell consists of three main design principles: passivation dielectric, patterning and local contact formation (metallisation). These three principles are interrelated to each other. First of all, an ideal dielectric should result in a low D_{it} and sufficient amount Q_f of a polarity that preferably induces an accumulation layer of carriers in the silicon. The dielectric layer should be patterned effectively and reliably in order to enable metal contacting the silicon in localised areas. High efficiency solar cells usually requires feature sizes in the range of tens of micrometres and the dielectric has to be completely removed in the patterned area for the formation of high quality metal contacts. Last but not least, the local contact formation is vital for the cell performance, because it determines the current and voltage of the cell. Contact formation is closely related to the properties of the dielectric and the quality of patterning. On the one hand, the dielectric needs to withstand the attack of metal during the metallisation firing, which is usually performed at high temperatures. On the other hand, the quality of contacts formed depends on the feature of patterns in the dielectric (e.g., opening width, point or line spacing, resolution of the edge, as well as the presence of dielectric residues in the openings). Therefore, the design of a commercial-viable high efficiency PERC solar cell in this thesis takes all of the above mentioned principles into consideration.

Chapter 3 Dielectric Patterning and Rear Local Contact Formation

Chapter 2 suggests that chemical etching techniques may be advantageous compared to laser-patterning because no process-induced defects are introduced and the τ_{eff} is maintained after dielectric patterning. This chapter first describes the optimisation of the AJE process for patterning 200 nm SiO_2/SiN_x dielectric stacks. Then it investigates three dielectric patterning techniques: laser scribing, boron laser doping, and AJE from the perspective of rear local contact formation. It begins with an investigation on the physical properties of LBSF regions with respect to: (i) S_{limit} of silicon in the aluminium; (ii) thickness; (iii) line widening effect; and (iv) Kirkendall void formation. Subsequently, the fabrication of PERC cells with AJE-patterned rear local contacts is reported, with a highest cell efficiency of 18.5% being achieved. An electrical characterisation and a loss analysis of the most efficient cell are presented.

3.1 Introduction

Rear local contact structures, which reduce the effective rear *SRV* by forming LBSF regions through patterned dielectrics, enable higher cell energy conversion efficiencies than cells employing a full area aluminium-alloyed BSF [19]. Prior research has shown that the LBSF formation is sensitive to: (i) dielectric opening size; (ii) spacing of openings; and (iii) aluminium firing process [192, 194, 203, 209-211]. Discontinuous BSF regions and Kirkendall voids have been reported due to poor selection of contact spacing and firing conditions [202]. It is also reported that the intentional addition of silicon into the aluminium paste can significantly improve contact geometry by reducing contact depth and increasing BSF thickness [194].

In most of the previous studies in local contact formation, openings in rear passivation dielectrics were formed by either laser ablation [146, 193] or screen printing of etching paste [192, 193, 212]. According to Section 2.3, boron laser doping [21, 45, 213] and AJE [185] have also been used to pattern the dielectric layer. The AJE is a low temperature process (e.g., [185]), which eliminates damage to the silicon wafer and minimises the influence on temperature-sensitive hydrogen passivation processes [57,

91, 101, 102, 214]. However, the properties of the LBSF regions formed through AJE-patterned dielectric layer have not yet been reported.

This chapter first describes the optimisation of the AJE for patterning thick dielectrics. It then investigates the effect of different dielectric patterning techniques on formation of the LBSF regions. Line openings were patterned using laser scribing, boron laser doping and AJE in a 200 nm SiO_2/SiN_x dielectric stack. The metal contacts were then formed by alloying screen-printed aluminium at high temperatures. The LBSF regions were imaged by SEM with the depth of the *p*+ regions being visualised using selective etching. A batch of PERC cells, with AJE-patterned rear surfaces, were fabricated and characterised to demonstrate the effectiveness of the chemical etching patterning method.

3.2 Optimisation of Aerosol Jet Etching Process for Patterning Thick Dielectrics

In recent years, several publications have reported the patterning of 75 nm SiN_x dielectric layers using AJE [188-190]. However, there are limited reports on the patterning of thicker dielectric layers, apart from using inkjet etching [215]. Initial experiments showed that the patterning of thicker dielectric layers by AJE was more difficult because of etchant spreading, deposition tip clogging and other issues associated with the increased volume of etchant required and prolonged etching time. In this section, the critical printing parameters were investigated and an optimised AJE process for achieving narrow and continuous line openings in a 200 nm SiO_2/SiN_x dielectric stack is reported.

3.2.1 Polymer Layer Thickness

Chemical etching was performed using an aerosol jet printer (Solar lab system, Optomec). Stock polyacrylic acid (PAA) solution [average MW ~250,000 g mol^{-1}, 25% (w/v) in deionised (DI) water, Polysciences] was diluted in DI water to 20% (w/v). Prior to aerosol jet printing, the dielectric surface was spin-coated with water-soluble 20% (w/v) PAA. The spin speed was programmed to start from 2000 rpm and increased to 7000 rpm in 10 s and stay at the top speed for 20 s, which yielded a PAA film of ~ 2 μm thick on a planarised surface. The thickness of the spin-coated PAA film was

determined by both the spin speed and the concentration of PAA used as described in [216]. Since the volume of the *in-situ* formed active etchant depends on the reaction between PAA and NH_4F in the localised area, a thin PAA film may result in insufficient reactant and therefore incomplete etching. On the other hand, if the PAA film is too thick, a larger volume of NH_4F solution is required to completely dissolve the water-soluble polymer and expose the underlying dielectric [188]. Consequently, in these experiments, which involved the patterned etching through a 200 nm SiO_2/SiN_x dielectric stack, a ~ 2 μm of PAA film was used. However, further optimisation of the PAA thickness may achieve reduced volume of printed NH_4F and reduced material waste during spin coating.

3.2.2 Mist Generation and Gas Flow Rates

The mist of 10% (w/v) NH_4F [diluted from 40% (w/v) in DI water, J.T. Baker] was generated by an ultrasonic atomizer with voltage of 42 V and then delivered by nitrogen and deposited on the substrate surface through an Al_2O_3 deposition tip. The maximum atomizer voltage of 45 V was not used, because variations in the mist generation and poor uniformity of the etched lines caused by the unstable power output at the maximum voltage. The cooling water temperature for ultrasonic atomizer was kept at 25 °C at all times for stable mist generation.

The volume of material deposited onto the substrate is primarily determined by the atomizer flow rate (AFR) if the printing speed is constant [188]. Line width increases with larger AFRs, most likely due to the spreading of the dissolved polymer region when more fluoride aerosol is deposited. For low AFRs, however, the dielectric may not be etched completely due to an insufficient amount of NH_4F. Therefore, the AFR was varied in the range of 10 to 15 sccm for reliable mist transportation. For improved resolution of printing, a cylinder of sheath gas is supplied at the deposition tip to confine the aerosol mist from contacting the inner wall of the tip. With larger AFRs, the sheath gas flow rate (SFR) needs to be increased for a reinforced shielding effect. However, for the range of AFRs studied in these experiments, a SFR of 25 sccm was shown to be effective for uniform deposition.

3.2.3 Printing Speeds

Printing speed in AJE is defined as the speed at which the platen moves. In general, line widths increase with slower printing speeds and increasing numbers of

printed layers [188]. The depth of etching is also positively correlated to the volume of etchant deposited. Hence, both the number of printed layers and the printing speed affect the etched line width. Figure 3-1 shows this interdependency of printing speed and number of layers for patterned etching of a 75 nm PECVD SiN_x layer [188]. A large number of layers at high printing speed provides the same volume of etchant as fewer layers at a low printing speed, which in theory should yield the same depth of etching. The following experiment explored the effect of printing speed on the etched line width for a 200 nm SiO_2/SiN_x dielectric stack.

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Figure 3-1 Graph showing how the etched line width varied as the number of printed layers and printing speed were varied. The experiment was performed on a textured silicon wafer coated with a 75 nm PECVD SiN_x layer that was fired at a peak temperature of 850 °C after deposition [188].

3.2.3.1 Experimental

The process optimisation of AJE was performed on test structures fabricated on wafer fragments of size ~ 40 mm × 40 mm. A batch of 15 alkaline-textured and single side planarised *p*-type Cz wafers were RCA cleaned [217] and oxidised in a quartz tube furnace to form a ~ 17 nm SiO_2 layer on both sides. A PECVD SiN_x layer of 180 nm thickness was then deposited on both surfaces (see Figure 3-2). A ~ 2 µm PAA layer was spin-coated over the SiN_x surface as described in Section 3.2.1 and 10% (w/v) NH_4F was aerosol jet printed using a 100 µm diameter deposition tip, with the AFR and SFR controlled at 15 sccm and 25 sccm, respectively. A platen temperature of 60 °C was used based on the fact that it was most effective when etching 75 nm SiN_x layers. The printing speed was varied (2, 3, 4, 6 and 8 mm s^{-1}) and the number of printed layers was varied (4, 8, 16 and 22 layers) for each printing speed. The chemically-etched line openings were inspected under a microscope and the line width was measured.

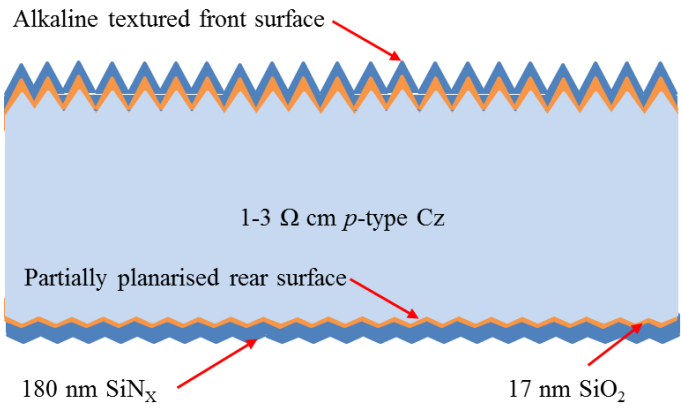

Figure 3-2 Test structures used for the AJE patterning optimisation.

3.2.3.2 Results and Discussion

Figure 3-3 shows that when 10 layers of etchant were printed, the average line width reduced dramatically with increasing printing speed. Although a line width of 40 µm was demonstrated at the speed of 8 mm s^{-1}, the dielectric was not completely etched due to the reduced amount of etchant deposited at the higher printing speed. On the other hand, the use of a slow printing speed resulted in a build-up of aerosol, which increased the risk of tip clogging, and spreading of the deposited fluid on the substrate. Therefore a medium printing speed of 4 mm s^{-1}, with a larger number of printed layers was used, aiming for cleanly etched lines of 40 µm wide. As shown in Figure 3-4, 10 layers of NH_4F were printed using a 100 µm deposition tip at a printing speed of 4 mm s^{-1} for each opened line, which resulted in an etched line width of ~ 60 µm.

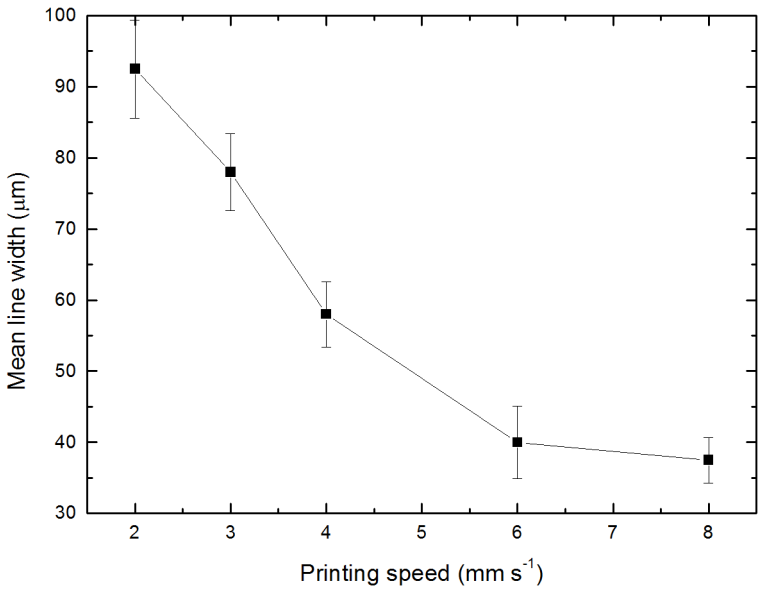

Figure 3-3 Mean etched line width graphed as a function of printing speed for lines etched in 17 nm SiO_2 / 180 nm SiN_x. The number of printed layers was 10 for all experiments and all other printing parameters were as detailed in Section 3.2.3.1. The error bars represent the standard deviation of five individual measurements.

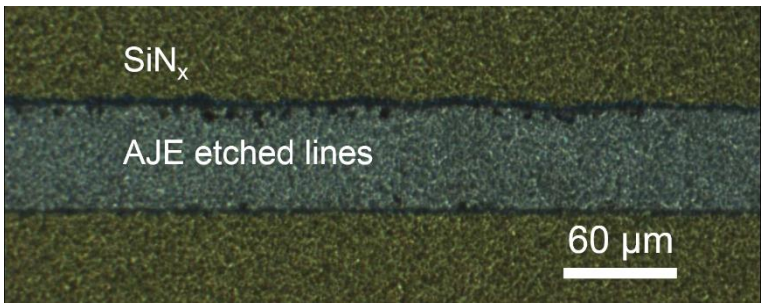

Figure 3-4 Microscope image of AJE etched lines with 10 layers of NH_4F printed using a 100 µm deposition tip at a printing speed of 4 mm s^{-1}, which resulted in an etched line width of ~ 60 µm.

3.2.4 Platen Temperature

The temperature of the platen determines the temperature of the etchant and the evaporation rate of the water, both of which affect the etching reaction rate [188]. Like most etching reactions [218], water is required for etching. Excessive evaporation of water in the deposited aerosol can result in a reduced etching rate [185].

3.2.4.1 Experimental

A batch of nine wafers was prepared. The test structure preparation and AJE were performed according to Section 3.2.3.1. The platen temperature was varied from 50 to 70 °C with an increment of 10 °C. Line openings after etching were measured using an optical microscope.

3.2.4.2 Results and Discussion

Figure 3-5 shows that low platen temperatures results in increased line width, because of the spreading of dissolved polymer regions due to reduced water evaporation. Temperatures higher than 60 °C reduced the line width, at a cost of having discontinuous lines due to the faster evaporation of water from the NH_4F solution. A high platen temperature may also affect the unregulated tip temperature and cause tip clogging during printing. A medium platen temperature of 60 °C resulted in complete etching and an acceptable line width of ~ 65 μm, which was in agreement with the findings of Rodriguez *et al.*, who showed the platen temperatures in the range of 50 - 60 °C resulted in clean and consistent etching of 75 nm SiN_x [188]. Therefore, the platen temperature of 60 °C was used for all experiments and, after printing, the wafers were left on the processing stage at 60 °C for 25 min to ensure complete etching of the 200 nm SiO_2/SiN_x stack layer.

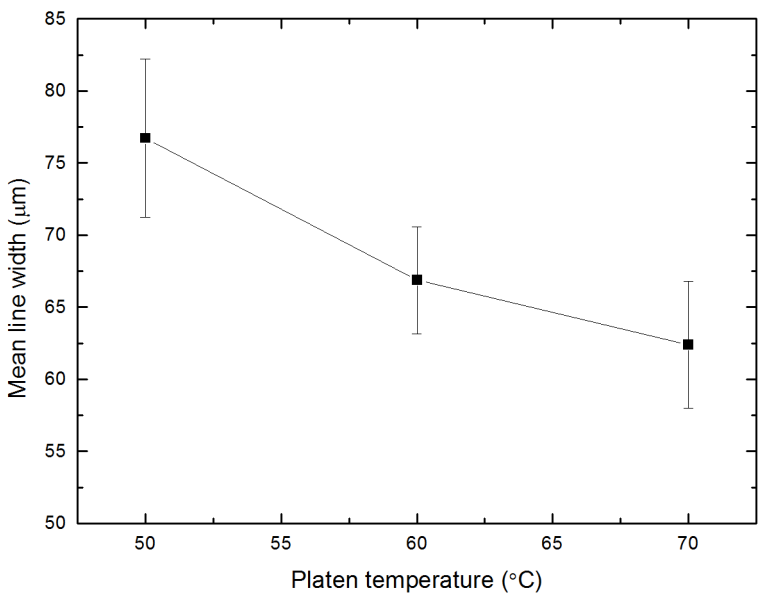

Figure 3-5 Mean etched line width graphed as a function of platen temperature for lines etched in 10 nm SiO_2 / 200 nm SiN_x. The number of printed layers was 10 for all experiments and all other printing parameters were as detailed in Section 3.2.3.1. The error bars represent the standard deviation of five individual measurements.

3.2.5 Deposition Tip Size and Tip-to-Substrate Distance

The deposition tip sizes of 100, 150 and 200 μm were investigated for the purpose of achieving high resolution printing. With the same AFR, larger tips result in the deposition of more material and therefore increased the etched line width. This maybe suitable for high throughput etching when printing resolution is less essential. However for the purpose of this work, high printing resolution (e.g., small etched line width) was required, therefore the smallest 100 μm tip was used.

Akhatov *et al.* showed the Saffman force [219] acting on aerosol particles in a gas flowing through a micro-capillary causes migration of particles toward the centre line of the capillary [220]. Consequently, there is a specific point at which the aerosol beam width is reduced to its minimum. Moreover, the aerosol focusing effect is dependent on the size of the micro-capillary (in this case, the tip). It was found that for 100 μm tips, the optimum distance is less than 2 mm; for 150 μm tips, it is within 3 – 4 mm; and for 200 μm tips, it is within 4 - 5 mm [190]. The highest printing resolution can therefore be achieved by adjusting the tip-to-substrate distance. Due to the physical limitation of the shutter between the tip and the substrate, the minimal tip-to-substrate distance in the aerosol jet printer used is ~ 2 mm. It was set for printing using the 100 μm tips in these experiments, unless otherwise specified.

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Figure 3-6 Laser-illuminated aerosol beam leaving 100 μm micro-capillary [220]. The tip is on the left side and the substrate (not shown) is on the right.

3.2.6 Summary

An optimised AJE process for patterning 200 nm SiO_2/SiN_x dielectric stacks was developed. Even after optimisation, the resulted line widths were still considerably wider than previously reported for 75 nm SiN_x due to the difficulty of etching through a 200 nm dielectric layer. Narrower line widths could be achieved on thick SiN_x films if geometric confinement was applied [216]. However confinement increased the complexity of the patterning process, and therefore was not adopted in the experiments reported in this chapter. Table 3-1 summarises the optimised printing parameters used for patterning 200 nm SiO_2/SiN_x dielectric stacks.

Table 3-1 Optimised AJE parameters for etching 200 nm SiO_2/SiN_x stack layers.

AJE Parameters	Values
PAA concentration	20% (w/v)
PAA coating thickness	2 µm
NH_4F concentration	10% (w/v)
Atomizer voltage	42 V
Atomizer cooling water temperature	25 °C
AFR	10 - 15 sccm
SFR	25 sccm
Printing speed	4 mm s^{-1}
Number of layers	10
Platen temperature	60 °C
Tip size	100 µm
Tip-to-substrate distance	~ 2 mm

3.3 Formation of Local Back Surface Field through Different Patterning Techniques

Having developed a robust AJE process for patterning 200 nm SiO_2/SiN_x dielectric stacks, the formation of LBSF regions via laser scribing, boron laser doping and AJE were investigated. This section reports on the physical properties of the LBSF regions formed through these different patterning techniques.

3.3.1 Experimental

3.3.1.1 Substrate Preparation

The results described in this section were achieved using small wafer fragments of 40 mm × 40 mm, 180 µm double-side alkaline-textured *p*-type Cz silicon wafers, with a bulk resistivity of 1 - 3 Ω cm. Figure 3-7 shows the sample preparation procedure. An *n*-type emitter with a sheet resistance of 150 Ω/□ was formed by solid source phosphorus diffusion at 850 °C for 12 min. The wafers were then immersed in 1% (w/w) HF (J.T.Baker) to completely remove the phosphosilicate glass. A 5 min etch in the isotropic silicon etchant 'Trilogy Etch' [221] was then performed to remove phosphorus, which had diffused into the wafer's rear surface, whilst the front surface was protected by an FSC-M novolac resin surface coating (Shipley Company Inc.). A 17 nm thermal SiO_2 layer was grown on both surfaces using dry oxidation at 980 °C for 18 min in a

quartz tube furnace, and then SiN_x was deposited on both surfaces using a Roth & Rou AK 400 remote PECVD. The thickness of the dielectric stack on the front surface was 75 nm (n_r = 2.05), while a 200 nm layer with an identical n_r was deposited on the rear surface. The thick SiN_x layer acts as a barrier during metallisation, which prevents aluminium from contacting silicon in the non-patterned area. A post-deposition anneal in nitrogen ambient at 400 °C for 20 min was performed to enhance hydrogen passivation [56, 101].

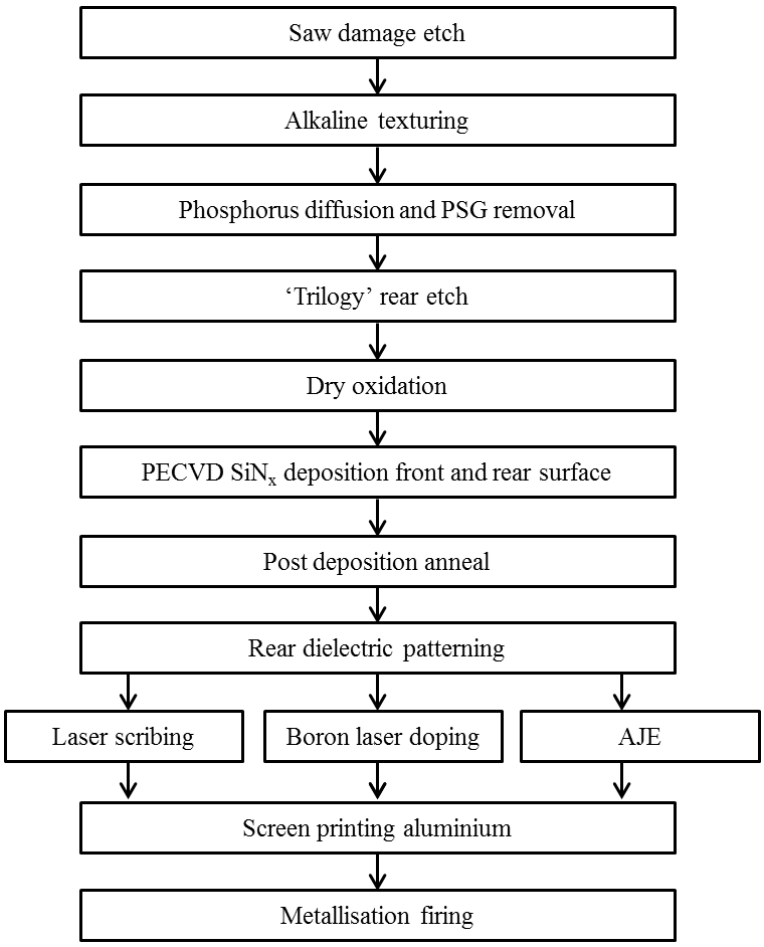

Figure 3-7 Process flow for sample preparation.

The passivated wafers were divided into three groups. The rear dielectric layers of the wafers in the different groups were then patterned by: (1) boron laser doping; (2) laser scribing; and (3) AJE (using the parameters reported in Section 3.3).

3.3.1.2 Dielectric Patterning

Laser patterning, including boron laser doping and laser scribing, were performed with a 532 nm CW laser (Spectra-Physics) using identical laser settings to allow comparable results. For boron laser doping, a thin layer of boron spin-on dopant

source, poly-boron film (PBF-1, Filmtronics), was spin-coated onto the dielectric surface at 3000 rpm for 20 s, followed by baking in a dehydration oven at 130 °C for 10 min to remove any solvents. A laser power of 15 W and laser speed of 500 mm s^{-1} were used to ensure a sheet resistance as low as 5 Ω/□ in the boron laser-doped *p*+ regions [222]. After laser doping, the boron laser-doped wafers were rinsed in DI water (18 MΩ cm) for 10 min to completely remove residue of the dopant source.

As the 532 nm laser irradiates to a depth of ~ 1 μm into the substrate [223] at the laser power and speed used, it simultaneously removes the dielectric layer and melts the silicon substrate in the laser irradiated regions in the case of laser scribing. Therefore, according to the discussion in Section 2.3.2.1, the term 'laser scribing' is used in this thesis rather than 'laser ablation'. Although laser ablation using a UV laser is beneficial, it was not studied due to the limitation of no available UV laser.

In these experiments, LBSF formation was investigated as a function of the line contact spacing and the firing temperature. Therefore, line openings were patterned with the line spacing varying from 0.2, 0.5, 1, 2 to 4 mm. The initial line opening width of ~ 25 μm was readily and reproducibly achieved for both laser patterning techniques.

The AJE patterning was performed using the optimised parameters summarised in Section 3.2.6. Line openings were patterned with line spacing varied from 0.5, 1, 2 and 4 mm. The 0.2 mm spacing was eliminated due to the relatively bigger line width of the etched line openings (60 - 70 μm) comparing to laser-patterned lines.

3.3.1.3 Screen-Printed Aluminium

After patterning, all wafers were then screen-printed using a semi-automatic screen printer (EKRA E4) with aluminium paste (Dupont's L9245), which has been specifically developed for localised rear contacts. According to the discussion in Section 2.4.1.2, the thickness of aluminium in these experiments was controlled in the range of 25 - 30 μm to avoid non-uniform LBSF formation due to agglomeration at 850 °C. After printing, the wafers were baked in a dehydration oven at 150 °C for 25 min to remove organic solvents in the paste. The ramp up rate during baking was not controlled as the cavity formation was trivial for the thickness of aluminium used. The wafers were then fired in a Centrotherm belt furnace with six heating zones, using a belt speed of 5400 mm min^{-1} at peak firing temperatures ranging from 700 to 850 °C with an increment of 50 °C. Other belt speeds were used to investigate the sensitivity of the

process to belt speed, however in the following discussions a belt speed of 5400 mm min^{-1} should be assumed unless otherwise specified. This speed corresponded to the wafers being exposed to the set peak firing temperature for duration of ~ 4 s. Under fast ramping conditions, the wafer passes through the eutectic point and reaches the peak firing temperature very quickly. This promotes uniform alloying and improves BSF uniformity [210]. Therefore, the temperatures of the first four heating zones was set to 250, 350, 450 and 550 °C, respectively and the last two zones were set to the peak firing temperature as mentioned above to ensure uniform alloying. The thickness of the screen-printed aluminium layer after firing was 20 - 25 µm.

3.3.1.4 Characterisations

Optical microscope images were recorded after patterning and belt furnace firing to determine the width and uniformity of the line openings, as well as the spreading of silicon in the aluminium after firing. The latter could be determined by measuring the width of the 'dark grey' region covering the line openings under a light microscope. For all wafers, the LBSF regions were exposed by cleaving the wafers using a Q-Switched, Nd:YAG laser at 10 kHz frequency from the non-metallised surface and then etching for 20 s in an CH_3COOH: HNO_3: HF = 6: 3: 1 solution. The solution etches $p+$ silicon at a much faster rate than lightly-doped silicon [224]. The wafer cross sections were then imaged by SEM and energy-dispersive X-ray spectroscopy (EDS) to visualise the $p+$ LBSF regions and to estimate their depth and uniformity.

The temperature profile of the belt furnace was measured using a thermocouple, which was connected to a data recorder stored in a heat resistant box. When the temperature of the furnace was stabilised at each set temperature, the data recorder was placed on the belt and travelled through all heating and cooling zones, with the tip of thermocouple probing the front surface of the wafer (i.e., surface without aluminium). The temperature was then recorded at an interval of 0.1 s and recorded as a function of time.

3.3.2 Results and Discussion

3.3.2.1 Temperature Profile

The aluminium-silicon alloying process is primarily determined by the peak firing temperature and the cooling rate. Therefore it is important to investigate the temperature profile of the furnace. Figure 3-8 illustrates the temperature profiles with

set peak firing temperatures (T_{peak_s}) as 750, 800 and 850 °C and a belt speed of 5400 mm min^{-1}. A significant difference between the set peak temperature and the measured peak temperature (T_{peak_m}) was observed (see Table 3-2), with the T_{peak_m} being lower by up to 90 °C. This difference may be caused by three reasons: (i) the time that the wafers were exposed to the peak temperature zones was too short to achieve the set temperature; (ii) the thermocouple in the profiler was not calibrated to the temperature sensor in the furnace, therefore a systematic error might have occurred; or (iii) the temperature of the front surface of the wafer might have differed from the rear aluminium surface. The difference between the set and T_{peak_m} became more pronounced with higher belt speeds (see Figure 3-9) and raised a concern in interpreting and comparing results from different research groups, as this difference may vary significantly from furnace to furnace. Despite the difference observed, the results presented in this chapter are discussed with reference to the T_{peak_s}. The results from different firing conditions were considered to be comparable as the same belt furnace was used for all experiments.

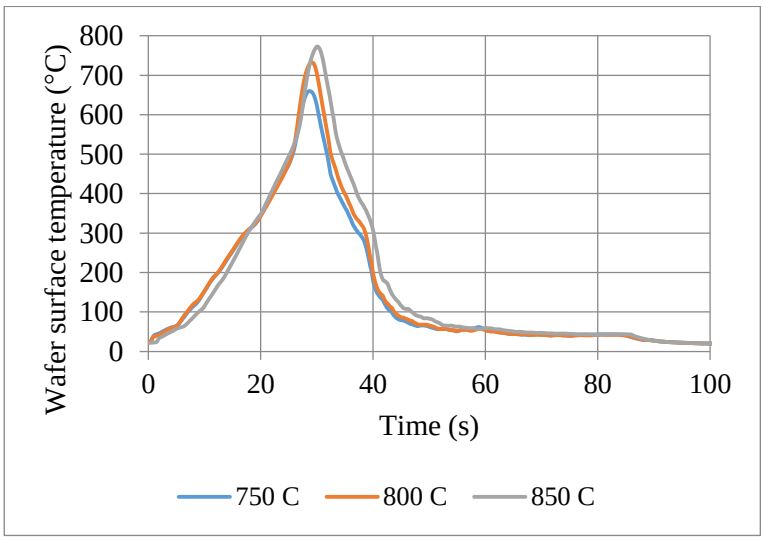

Figure 3-8 Temperature profiles of T_{peak_s} being 750, 800 and 850 °C and a 5400 mm min^{-1} belt speed.

The cooling rate, $R_{cooling}$, was calculated based on the slope of the temperature profile from peak temperature to eutectic temperature. Assuming the epitaxial growth of the LBSF starts from the beginning of the cooling period, the epitaxial growth time can be determined by the following relationship:

$$t_{epi} = \frac{T_{peak\_m} - T_{eutectic}}{R_{cooling}} \quad (3.1)$$

where t_{epi} is time for epitaxial growth of LBSF, $T_{eutectic}$ the eutectic temperature of 577 °C. As the cooling zone of the furnace was not controlled, the cooling air flow was identical in all the firing profiles. It was found that $R_{cooling}$ increased with higher peak temperatures, and the time for epitaxial growth of LBSF was also increased due to the larger difference between the T_{peak_m} and $T_{eutectic}$.

Table 3-2 Comparison of actual firing temperature, cooling rate and alloying time for the different firing profiles used.

T_{peak_s} (°C)	T_{peak_m} (°C)	T_{peak_s} - T_{peak_m} (°C)	$R_{cooling}$ (K s^{-1})	t_{epi} (s)
750	660	90	-45	1.9
800	733	67	-68	2.3
850	772	77	-70	2.8

The repeatability of the temperature profile was investigated by passing five wafers through the furnace under identical temperature settings after the temperature readings were stabilized. Figure 3-9 shows the temperature profiles of the five passes. In general, the profiles were consistent with each other, evidenced by the characteristics (e.g., plateaus and kinks) of each curve. However in the peak temperature zone, a difference of 25 °C was observed between the five passes. This variation may have been caused by the position of the small wafers on the conveyer belt or the contact between the thermocouple and the wafer. Since this maximum 25°C variation is small compared to the temperature interval of 50 °C used in these experiments, the error was considered to be acceptable.

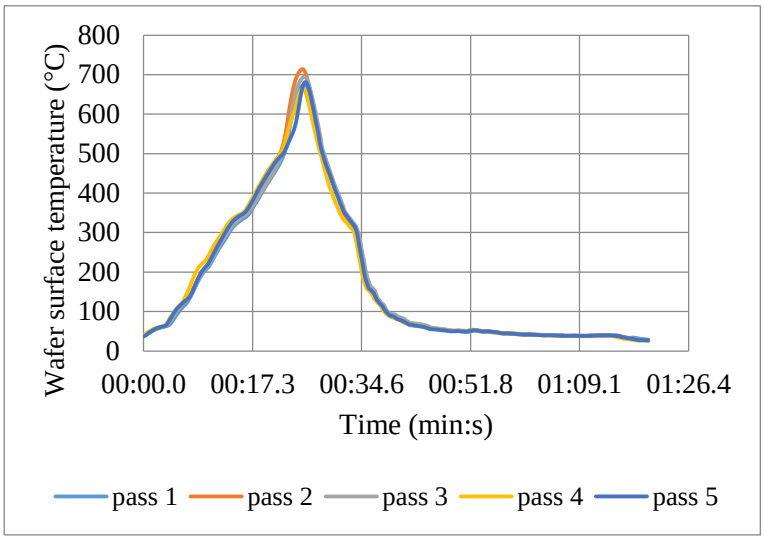

Figure 3-9 Temperature profiles of the 810 °C peak temperature profile with 6000 mm min^{-1} belt speed. The thermocouple passed the firing zone five times and variation up to 25°C in the peak temperature was observed.

3.3.2.2 The Spread of Silicon in Aluminium

In this work, S_{limit} was defined as half of the difference between the maximum width of the spread region, d_2, and the initial line opening width, d_1 (see Figure 3-10).

$$S_{limit} = \frac{d_2 - d_1}{2} \tag{3.2}$$

Figure 3-10 and Figure 3-11 show the S_{limit} of silicon in aluminium for contacts formed by boron laser doping, laser scribing and AJE as a function of peak firing temperatures. The S_{limit} for all patterning processes increased with increasing peak firing temperature, which is in good agreement with [202]. At the peak firing temperature, silicon dissolution and diffusion into aluminium occur simultaneously. If it is assumed that the aluminium region directly above the opening immediately saturates with silicon and remains that way, then in theory the S_{limit} should not depend on the opening width or the silicon dissolution rate (i.e., as observed by Urrejola *et al.* [202]). However, if the silicon dissolution rate is slow and varies between opening types, then the above-mentioned assumption is not necessarily valid and wider lines should result in a larger S_{limit}.

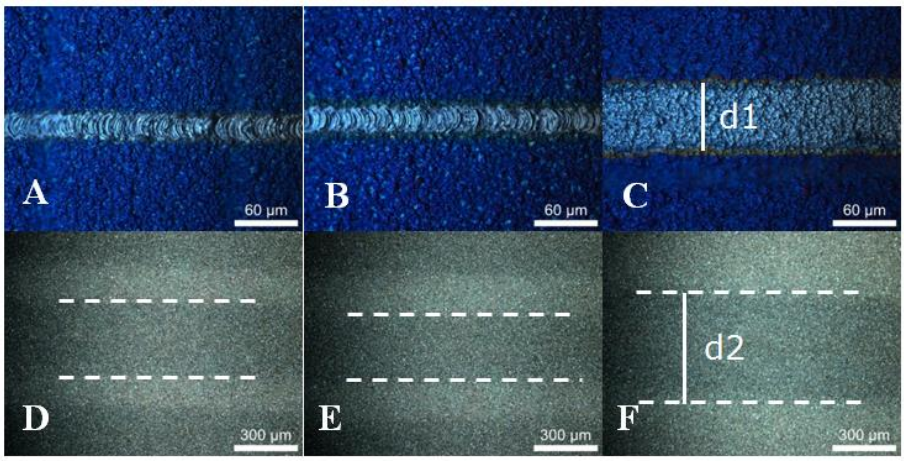

Figure 3-10 Optical microscope images of patterned lines (top row) and spread of silicon in the aluminium after firing at 750 °C with a 5400 mm min^{-1} belt speed are shown as dark-grey region in between the dashed white lines (bottom row). The lines were patterned by boron laser doping (a), (d); laser scribing (b), (e); and AJE (c), (f), respectively.

According to Figure 3-11, the fact that the S_{limit} for the AJE openings is very similar to those of laser-patterned openings, despite that the AJE lines being about three times wider, suggests that the silicon dissolution rate is relatively fast for all types of openings. Moreover, a consistent difference in S_{limit} between the three patterning techniques implies that the spread of silicon in aluminium is limited by both dissolution and diffusion, with the latter being a stronger limiting factor. The variation in S_{limit} for different firing temperatures may have been caused by the different dissolution rates at the silicon surfaces exposed by different patterning techniques. To confirm this it would be necessary to form laser openings of the same width as the AJE lines. However the use of multiple overlapping passes may result in further variations in the exposed silicon surface and therefore also affect the dissolution rate.

The laser patterning process involves considerable melting and re-crystallisation of the silicon. The crystal defects generated in this process result in more strained silicon-silicon bonds, which could be expected to make silicon dissolve more rapidly in the aluminium due to a larger effective surface to volume ratio. This possibility is supported by the fact that the re-crystallised silicon etches more rapidly in the selective $p+$ etching solution that was used to image the BSF regions [see

Figure 3-13(d)]. Furthermore, residue from the dielectric layer, which is incorporated into the silicon lattice in the opened area, may also have impacted the dissolution of the silicon. This is in contrast to the AJE lines, which would have been

free of residue from the dielectric layer. The hypothesis is evidenced in Figure 3-11 where the S_{limit} of laser-patterned lines is generally larger than the AJE lines at all temperatures.

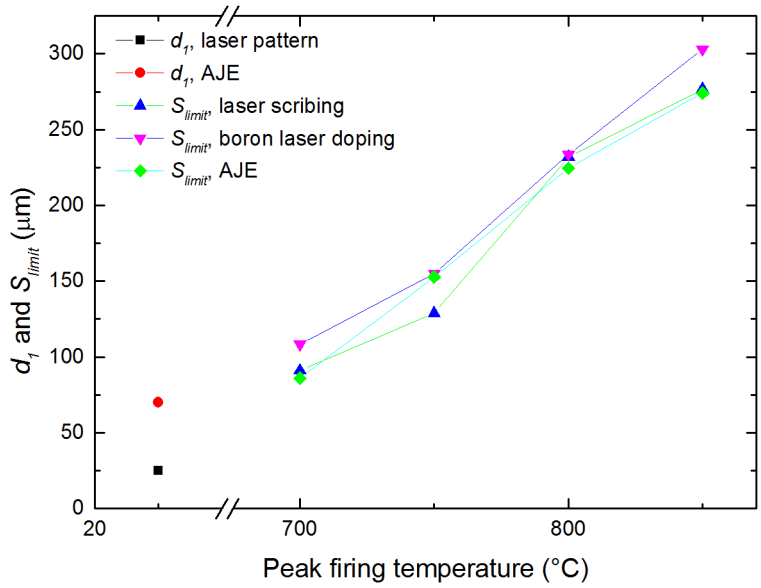

Figure 3-11 Spread limit of silicon in aluminium after firing. The y-axis represents the S_{limit} of silicon based on optical measurement of d_2 and d_1 after patterning versus the peak firing temperature for boron laser doping, laser scribing, and aerosol jet chemical etching. The value of d_1 of laser-patterned and AJE lines are provided as references.

Interestingly, the boron laser-doped openings showed a wider S_{limit} than the laser-scribed lines [see Figure 3-10(d) and (e)], given identical initial line opening widths. As both sets of lines were laser-processed with identical laser speed and power, the only difference in the opened regions was the presence of additional boron dopants. Therefore, it is hypothesised that stress introduced by impurity atoms during the doping process weakens the bonds between silicon atoms, which may enhance the rate at which silicon atoms can diffuse into the aluminium, hence increasing the S_{limit}.

In summary, the spreading of silicon in aluminium is primarily limited by diffusion. Although there are reasons to suggest that the silicon dissolution rates could vary at the silicon surfaces exposed by AJE and laser-patterning, the results presented here suggest that these effects may be minimal.

3.3.2.3 Thickness of Local Back Surface Field

Thickness and uniformity of the LBSF regions are important indicators of their effectiveness as a shield for the minority carriers [191, 193, 194]. Chen *et al.* [225]

showed that a LBSF regions with thickness of at least 2 μm was required to achieve effective local contacts on the rear surface of a solar cell. If the LBSF regions was thick enough (e.g. > 3 μm), its uniformity had less impact on cell performance. Figure 3-12 shows the thickness of the LBSF regions formed using the three different dielectric patterning techniques, with varied line spacing and peak firing temperatures. The thickness of LBSF was determined by process detailed in Section 3.3.1.4. Missing data at 700 °C is due to failed alloying at the low temperature. This result is consistent with reports that the melting of the aluminium starts at ~660 °C locally on the silicon surface [196]. If the firing temperature is too low (i.e., 700 °C) the thickness of LBSF regions is strongly limited by four factors: (1) the molten aluminium only partially wets the silicon surface, resulting in inhomogeneous LBSF regions in the line contact; (2) the low driving force of silicon dissolution into aluminium leads to an unsaturated aluminium layer directly above the contact opening and hence not enough silicon is segregated out during the epitaxial growth of the $p+$ layer; (3) during the cooling period, the t_{epi} is short; and (4) the process is sensitive to the variation of the T_{peak_m} and T_{peak_s} in the conveyer belt furnace.

There is also data missing for the temperatures of 800 °C and 850 °C because of the excessive formation of Kirkendall voids in the eutectic region, leaving partial or failed formation of the LBSF regions (see Section 3.3.2.5).

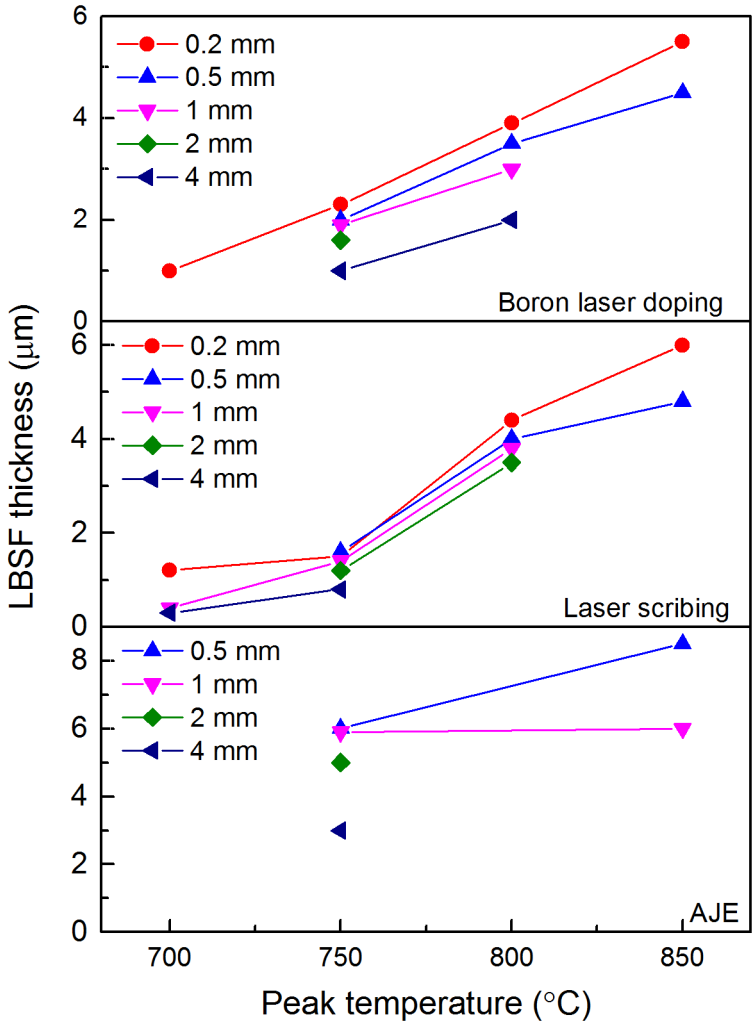

Figure 3-12 The thickness of LBSF formed through dielectrics patterned by boron laser doping, laser scribing and AJE patterning with varied line spacing and peak firing temperatures. All wafers were fired with identical belt speed of 5400 mm min^{-1}.

For all three groups, the thickness of the LBSF regions increased with increasing peak temperature for samples with identical line spacing. This was because at the higher peak temperatures, the solubility of aluminium in silicon is increased [226], hence making the concentration of aluminium higher at the initial interface during liquid phase epitaxial growth. Moreover, as discussed in Section 3.3.2.1, a higher peak temperature allows longer time for the sample to cool to the eutectic temperature, thus resulting in longer t_{epi} and therefore a thicker LBSF. There appears to be a relationship between the thickness of LBSF and the S_{limit} of silicon in aluminium. Boron laser doping, which resulted in the largest S_{limit}, yielded the thinnest LBSF of the three groups, while the LBSF regions resulting from AJE lines were usually 2 to 3 μm thicker than those formed from boron laser-doped lines at identical peak temperatures. This observation

was expected because during cool down, the silicon is only partially segregated from the liquid aluminium-silicon reservoir at the interface. Therefore not all the silicon that has laterally-diffused in the aluminium layer diffuses back to the contact region, especially the silicon that spread further in to the aluminium as in the case of boron laser doping, resulting in a lower concentration of silicon in aluminium in the region above the epitaxial growth region and a thinner BSF region.

The wider AJE lines may also contribute to forming thicker LBSF by nature of their flatter shapes (see Figure 3-13). If it is assumed that the amount of silicon dissolved is limited by its saturation in the aluminium layer [203], then the thickness of the LBSF regions will be largely determined by the effective diffusion of silicon back to the recrystallising surface. The silicon diffusing back to the openings from the lateral regions needs to saturate a thicker layer of aluminium above the contact area with the hemispherical shapes of the contact regions that result from the narrower laser-processed lines. Consequently, a thinner LBSF is formed.

A disadvantage of using AJE was the poorer uniformity of LBSF thickness across the opening area, with the centre being the thickest and the edges the thinnest [see Figure 3-13(c)]. Large variations in thicknesses were not observed for laser-patterned lines. Non-uniformity has also been observed for wider than 100 μm laser-patterned openings, where thick LBSF regions only form towards the edges of the openings. A similar observation was also reported by Urrejola [192] and Uruena [193] as discussed in Section 2.4.1.4, when the LBSF was formed via large openings (~ 100 μm) patterned by screen printing etch paste. In other words, the improved uniformity in thickness that resulted in the laser-processed openings may simply be due to the different opening size rather than a property of the different patterning processes.

The thickness of the LBSF also depends on the line spacing. At each peak temperature, it decreased with increased line spacing. This difference was as large as 3 μm between chemically-etched lines spaced 0.5 mm and 4 mm apart when they were fired at 750 °C. The cause of this difference is believed to be due to the overlapping of the silicon-saturated aluminium. For closely-spaced lines (e.g., 0.2 mm and 0.5 mm), the $2S_{limit}$ is larger than the spacing. Therefore, silicon-saturated aluminium overlaps for the neighbouring line contacts, which enhances the silicon segregation during cooling. When the line spacing exceeds the $2S_{limit}$, the driving force for silicon back diffusion is

reduced. Consequently, the aluminium layer overlying the opening does not saturate resulting in thinner LBSF regions.

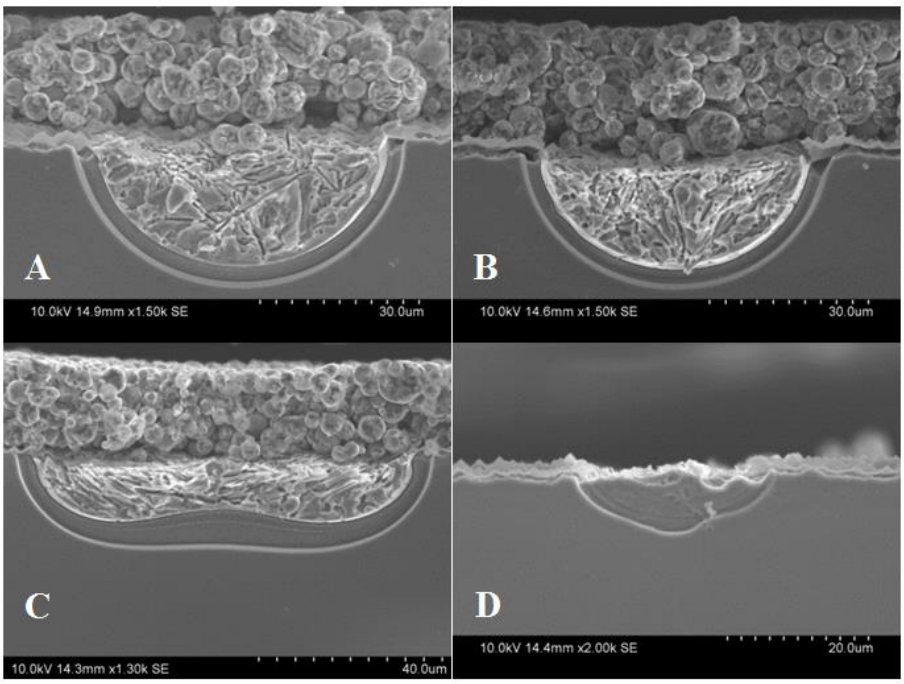

Figure 3-13 Cross sectional SEM images of LBSF regions formed where a 200 nm SiO_2/SiN_x layer was patterned by boron laser doping (A); laser scribing (B); and AJE patterning (C). The contacts were spaced 0.5 mm apart and fired at 850 °C, where (A) and (B) were fired with a belt speed of 5400 mm min^{-1} and (C) with a belt speed of 6400 mm min^{-1}. (D) shows a cross sectional image of a laser ablated line after selective *p*+ etching.

This difference in the thickness due to different line spacing is more pronounced with increasing peak temperature. At higher temperatures the diffusivity of silicon in aluminium is increased, resulting in increased silicon diffusion away from the line openings. Therefore, thicker LBSF regions can be obtained for all dielectric patterning methods by spacing lines closer together. Close spacing can however represent a problem for laser-patterned openings where device voltage can be reduced by excessive laser damage. It's also challenging for AJE because the metal contact fraction increases, due to the difficulty in further reducing the etched line width. If contacts are spaced too far apart, voids instead of eutectic regions will be formed in the contact area, because of the high generation of vacancies during the silicon-aluminium inter-diffusion at high firing temperatures [202].

3.3.2.4 Line Widening Effect

For rear local contact solar cells, the contact fraction, defined as the area ratio of metal/silicon contact area to the entire cell surface, determines the cell's rear effective *SRV* and rear series resistance. The PERL cell used a 1% rear contact fraction as a balance between low rear *SRV* and minimized rear series resistance (R_s) [227]. Suntech's Pluto-PERL cell achieved 20.3% efficiency on 125 mm × 125 mm commercial grade *p*-type Cz wafers, with a 1% rear contact fraction by limiting the rear effective *SRV* to 100 cm s^{-1} and rear R_s to 1.1 Ω cm^2 [21]. It was found that line widening occurred during firing and thus dramatically increased the contact fraction on final devices.

The boron laser-doped lines appeared to have the smallest increment in line width when fired between 750 to 850 °C (see Figure 3-14). The percentage increase was 116% after firing at 850 °C for 0.5 mm spaced lines. This increment in line width was slightly more for laser-scribed lines which increased by 132% at identical firing temperature and line spacing. In both cases the line width was increased by more than 100% upon firing at 850 °C. In contrast, although the AJE patterned lines were widened, the percentage increment was much less, with 0.5 mm spaced lines increased by ~ 50%. However, it is difficult to directly compare the line widening of the AJE patterned and laser-patterned lines because of the different initial width.

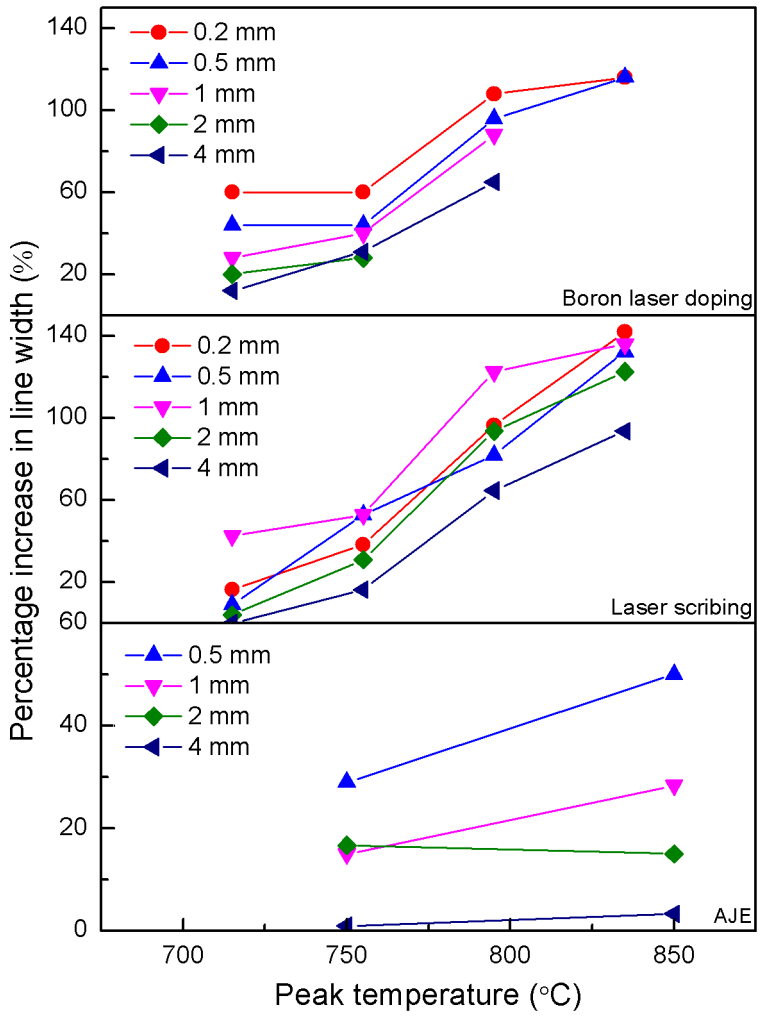

Figure 3-14 Percentage increase in line width before and after firing of contacts formed via dielectrics patterned by boron laser doping; laser scribing; and AJE patterning with varied line spacing and peak temperatures. Line width before firing was measured on microscope images after patterning (Figure 3-10) and that of after firing was measured from SEM cross sectional images. Only one sample was processed and measured for each condition.

Interestingly, the lines with narrower spacing experienced more line widening than lines spaced further apart. This trend is especially clear for boron laser-doped and AJE lines, and it is also similar to the trend of thickness of LBSF regions with respect to line spacing as discussed in Section 3.3.2.3, suggesting a link between the alloying process and line widening. The SEM images show that in many cases some residue of the dielectric layer appears to remain above the LBSF region suggesting that silicon dissolution proceeds laterally underneath the dielectric which effectively extends the width of the opening. The recrystallised silicon lattice that resulted from laser patterning is dissolved more rapidly in the aluminium due to the more strained silicon-silicon bonds, therefore stronger laterally dissolution of silicon occurs. On the contrary, in the

AJE lines, there was no recrystallisation of silicon and hence reduced widening was observed. The saturation of aluminium with silicon above the dielectric regions adjacent to the line openings may result in an increased dissolution of silicon on heating due to the increased fluidity of the surrounding molten alloy. Moreover, it is also possible that aluminium and silicon mixing occurs through defects in the dielectric layer immediately adjacent to the opened area caused by the laser.

3.3.2.5 Kirkendall Void Formation

Figure 3-15 (A), (B) and (C) show Kirkendall void formation in lines patterned by the three different approaches respectively. A comparison between Figure 3-15 (C) and (D) shows that the Kirkendall voids are serious problem for localised rear contacts, because where the voids are formed there is no metal/silicon contact, which significantly increases the R_c.

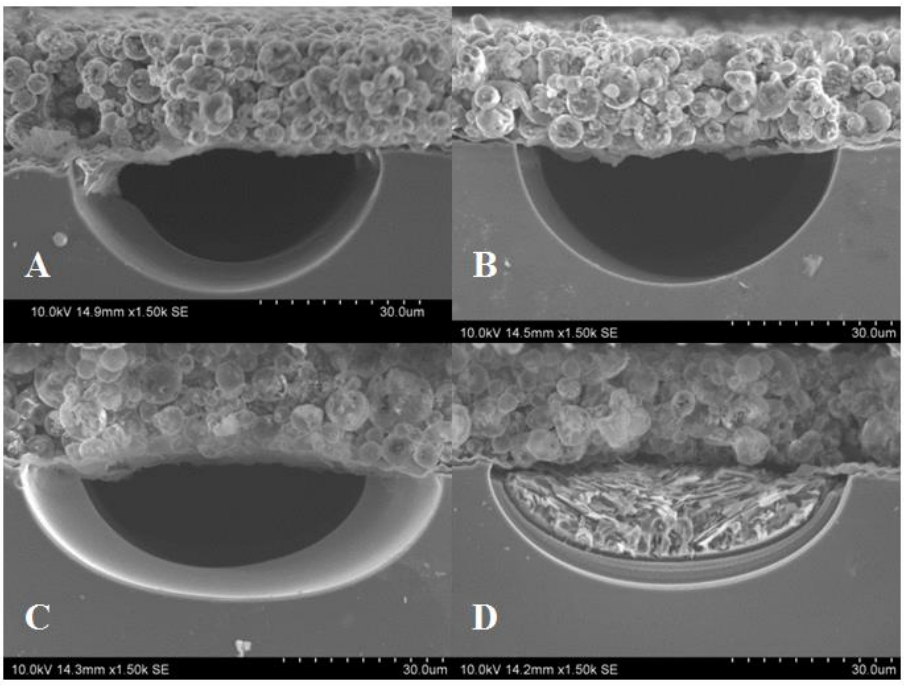

Figure 3-15 Cross sectional SEM images of Kirkendall voids formed in lines patterned by boron laser doping (A); laser scribing (B); and AJE (C). (D) shows a good contact achieved with the same patterning and firing condition as used for (C). All line openings were spaced 1 mm apart and fired at 850 °C with belt speed of 5400 mm min^{-1}.

The percentage of line contacts (out of 10 lines which were sampled with identical spacing) containing voids is presented in Figure 3-16 for each patterning technique. The percentage of Kirkendall voids was found to be correlated to: (i) peak temperature; (ii) line spacing; and (iii) S_{limit}. However the trends are different for the

different patterning techniques. Laser scribed lines with spacing less than 2 mm are less likely to form voids compared to boron laser doped lines, presumably because of the smaller S_{limit}. When the line spacing exceeds 2 mm, the void formation is dominated by the line spacing rather than S_{limit}, hence the two laser patterning methods showed similar trends. With the AJE lines the relationship between void formation and line spacing was not clear. At lower temperatures (e.g., 750 °C), chemical etching results in fewer voids even with 4 mm spacing compared with the laser-patterned lines. However, at 850 °C this advantage appears to no longer exist, because the peak temperature is dominating the process due to excessive silicon dissolution and diffusion in the aluminium at high temperatures. These results suggest the potential advantage of forming good quality LBSF using chemical patterning, given the peak temperature is no higher than 800 °C.

It is instructive to note that a large number of Kirkendall voids form with a line spacing of 1 mm, which is commonly adopted for PERC cells. Without imaging, the presence of these voids can only be indirectly inferred through higher R_s in the final devices. The thick screen printed aluminium may be causing the vigorous formation of voids, therefore it was hypothesised that using a thinner layer of aluminium (e.g., evaporated aluminium) may represent a solution.

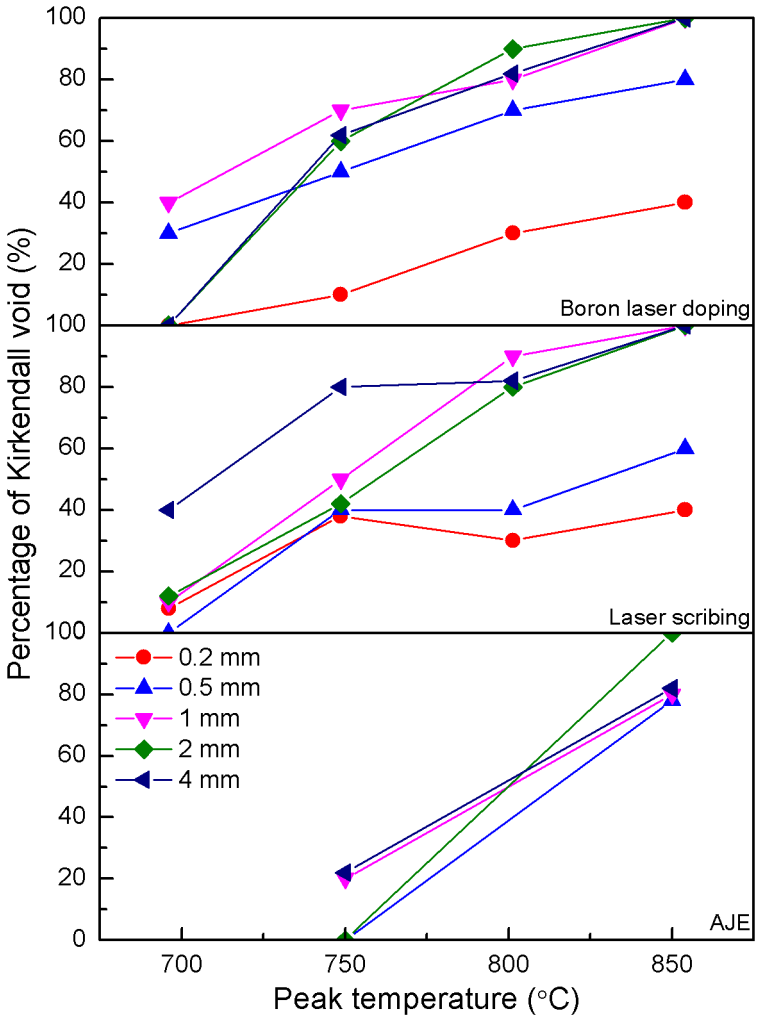

Figure 3-16 Kirkendall void formation in linear LBSF regions patterned by boron laser doping; laser scribing ; and AJE patterning with varied line spacing and peak temperatures.

3.3.3 Conclusions

The LBSF formation via boron laser doping, laser scribing and AJE patterned dielectrics have different properties with respect to the S_{limit}, thickness and uniformity, line widening and Kirkendall void formation. It was shown that closer spacing of the openings resulted in thicker LBSF regions and fewer Kirkendall voids for all patterning methods. However, line widening is more pronounced with more closely spaced contacts making it difficult to maintain low contact fractions unless the initial line widths are reduced.

Although the laser-patterning techniques cause crystal damage, the re-crystallised silicon region [see Figure 3-13(d)] is effectively dissolved by the alloying process. In theory this silicon dissolution and re-crystallisation should mitigate the damage induced during laser patterning. It suggests that the observed voltage penalties

for more closely-spaced laser line openings are due to the increased contact fraction given a defined laser line width, as opposed to laser induced damage. Despite the introduction of additional boron dopants during the laser doping process, aluminium alloying through the boron laser-doped lines did not result in thicker LBSF than laser scribing for the temperatures used in this study. On the contrary, boron laser doped openings resulted in a larger S_{limit}, which contributed to thinner LBSF and an extensive void formation at narrow line spacing. The only benefit that boron laser doping appears to present when compared with laser ablation is a slight reduction in line widening with firing.

Aerosol jet etching results in thicker LBSF regions than laser patterning. Moreover, it reduces percentage of Kirkendall voids and the percentage increase in line width upon firing. However, from the results presented here, it is difficult to separate the effects of the patterning method from the effects of the larger opening width of the AJE lines as compared to the laser-patterned lines. Further experiments where several laser passes are used to form wider laser-patterned lines may help clarify the contributions of the different effects. Finally, although AJE is a promising rear dielectric patterning approach for silicon solar cells, it has yet to demonstrate reliability, stability and capability to process wafers at industrial throughput. Although the AJE technique used in this work has demonstrated etched line width as narrow as 25 μm in 75 nm SiN_x [228], it is challenging to reproduce this result with 200 nm SiN_x. Consequently, for current silicon solar cell manufacturing, laser patterning remains the "tried and tested" approach.

3.4 Aerosol Jet Etching Patterned PERC Solar Cells

In these experiments, the cell structure was designed to be compatible with industrial mass production, with the rear dielectric layers being patterned by AJE. A PECVD AlO_x/SiN_x stack layer was deposited on the rear surface and the illuminated surface contacts were formed using a laser-doped selective-emitter and metallised by bias-assisted LIP of nickel and copper [229]. A thermally-evaporated (hereafter, evaporated) aluminium layer was used for better control of the metal layer thickness. Figure 3-17 illustrates the structure of the PERC cells fabricated in this work. This cell structure is also commonly-referred to as a PERL cell [42], due to the fact that it has aluminium-doped $p+$ region on the rear surface. However, as discussed in Section 2.1.3,

the term PERC cell is used in this thesis because the *p*+ regions were not formed by local boron diffusion.

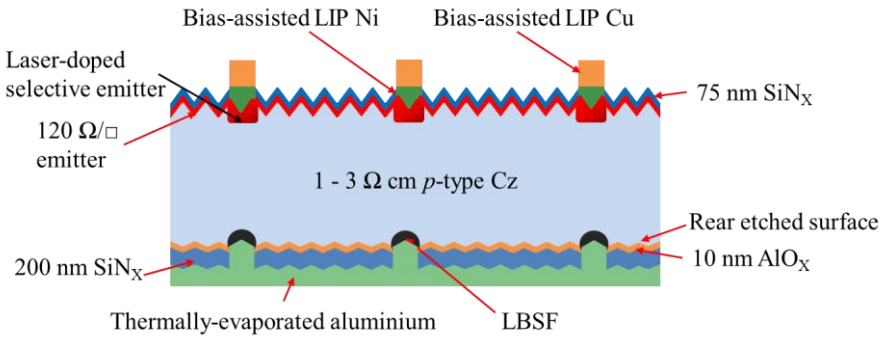

Figure 3-17 Schematic representation of the AJE-patterned PERC cells fabricated as part of this work.

3.4.1 Experimental

The PERC cells were fabricated on 40 mm × 40 mm *p*-type Cz, 1 - 3 Ω cm silicon wafer fragments. The fragments were laser cleaved from 156 mm × 156 mm wafers which were partially-processed by an industrial partner with alkaline-textured random pyramids and a $POCl_3$ diffused *n*-type emitter of 120 Ω/□ sheet resistance. A 75 nm SiN_x (n = 2.05) was deposited on the front surface by industrial PECVD as an ARC and a stack of AlO_x/SiN_x was deposited on the rear surface, with the two layers being 10 nm and 200 nm thick, respectively.

The AJE rear dielectric patterning was performed as described in Section 3.2.6. The line spacing was varied as 1, 1.5 and 2 mm. After patterning, the wafers were rinsed in DI water for 10 min to remove residual etchant and unreacted PAA, and then dried using nitrogen. A layer of 2 µm aluminium was evaporated on the patterned rear surface and fired to form LBSF regions in the openings in the dielectric layer. The advantage of evaporated over screen-printed aluminium is the precise control of the thickness and ability to apply thin layers (e.g., less than 10 µm). Thin aluminium layers are more readily saturated with silicon during the high temperature firing and hence the Kirkendall void formation may be able to be significantly suppressed even with 2 mm line pacing (see discussion in Section 3.3.2.5). Three different peak temperatures were used (750, 810 and 850 °C) based on the discussion in Section 3.3.2.

After rear metallisation, the illuminated surface was then spin-coated with 85% (w/w) H_3PO_4 prior to being laser doped using a 532 nm CW laser (Spectra-Physics)

with 15 W laser power and speed of 3 m s^{-1}, which corresponded to a sheet resistance of the laser-doped region of ~ 10 Ω/□ [172]. The front surface was then metallized by bias-assisted LIP of nickel and copper [229]. The process of the cell fabrication is shown in Figure 3-18. After laser edge isolation, the solar cells had an effective area of 6.25 cm^2 and they were characterised by 1-sun *I-V*, quantum efficiency (QE), Suns-V_{oc} and reflectance measurements. The cells were placed on a copper block during *I-V* measurement, which eliminated any R_s effect that may have resulted from the rear metal layer being thin. The local contact formation was analysed by SEM and EDS as described in Section 3.3.1.4.

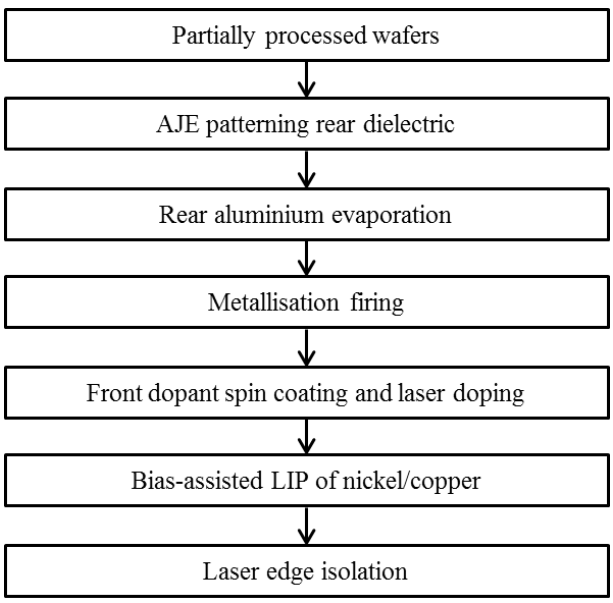

Figure 3-18 Process flow for the AJE-patterned PERC cells.

3.4.2 Results and Discussion

3.4.2.1 Local Contact Formation

Figure 3-19 (a) shows that at 850 °C uniform LBSF regions could be formed. The thickness of LBSF regions was reduced from 4 µm to less than 1 µm with the lower aluminium to silicon ratio in the localised area which is in good agreement with that observed with screen-printed aluminium [192]. However, despite the initial evaporated aluminium thickness being uniformly ~ 2 µm, the thickness of the metal layer varied significantly after high temperature firing. As shown in Figure 3-19 (c), after firing the aluminium thickness varied from 0.5 to 15 µm. A thin and discontinuous LBSF was formed where the capping aluminium layer was thin [see Figure 3-19 (b) and (d)]. The area where LBSF regions were not formed acted as high *SRV* sites, which limited the

cell V_{oc} and increased the R_s due to a direct contact between the metal and the lightly-doped silicon.

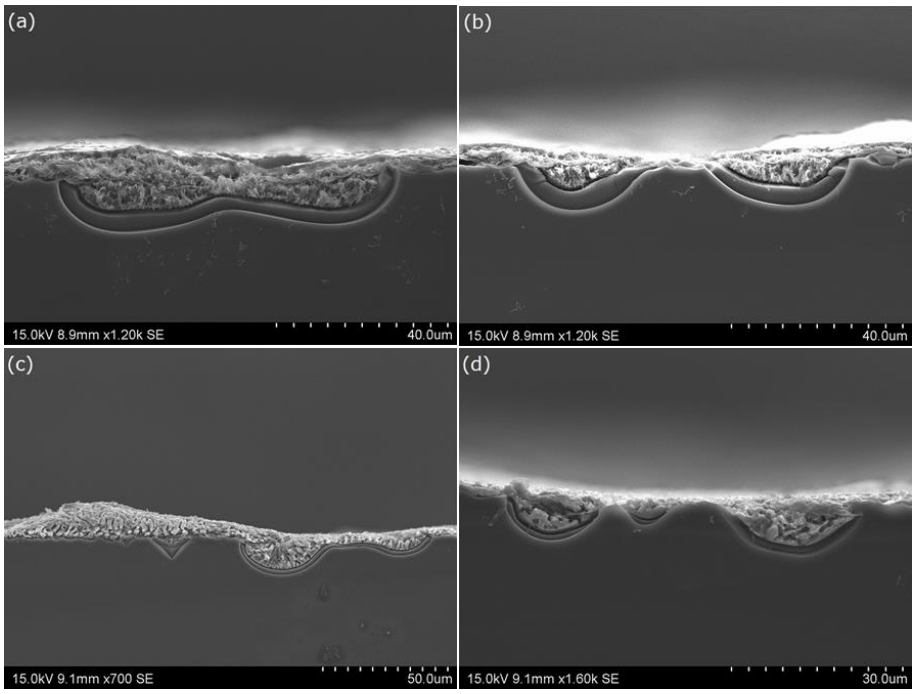

Figure 3-19 Cross sectional SEM images of LBSF regions for: (a) a homogeneous LBSF region; (b) and (d) poor LBSF due to aluminium redistribution on the surface; and (c) poor LBSF due to aluminium spiking through dielectric stack in the non-contact area.

It was also found the high temperature firing caused evaporated aluminium spiking through the dielectric in the non-patterned areas. Spiking was more common in areas where a thick layer of aluminium accumulated above the dielectric layer. This phenomenon can be attributed to the higher reactivity of the evaporated aluminium as compared to its screen-printed counterpart. Figure 3-20 shows an EDS mapping of the cross-sectional area of such a spike. These spikes were more prevalent at the higher firing temperatures.

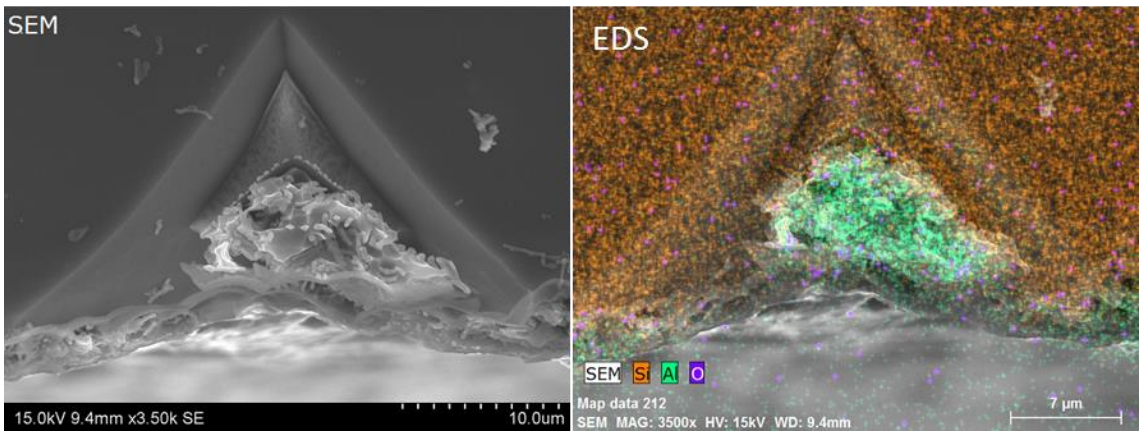

Figure 3-20 (a) A high magnification SEM cross-sectional image; and (b) an EDS mapping of a region where aluminium spiked through the rear dielectrics in a non-patterned area.

3.4.2.2 Cell Characterization

Figure 3-21 and Figure 3-22 show the V_{oc}, and J_{sc} of the fabricated cells graphed as a function of AJE-patterned line spacing. For cells fired at 750 and 810 °C, an increasing trend in V_{oc} was observed with the increased line spacing from 1 to 2 mm. This was attributed to the reduced contact fraction from 7% to 3.5%, which served to reduce the effective rear *SRV*. The J_{sc} followed the same trend as V_{oc} because the reduced contact fraction increased the internal reflectance of the rear surface of the cell. Also, the additional recombination from having more rear fingers with small line spacing can also reduce J_{sc}. Interestingly, the J_{sc} of cells fired at 810 °C were consistently higher than those fired at 750 °C, implying thicker LBSF and eutectic regions were formed at the higher temperature. This was because the eutectic region was reported to increase the cell internal reflectivity of the aluminium BSF cells [196]. However, at 850 °C, the V_{oc} and J_{sc} do not show any dependence on the line spacing. This is most likely due to aluminium spiking and redistribution, which were more prevalent at higher firing temperatures.

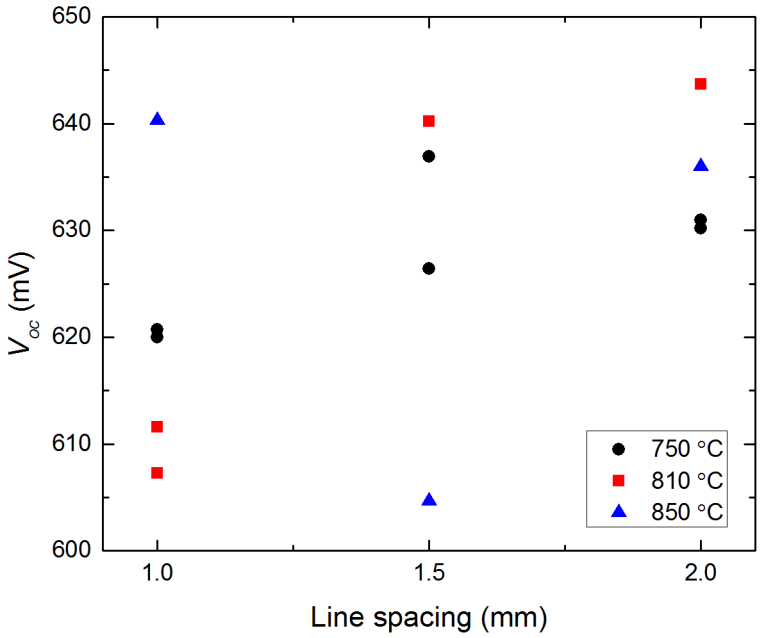

Figure 3-21 Open circuit voltage of cells with 1, 1.5 and 2 mm AJE-patterned line spacing.

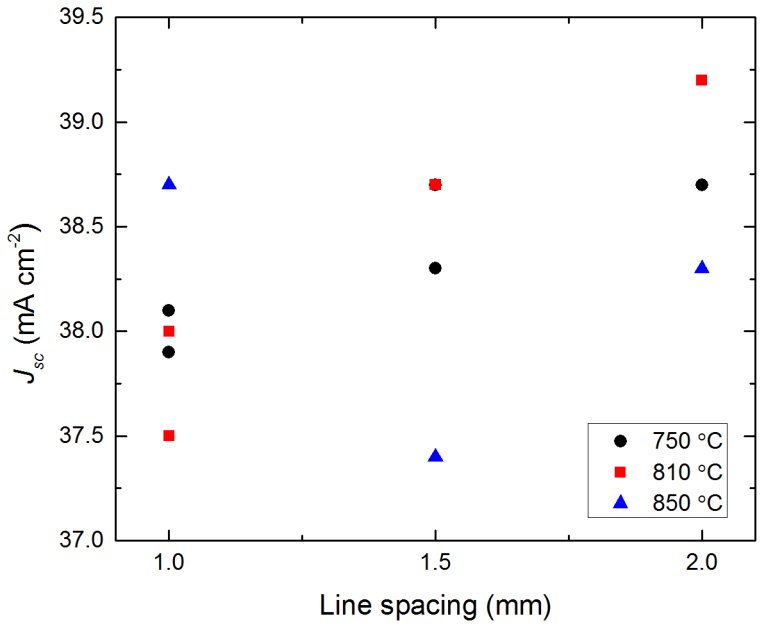

Figure 3-22 Short circuit current density of cells with 1, 1.5 and 2 mm AJE-patterned line spacing.

The cell *FF* and pseudo-*FF* (*pFF*, determined by Suns-V_{oc}) are graphed as a function of peak temperature in Figure 3-23. The difference between the *pFF* and *FF* was reduced with increased peak temperature. This can be attributed to the reduced R_c and hence R_s, which is primarily due to the increased LBSF thickness and the uniformity at higher firing temperatures. To validate this argument, the R_s was estimated by comparing the 1-sun light and dark *I-V* curves [230]. Figure 3-24 shows that the R_s

values are all significantly higher than values of 0.6 Ω cm^2 reported for full-area aluminium-alloyed cells [231] and decrease with higher firing temperatures which is in agreement with the previously-drawn conclusion.

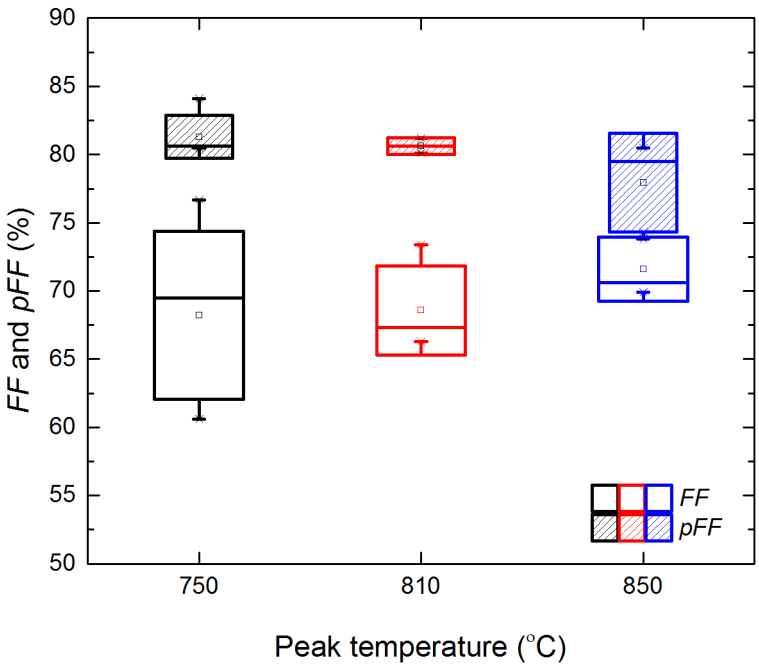

Figure 3-23 Fill factor and *pFF* of cells graphed as a function of peak firing temperature. Each box represents the mean and standard derivation of five cells.

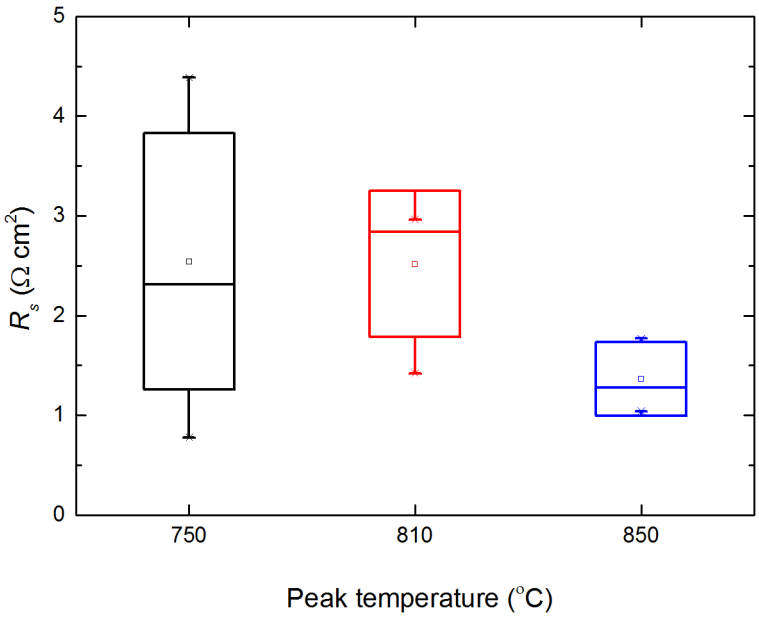

Figure 3-24 Series resistance of cells metallized at750, 810 and 850 °C, respectively. Each box represents the mean and standard derivation of five cells.

The most efficient AJE-patterned PERC cell was fired at 810 °C with 2 mm line spacing. Table 3-3 details the current density-voltage (*J-V*) data, *FF* and R_s for that cell. These results are compared to two reference cells: (i) 'Laser-patterned PERC' (a PERC cell with a boron laser-doped rear surface with metallised using screen-printed aluminium rear contacts and phosphorus laser-doped front surface with LIP nickel/copper front contact); and (ii) 'SP Al-BSF' (a standard screen-printed cell with full-area aluminium BSF and silver grids on the front). The light *J-V* curve and local ideality factor (*m*) curve for the most efficient AJE-patterned cell are shown in Figure 3-25.

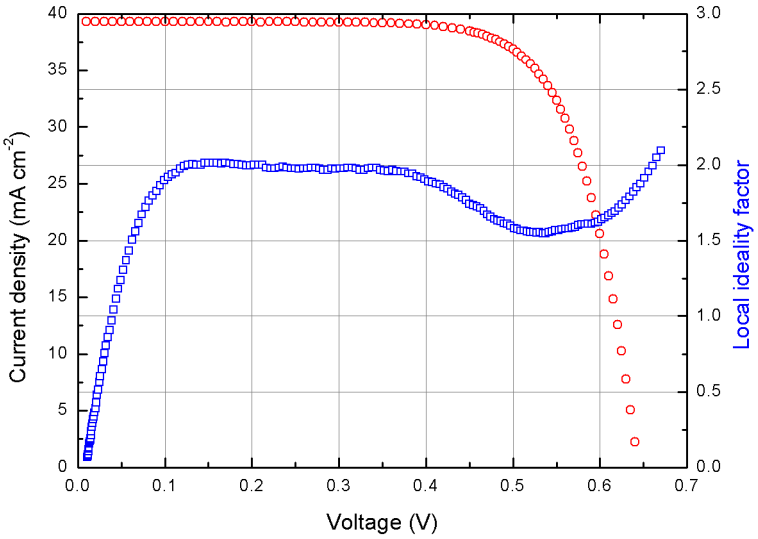

Figure 3-25 Light *J-V* and *m-V* curve of the most efficient AJE-patterned PERC cell.

As shown in Table 3-3, the V_{oc} and J_{sc} of the AJE-patterned cell are 18 mV and 1.9 mA cm^{-2} higher than the SP Al-BSF cell, due to the improved rear surface passivation and the increased internal reflectance at the rear surface. However, the *FF* of the AJE-patterned cell was 5.4%$_{abs}$ lower than the screen-printed reference cell, which is attributed to the increased R_s of the former cell that would have had contributions from the current-crowding at local contact regions on the rear surface [227] and R_c (due to non-uniform LBSF regions). Although the non-uniform thickness of the thin aluminium layer on the rear surface would have increased resistance in the rear metal electrode and hence the R_s, the temperature-controlled copper block used in the *I-V* measurement mitigated these resistive effects. The high R_s value of the AJE-patterned cell limited the increase in efficiency over the 'SP Al-BSF' cell to 0.2%$_{abs}$. The high R_s was evidenced as the upward bending of the *m-V* curve at voltages larger than the maximum power point voltage (V_{mp}) in Figure 3-25. Moreover, the

'bump' in the *m*-*V* curve in the voltage range of 0.1 - 0.4 V showed an *m* equals to 2 diode character [232], which indicated that edge recombination may be another significant source of reduction in *FF*. The *FF* of cells with *m* equals to 2 recombination decreases with higher V_{oc}, therefore the degradation in *FF* is more pronounced in the AJE-patterned cell which has higher V_{oc} compared to the SP Al-BSF cell.

Table 3-3 Summary of *J*-*V* characterization of the most efficient AJE-patterned PERC cell. Results are compared to a laser-patterned PERC cell and a screen-printed cell as references.

	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF* (%)	R_s (Ω cm^2)	Eff (%)
AJE-patterned PERC	644	39.2	73.4	1.42	18.5
Laser-patterned PERC*	656	40.2	75.7	0.68	20.0
SP Al-BSF**	626	37.3	78.8	0.60	18.3

*Laser-patterned PERC: a double-side laser-doped PERC cell using PECVD AlO_x/SiN_x rear surface passivation, laser doping and LIP nickel/copper front contact and screen printed aluminium rear contact [231].

**SP Al-BSF: a standard screen-printed cell with full-area aluminium BSF and silver grids on the front surface.

The V_{oc} of the AJE-patterned cell was 12 mV lower than that measured for the laser-patterned PERC cell. This was partly due to the larger rear surface contact fraction of 3.5% of the AJE-patterned cell as compared to ~ 1% of the laser-patterned cell. However a more significant problem was that the thermally-induced redistribution of the evaporated aluminium layer of the AJE-patterned cell during firing was shown to result in inhomogeneous LBSF regions, which would have increased the contact recombination and hence limited the cell voltage. Figure 3-26 shows the comparison of the internal quantum efficiency (*IQE*) and reflectance of the AJE, laser-patterned PERC cells and the SP Al-BSF cell. The PERC cells demonstrate improved blue and red responses compared to SP Al-BSF cell due to the use of a selective-emitter and rear surface passivation. Although the *IQE* curves of the AJE-patterned and laser-patterned PERC cells are similar in the range of 400 to 900 nm, the *IQE* of the AJE-patterned cell is reduced at wavelengths greater than 900 nm. The reflectance was also ~ 10% lower for AJE-patterned cell at 1200 nm. The reduced *IQE* in this range is attributed to a higher rear *SRV* caused by the larger contact fraction and non-ideal LBSF as discussed previously. Consequently, it was concluded that the contact fraction of the AJE-patterned cells needed to be reduced by patterning narrower lines and the thickness

of the evaporated aluminium needed to be increased to mitigate the LBSF uniformity issues arising from the non-uniform aluminium thickness.

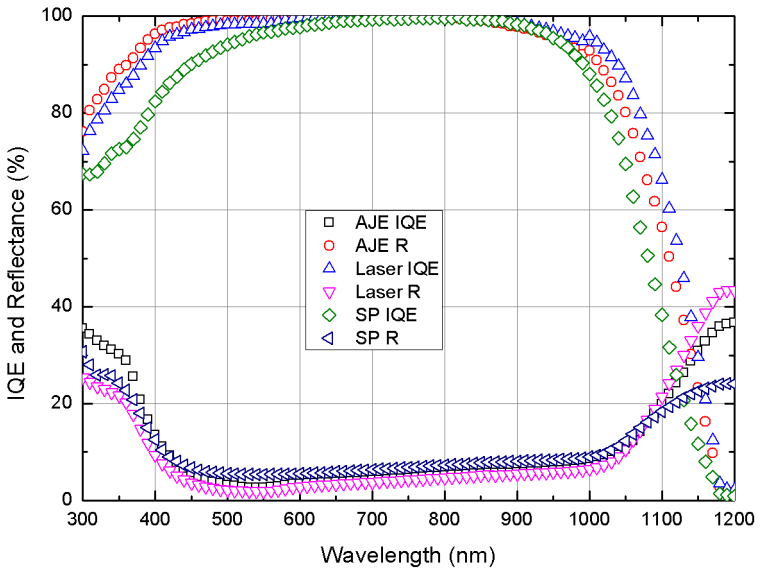

Figure 3-26 Internal quantum efficiency and reflectance of the most efficient AJE patterned PERC cell, laser-patterned PERC cell and the SP Al-BSF cell.

3.4.3 Conclusions

This section reported on the fabrication of AJE-patterned PERC cells featuring an AlO_x/SiN_x passivated rear surface; high-temperature metallised evaporated aluminium; and a laser-doped selective-emitter with bias-assisted LIP nickel/copper contacts. The highest fabricated cell efficiency was 18.5%. Although this was $0.2\%_{abs}$ higher than the efficiency of a screen-printed reference cell with a full-area BSF, it was $1.5\%_{abs}$ lower than a laser-patterned PERC cell. The AJE-patterned cell was limited by a low *FF* of 73.4% which was attributed to a high R_s arising from non-uniform and, in some cases, discontinuous LBSF formation due to the non-uniform aluminium thickness after high temperature firing. These LBSF deficiencies also impacted the V_{oc} of the most efficient AJE–patterned cell which was limited to 644 mV, 12 mV lower than the laser-patterned PERC cell.

A key finding of these experiments was that, although thinner aluminium layers may hold the promise of controlling the spreading of silicon in the aluminium layer on firing, the molten aluminium can move on the wafer surface resulting in non-uniform LBSF formation. This can limit both the *FF* (through high R_s) and the V_{oc} (through increased SRV). Furthermore, where thicker aluminium regions occurred over

non-patterned regions, the aluminium was observed to spike through the dielectric layer. This problem further impacted the V_{oc} as the aluminium that penetrated the dielectric was not shielded from minority carriers. Future experiments should use thicker aluminium layers to improve the uniformity of the LBSF regions. If screen-printed aluminium is used, then the thickness of the aluminium paste should be controlled to 15- 20 μm to reduce Kirkendall void formation.

For the AJE-patterned PERC cells the problems associated with the thin aluminium layer and spiking were further exacerbated by the larger contact fraction of 3.5% compared to 1% for the laser-patterned PERC cells. This was a direct consequence of the wider lines that resulted with AJE. If advantages are to be achieved with AJE-patterning over laser patterning, then thinner etched line widths will be required in order to reduce the metal contact fraction without significantly increasing the line spacing and hence current crowding.

3.5 Chapter Conclusions

Local BSF formation through AJE-patterned line openings in a 200 nm SiO_2/SiN_x dielectric stacks was investigated in this chapter. A robust AJE patterning process was developed to form line openings in 200 nm thick dielectric layers and AJE-patterned PERC solar cells were fabricated, demonstrating a highest cell efficiency of 18.5%.

The dependence of the etching completeness and uniformity of the 200 nm SiO_2/SiN_x dielectric stacks on the AJE parameters was studied by using a range of printing speeds and the number of printed layers. Higher speeds with a larger number of layers yielded similar etched line widths to lower speeds with smaller number of layers. Increased platen temperatures were found to effectively reduce the etched line width, however platen temperatures exceeding 60 °C resulted in incomplete etching due to excessive evaporation of water. The optimised tip-to-substrate distance which resulted in a focused aerosol beam increased with increasing deposition tip size. Smaller tip sizes resulted in narrower line widths for a given tip-to-substrate distance. A 100 μm deposition tip with a 2 mm tip-to-substrate distance was found to provide reliable etching of lines of width 60 - 70 μm.

The influence of the different dielectric patterning processes on the local contact formation was investigated. Aerosol jet etching does not introduce crystal defects in the silicon, therefore the S_{limit} was reduced in comparison to laser-patterning, where crystal defects in the recrystallised silicon can enhance dissolution and hence result in increased S_{limit}. Reducing the S_{limit} is advantageous in forming thick and uniform LBSF regions, because the aluminium above the contact openings is more easily saturated. Consequently, patterning by AJE resulted in 2 - 3 µm thicker LBSF regions than laser-patterned line contacts. Reduced dissolution of silicon also reduced the percentage line widening observed for AJE-patterned lines. However, the current limitation of AJE is the difficulty of etching narrower lines (e.g., 20 - 30 µm) in 200 nm SiO_2/SiN_x thick dielectric stacks. The AJE process needs to be further optimised by fine tuning parameters, such as the thickness of the PAA layer and the aerosol flow rates, or perhaps using geometric confinement [216].

Evaporated aluminium was used for the AJE-patterned PERC cells, in preference to screen-printed aluminium, because its precise thickness control and hence easier saturation of aluminium with silicon and reduced Kirkendall void formation. However, the thin aluminium layer redistributed during high temperature firing causing non-uniform LBSF which impacted both the R_s (and hence FF) and the V_{oc} of the cell. Furthermore, evaporated aluminium spiked through the dielectric layer in the non-patterned areas suggesting it is more reactive than the screen-printed aluminium pastes. The lower V_{oc} was attributed to the non-uniform LBSF formation and the higher contact fraction due to the wider etched line widths of the AJE lines as compared to the laser-patterned lines. It was concluded that thicker evaporated aluminium layers than 2 µm were required for uniform LBSF formation. Finally, the AJE-patterned line width needs to be reduced to the range of 20 - 30 µm to be competitive to laser patterning techniques.

Chapter 4 Inkjet Patterning Anodic Aluminium Oxide and Rear Local Contact Formation

It was concluded in Chapter 3 that chemical patterning would only be viable alternative to laser-patterning if 20 - 30 µm patterning resolution was possible. The aim of this chapter was therefore to explore whether the porous nature of AAO could be used to achieve reliable, cost-effective dielectric patterning without process-induced damage. The chapter reports on the development of a novel inkjet patterning technique for AAO layers. Well-defined arrays of point openings with diameters as small as 20 µm in 600 nm AAO layers are demonstrated. Furthermore, it is shown that LBSF regions with thickness up to 7 µm can be formed through these point openings. This inkjet patterning technique is an improvement from 'direct etching', where an inactive etchant needs to be applied to the substrate surface before the patterning process [185]. In contrast, this technique simplifies the process by directly printing active etchant to the localised area, where etching is required. The developed process is free of HF and hence increases the process safety.

4.1 Introduction

Most reported rear local contact solar cells have employed laser ablation [146, 233-235], laser doping [21, 174, 236, 237] or the use of etching pastes [212] to pattern a dielectric layer before the aluminium alloying process. However, few silicon solar cell manufacturing companies have committed to volume production of these cells, thus raising questions about the ability to pattern the dielectric layers in a reliable and cost-effective way at high throughput. Furthermore, the continued reliance on screen printing and its associated issues of wafer bowing and high paste costs limit the adoption of these local contacting methods for use with emerging thin silicon technologies [238]. Anodic aluminium oxide is a potentially low-cost dielectric which may also provide a valuable template for novel light trapping structures for thin silicon cells in the future [239, 240]. The layers have been shown to enhance minority carrier

lifetimes of phosphorus–diffused commercial grade *p*-type Cz wafers when formed over an intervening thermal SiO_2 or SiN_x [241-243]. In addition, the rear local contact formation through AAO has been investigated in terms of self-patterned contacting [206] or laser scribing using AAO as a dopant source [244]. However, a convincing case for the adoption of AAO in mass production remains outstanding with problems of residual aluminium and patternability needing to be address, as discussed in Section 2.4.2.

The idea of chemical patterning AAO layer for rear local contact formation is evaluated in this chapter. Chemical patterning techniques generally fall into two categories: indirect and direct etching, as illustrated in Figure 4-1. A review of these techniques can be found in Section 2.3.3.2. Direct etching is simpler. It delivers etchant on demand to local areas where patterning is required.

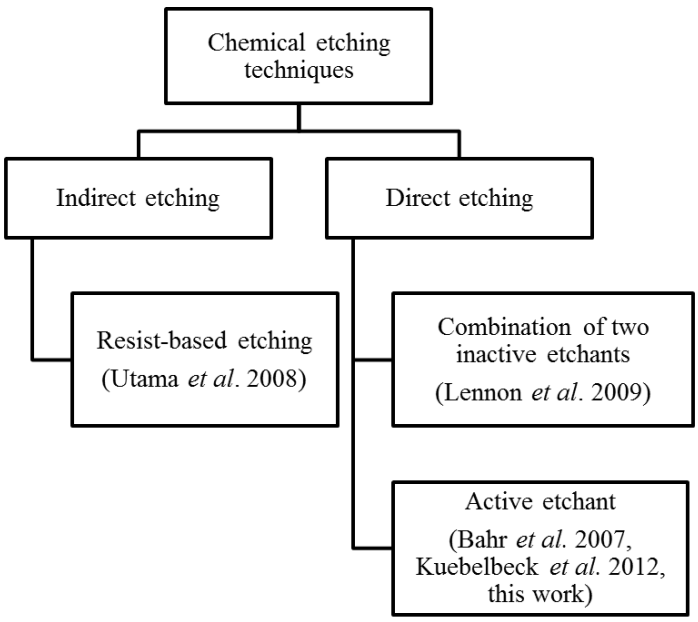

Figure 4-1 Category of chemical etching techniques. The inkjet patterning technique developed in this work is direct etching with one active etchant.

The inkjet patterning technique developed in this chapter takes the approach of delivering an active etchant to the surface. It satisfies the following constraints: (i) the active etchant is available to etch the targeted dielectric at a high etch rate; (ii) the etchant can be reliably deposited and is non-hazardous at the concentration and temperature used in the deposition process; (iii) the products of etching are water soluble and can be effectively removed from the etched surface, or alternatively the removal step can be avoided leaving the product as part of the cell; and (iv) a high

patterning resolution is achievable. Inkjet printing is used for material deposition in these experiments.

This chapter begins with a description of the inkjet patterning process development in terms of the determination of inkjet printer jetting conditions, etchant selection and effect of substrate in the patterning process. The critical parameters that affect the etching process are then investigated in detail. The chapter also reports on investigations into LBSF formation through openings in AAO layers formed by the inkjet-patterning process.

4.2 Printer, Etchant and Substrate

4.2.1 The Inkjet Printing System and Jetting Conditions

Droplet formation was first described by Rayleigh in 1878 [245]. He showed the instability of cylindrical films was established with a well-defined wavelength and this theory was named 'Rayleigh instability'. Since then, the core of the development of inkjet printing system was to control the 'Rayleigh instability'. In 1951, inkjet printing technology was commercialised [246]. It quickly changed the printing industry and became one of the dominating printing technologies in the field of graphics printing. Over the last decade, there has been increasing interest in inkjet printing of functional fluids, such as metal inks, conductive polymers, surface coating, proteins and nanoparticles, which highlights its application in a wide range of areas [183].

Inkjet printing has several distinct advantages compared to other material deposition techniques when applied to PV applications. First, the PV manufacturing industry is moving towards using thinner silicon substrates [8], and the non-contact nature of inkjet printing enables the processing of thinner wafers and printing on a wide range of surfaces. Second, patterning of dielectrics for PV applications requires high precision and reliability. The reported positional accuracy and repeatability of industrial inkjet printers has been reported to be as fine as ± 5 and ± 1 μm, respectively [247], which can readily enable patterning of dielectrics for PV applications with expected feature sizes between 20 - 30 μm. Third, inkjet printing can deliver etchant only to local areas where patterning is required. This is efficient in etchant usage and leaves negligible residue on an etched surface thus reducing operating cost and simplifying subsequent cleaning processes. Finally and most importantly, inkjet systems not only

require low upfront capital expenditure but also have lower operating cost than other deposition methods [183], which is critical if the process is to be adopted by the PV manufacturing.

Contemporary inkjet printers are classified as either continuous inkjet (CIJ) or drop-on-demand (DOD), depending on the printing mechanism (see Figure 4-2). The operation of CIJ depends on the continuous generation of an ink stream from a pressurised fluid reservoir. When the fluid stream reaches a certain critical length, surface tension breaks up the stream into individual droplets. The main advantages are very fast printing speed and less clogging; however it is limited by its high cost and relatively low drop precision in the application of material deposition.

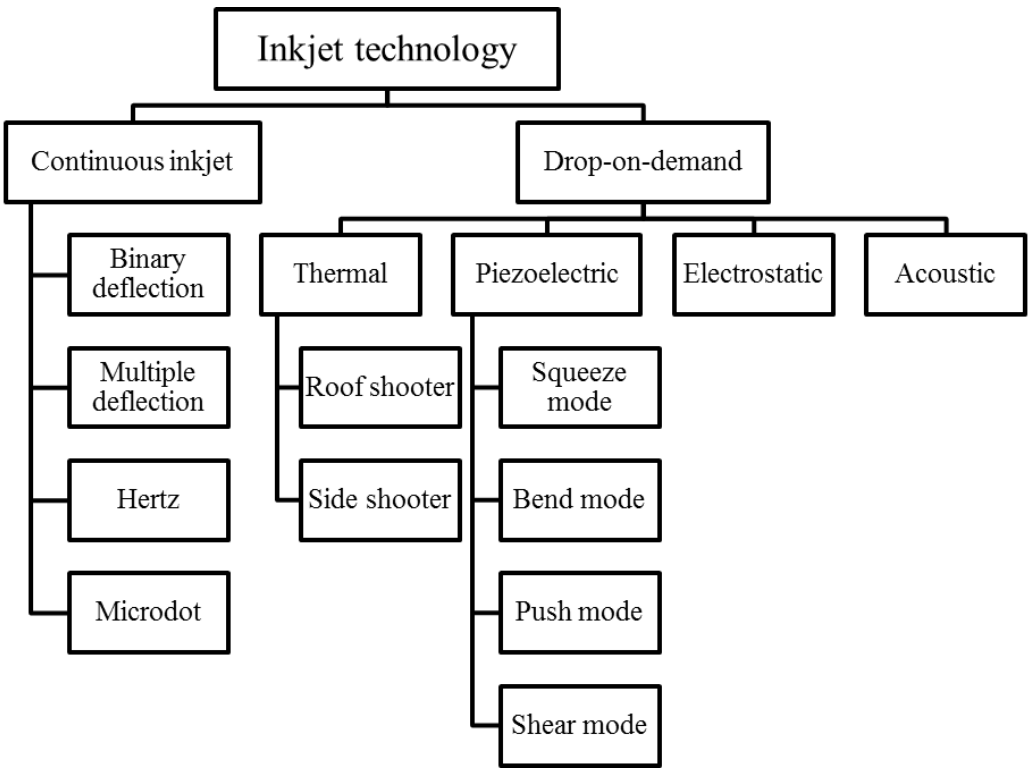

Figure 4-2 Category of inkjet technology (adopted from [248]). The inkjet printing system used in these experiments is bend mode, piezoelectric, DOD system.

The DOD system eliminates the need to have large volumes of pressurised printing material and a separate ink recycling system. The piezoelectric device is one of the most common DOD devices. In a piezolectric DOD system, each droplet is individually formed and ejected. In this system, a piezoelectric material is used to produce the energy necessary to eject a droplet. The process is purely mechanical, and therefore does not affect the chemistry of material printed. Although the use of a

piezoelectric material increases the complexity and cost of the devices, piezoelectric inkjet devices are the only choice for certain applications so far because they provide the widest range of fluid formulation possibilities as well as greater ability to control the droplet formation process through voltage waveform shaping. For these reasons, in these experiments, a piezoelectric DOD inkjet printer was used.

The inkjet printing system used is the Dimatix Materials Printer 2831 (DMP2831) designed by FUJIFILM Dimatix Inc. The cartridge used in DMP2831 is a silicon MEMS cartridge with a replaceable piezoelectric DOD printhead. The cartridge has 16 jetting nozzles and comes with two drop volumes of 1 pL (DMC-11601) and 10 pL (DMC-11610). A photo of the DMP2831 printer is shown in Figure 4-3.

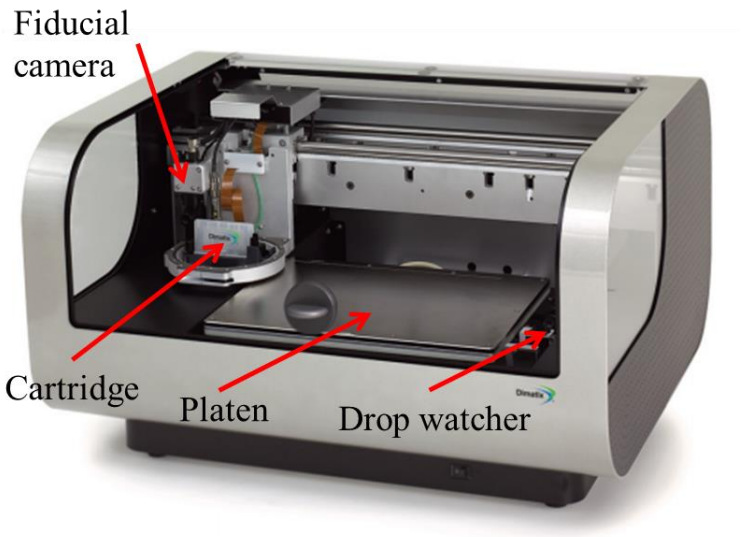

Figure 4-3 FUJIFILM Dimatix DMP2831 inkjet printer (adopted from [249]).

The printer features a flat platen with a printable area of 210 mm × 315 mm and an *x*-*y* stage. The platen, which moves in *x*-*axis*, serves as a substrate holder and its temperature is adjustable from RT to 60 °C with vacuum suction being available to maintain the substrate in place as the platen moves. The *y*-*axis* and *z*-*axis* movement are realised by the cartridge mounting system. The cartridge used has ink capacity up to 1.5 mL and is compatible with a large range of acidic and basic fluids. The printhead has 16 nozzles in a row spaced 254 µm apart, which allows simultaneous printing of multiple lines. It can also be heated to 70 °C for printing temperature sensitive fluids. A fiducial camera is attached to the cartridge mount, which allows substrate alignment using reference marks and inspection of printed patterns. Additionally, a drop watcher is

integrated with the printer to allow visual checking of droplet formation and other jetting properties.

Besides fluid properties, the jetting quality is largely determined by the following three parameters:

- Jetting voltage that represents the amplitude of the piezo driving pulse and determines the droplet volume and the velocity at which the droplet is ejected.
- Jetting frequency that represents number of cycles of the piezo driving pulse and controls how fast the jetting cycle is repeated.
- Jetting waveform that represents the shape and width of the piezo driving pulse. Slew rate and duration of each segment in the waveform can be adjusted to achieve the best jetting quality [183].

In the experiments reported in this thesis, it was critical to deposit etchant with high accuracy and repeatability when multiple layers were printed. Since the drop placement accuracy of the DMP2831 printer is reported to be ± 25 μm [250], only a single nozzle was used for each printing process to minimise alignment problems. Jetting voltage usually has the most impact in determining the droplet formation. It was varied between 11.2-12.8 V in order to print 50% (w/v) H_3PO_4 (which will be discussed in the next section). The optimised jetting frequency of 5 kHz and waveform shown in Figure 4-4 were reported by Utama [183] when printing the same etchant with DMP2831 printer, and therefore these conditions were used for experiments reported in this chapter.

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Figure 4-4 Jetting waveform used to jet 50% (w/v) H_3PO_4 in the DMP2831 inkjet printer (adapted from [183]).

The platen temperature during patterning was varied between 30 to 60 °C to ascertain the effect of substrate temperature on etching. There is a trade-off in selecting platen temperature because the decreased platen temperature decreases surface energy, therefore reduces the chance of surface wetting and achieves finer patterning resolution. On the other hand, however, lower temperature limits the etch rate and increases

process time. The optimised etching temperature was determined to be 60 °C, which will be discussed in Section 4.3.2. The printhead temperature was set to 30 °C to minimise the temperature fluctuation induced by heating from platen.

4.2.2 Etchant

The pore diameter and barrier layer thickness of AAO layer can be altered by subsequent processes when used as a template for growth of nano-structures. The AAO layer is amorphous alumina. It comprises an amphoteric oxide which reacts both with acid and alkali. Therefore, a relatively wide range of chemicals are capable to be etchant for the inkjet patterning process. The equations for the etching processes with acid and alkali are expressed by the following reactions [251]:

$$6H^{+}\,(aq) + Al_2O_3 \rightarrow 2Al^{3+}\,(aq) + 3H_2O \qquad (4.1)$$

$$2OH^{-}\,(aq) + Al_2O_3 \rightarrow 2AlO_2^{-}\,(aq) + H_2O \qquad (4.2)$$

In nanofabrication, chemicals such as NaOH (and other hydroxides), H_3PO_4, or a mixture of H_3PO_4 and H_2CrO_4 [251] are typically used for widening the pores and etch barrier layers [252], due to their ability to etch the AAO layer. However these processes are usually performed by immersed etching. When these etchants are delivered by an inkjet printer, its impact to the cell process by the drop-wise delivery of the etchant and the compatibility of the printhead must be evaluated.

4.2.2.1 Impact to Solar Cell Processing

A basic rule of process development for non-disruptive technology integration is that any alternative or extra process introduced must have minimum impact on the subsequent processes. Although having a much higher etch rate than acidic etchants, alkaline etchants such as NaOH contain large concentration of sodium ions which can be driven into bulk silicon during metallisation firing and hence detrimental to solar cell performance if not thoroughly removed by subsequent cleaning. Consequent cleaning processes, such as RCA 2 (laboratory) or HF/HCl (industry), should be performed after alkaline etching, which increases the complexity and cost of the process.

Hu *et al.* studied the wet chemical etching of AAO at RT with both H_3PO_4, NaOH and mixtures of 6% (w/w) H_3PO_4 and 1.8% (w/w) H_2CrO_4 solutions [251] They showed that etch rate increased with an increasing concentration of H_3PO_4, with 10% (w/w) H_3PO_4 resulting in the highest etch rate in the range of concentration investigated (see Figure 4-5).

Moreover, the residue from acidic etchants does not contaminate wafers and it can be readily removed by rinsing in DI water, therefore H_3PO_4 was the selected as a preferred etchant for inkjet patterning of AAO.

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Figure 4-5 Etch rate presented as percentage mass loss with respect to etching time of AAO layer in H_3PO_4 solutions (adapted from [251]).

4.2.2.2 Etchant Compatibility with the Inkjet Printer

Another constraint is the etchant cannot chemically react with any part of the fluid reservoir of the cartridge or the printhead. In addition, the fluid properties of the etchant should be within the range of optimum jetting conditions for the inkjet printer. Table 4-1 lists the optimum jetting conditions for the DMP2831 printer and compares these values with the properties of two concentrations of H_3PO_4 [183].

Table 4-1 Properties of 85% and 50% (w/v) H_3PO_4 and the desired properties for optimum jetting.

	H_3PO_4 (85%)	H_3PO_4 (50%)	Optimum Jetting
Molecular Weight	98	98	N/A
Particle Content Size (μm)	None	None	< 1.0
Viscosity @ 25 °C (cP)	47.0	8.0	8.0 – 14.0
Surface Tension @ 25 °C (mN m^{-1})	80.70	75.73	28.00 – 36.00
Density (g cm^{-3})	1.69	1.33	> 1.00
Boiling Point (°C)	158	>100	> 100

The research into the etch rates of AAO with H_3PO_4 complements research conducted by Utama in 2009 [183], which investigated the use of inkjet-printed H_3PO_4 as a phosphorus dopant source. It was found in Table 4-1 that the viscosity and surface tension of the 85% (w/w) H_3PO_4 stock solution were too high for optimum jetting, and so Utama investigated the jetting properties of different dilutions of the stock solution (see Figure 4-6). The closest optimal viscosity from these measurements was 50% (w/v) H_3PO_4, at which concentration the surface tension and density were 75.73 mN m^{-1} and 1.33 g cm^{-3}, respectively. Utama reported an optimal jetting voltage of 16 V, jetting pulse length of 8.768 μm and jetting frequency of 5 kHz, and also noted that the higher than optimal surface tension was advantageous as it prevented excessive droplet spreading on the surface,

which is critical if fine features are to be printed. Therefore 50% (w/v) H_3PO_4 was used in the experiments reported in this thesis for the etching of AAO using inkjet printing.

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Figure 4-6 Viscosity, surface tension and density of diluted H_3PO_4 solution as a function of its concentration [183].

4.2.3 Effects of Substrate

Inkjet printing is a non-contact process that involves the formation of droplets and, more importantly, the interaction between droplets and the substrate surface. The formation of droplets is determined by the type of printhead and properties of printed fluid, which are discussed in the previous sections. In this section, the surface properties of AAO and their interaction with deposited H_3PO_4 droplets are discussed. In general, interactions between a fluid and a substrate involve both physical and chemical aspects. In a physical sense, the interaction is largely determined by the physical properties of the substrate, such as: (i) surface energy and (ii) surface roughness. If chemical reactions are involved, the interaction will also be affected by the reaction kinetics and the time scale of chemical reaction. In the interaction of inkjet-printed H_3PO_4 and AAO, both physical and chemical interactions occur on the substrate surface.

4.2.3.1 Surface Energy

Surface energy quantifies the disruption of intermolecular bonds that occur when a surface is created. In the interaction of a droplet with the surface of a solid, a higher solid surface energy tends to attract molecules from the droplet resulting in increased wetting of the surface. Wetting of the substrate surface expands the interface of the liquid and solid, thus reduces the resolution of printing. In the case of inkjet patterning, however, a well-defined pattern with high resolution is required. Therefore a substrate with low surface energy is desired to reduce the spread of the deposited solution. The surface energy is also influenced by the temperature. High temperatures lead to increased surface energy and increased chance of surface wetting.

The contact angle is often used as a measure of the surface wettability. It is an angle measured through the liquid, where a liquid/air interface meets a solid surface and it quantifies the wettability of solid surface by a liquid via the Young's equation. In general, if the water contact angle, defined as the angle between the solid-liquid

interface and the liquid vapour interface, is smaller than 90°, the solid surface is considered as hydrophilic and if the water contact angle is larger than 90° the solid surface is hydrophobic. Materials with low surface energy result in high contact angles. To investigate the wettability of the AAO layer, the water contact angles of the AAO and PECVD SiN_x were measured.

Experimental

A batch of six (100)-oriented boron-doped *p*-type Cz, 1-3 ohm cm wafer fragments (40 mm × 40 mm) were etched in 25% (w/v) NaOH solution at 80 ± 2 °C for 10 min to remove any surface damage and result in a planarised surface. After removing the trance of sodium ions, the wafers went through a full RCA clean [217] and then dipped in 1% (w/v) HF until the wafer surface is 'pull dry'. Wafers were then thermally oxidised in a quartz tube furnace at 980 °C for 18 min to grow a 17 nm SiO_2 layer on both surfaces, which serves as a buffer layer during anodisation to increase the adhesion of the AAO layer. After thermal oxidation, a 75 nm thick SiN_x layer was deposited on three wafers by PECVD (AK400, Roth & Rou) to establish a reference and other three wafers were thermally evaporated with a 600 nm aluminium layer for anodisation.

The anodisation was performed in an electrochemical cell as shown in Figure 4-7. Wafers were processed one at a time, with each wafer being submersed in a 0.5 M H_2SO_4 and biased with a DC voltage via a conductive clip. A nickel plate was contacted to the negative terminal of the power supply, acting as cathode. A constant 25 V DC bias voltage (V_{bias}) was applied across the wafer and the counter electrode until the aluminium layer was fully anodised. Due to the dependence of conductive clips to apply bias voltage, this anodisation technique is referred to as 'clip anodisation' in order to distinguish it from the 'LIA' that will be introduced in Chapter 5.

After anodisation, the water contact angle on the AAO and SiNx surfaces was measured using a goniometer Model 190 (rame-hart).

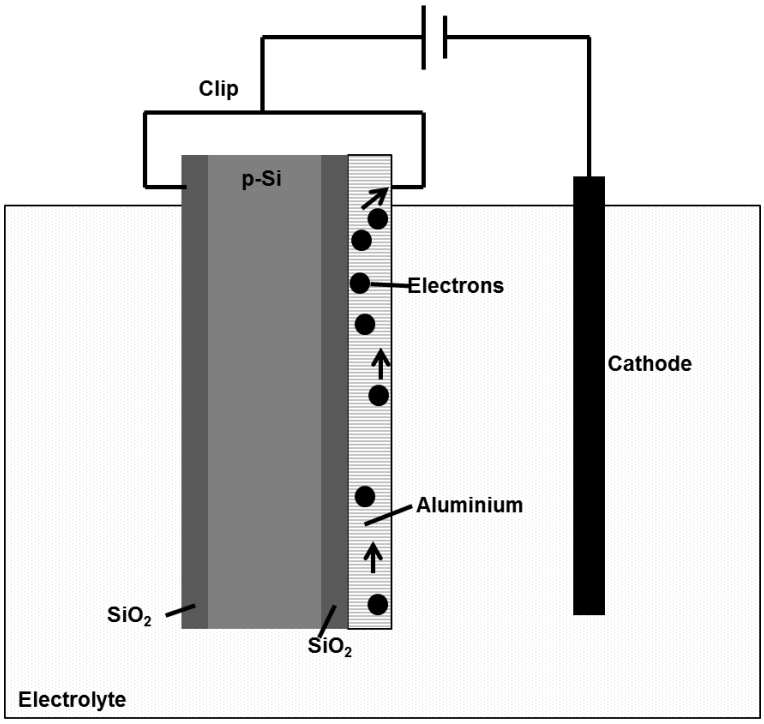


Figure 4-7 Clip anodisation apparatus.

Results and Discussion

The contact angle on AAO surface is 90° ± 2° compared to that on the SiN_x surface is 54° ± 2°. This result shows the AAO layer has a much lower surface energy than PECVD SiN_x, and therefore spread of deposited H_3PO_4 droplets on the AAO surface is expected to be reduced. Consequently, it was considered likely that well-defined and fine resolution patterning would be possible on AAO surfaces without any additional surface treatment.

4.2.3.2 Surface Roughness

The surface roughness will be discussed in two levels: the macro level and the micro level. In the macro level, the surface roughness is determined by topography of the silicon substrate surface. Topography is the description of surface shape and features, which may influence the interaction of a liquid and solid. In this study, the AAO layer was formed on three silicon substrates: (i) mechanically polished; (ii) chemically planarised; and (iii) alkaline-textured. For polished and planar substrates, the topography was only a second order effect as the surface was visually flat. For the textured substrates, however, the size of the 'pyramids' formed by alkaline texturing was in the range of 3 - 5 µm which is comparable to the size of a 1 pL droplet and was

hypothesised to affect the impaction and spreading of inkjet-printed droplets. This will be further discussed in Section 4.3.3.

At the micro level, especially on the planar and polished substrates, the roughness of the porous AAO surface plays a very important role in determining the wettability. The theory was explained by two main hypotheses attributed to Wenzel [253] and Cassie [254]. The Wenzel and Cassie models described two extremes of surface wetting. In the Wenzel model, the grooves or space between the protrusions is completely wetted with liquid. The surface contact area of liquid with solid is increased by surface roughness. In the Cassie model, however, the liquid is only in contact with the peaks of the rough surface, and air pockets exist between the liquid and roughened solid surface. Since the AAO layer surface is porous and the surface roughness is determined by the pore diameter, the spacing and the depth of pores, the wettability of AAO layer surface may vary with the anodisation conditions. Ran *et al.* [255] showed the wetting states on the AAO layer with pore diameter of 85 and 420 nm were likely to be described by Wenzel and Cassie model, respectively. They also showed the increased depth of pores from 0.8 to 9.2 μm changed the surface wetting from the Wenzel model to the Cassie model with pore diameter and spacing fixed at 260 ± 10 and 400 ± 18 nm, respectively. Figure 4-8 shows the transition of surface wetting condition with respect to the pore diameter and depth of the AAO layer. It is reasonable to conclude from Ran's work that the surface of a thin AAO layer with a smaller pore diameter to spacing ratio is likely to be wetted as described by the Wenzel model (i.e., the contact angle is smaller).

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 4-8 Water contact angle on the AAO layer as a function of the pore diameter and pore depth (reproduced from [255]).

In this thesis, aluminium films of 600 nm thickness were anodised in H_2SO_4 using a bias voltage up to 25 V which corresponded to a pore spacing of 52 ± 15 nm and diameter of 12 ± 2 nm [256]. This resulted in the pore diameter to spacing ratio of 0.23 ± 0.07. According to the trend illustrated in Figure 4-8, the AAO layer fabricated in this thesis has both small thickness and a low pore diameter to spacing ratio. Therefore it implies that the surface wetting of this layer is predominantly determined by the Wenzel model, in other words, the etchant is likely to fill up the pores, assisting the etching process.

In inkjet patterning, the wetting mechanism of Wenzel model is advantageous because etchant deposited on the AAO layer surface tends to repel the air from the pores and wet the majority of the surface including inner wall of the pores (see Figure 4-9). The increased wetting area of etchant on the AAO layer reduces the time required to etch through the film of a certain thickness.

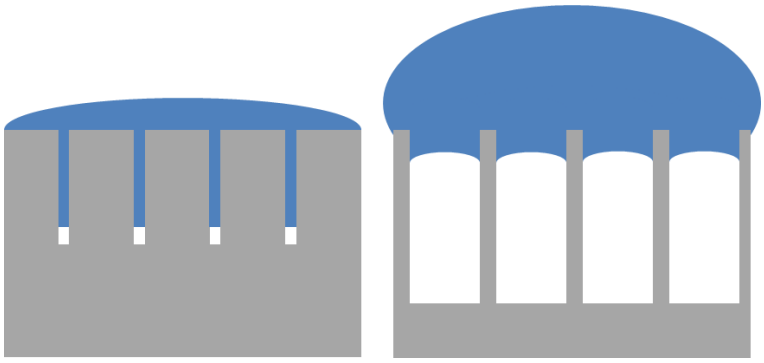


Figure 4-9 Schematic representative of water on the surface of AAO layer with small pore diameter to spacing ratio (left) and large pore diameter to spacing ratio (right). The left figure shows the case of the AAO layer used in these experiments.

4.2.3.3 Time Scale of Chemical Reaction

In a process where chemical reaction(s) are involved, the time scale of the reaction needs to be considered for a complete understanding of the deposition process. The etch rate of AAO by inkjet-printed 50% (w/v) H_3PO_4 was estimated to be 30 nm min^{-1} from the work of this thesis, thus the complete etching of a 600 nm thick AAO layer requires 20 min. However the time scale of the reaction has to be compared with the time scale of droplets spreading on impaction with the surface to determine the limiting factor of the final liquid and solid contact area. Dong *et al.* [257] studied the impaction of drops deposited by the DOD method on smooth solid substrates over a wide range of impaction speeds, surface contact angles and drop diameters. It was demonstrated the duration of drop impaction was varied from 10^{-4} to 10^{-2} s with the impaction speed and drop diameter similar to these experiments, which was a negligible short period of time compared to the time required for etching. Therefore, in the etching process studied in these experiments, it was assumed that droplet impaction was completed before the etching reaction commenced. So the final liquid and solid contact area was dominated by the impaction process.

4.2.4 Conclusions

The DOD inkjet system with a piezoelectric print head was used for the experiments reported in this chapter because of its compatibility to deposit a wide range of corrosive etchants and ability to accurately control the drop formation. Diluted 50% (w/v) H_3PO_4 was chosen as the active etchant because it effectively etches AAO and is eligible for optimum jetting in the DMP2831 inkjet printer. The surface property of the AAO layers prepared in these experiments is eligible for achieving high resolution patterning. It was concluded that the surface wetting was most accurately described by the Wenzel model, where the wetting area between the etchant and film is maximised by repelling air from the pores of the AAO layer. The pores with low diameter-to-spacing ratio limit the water contact angle on planar substrate to be 90° ± 2°. Finally, it was concluded that the size of etched features would primarily be determined by the impaction of droplet on the surface rather than the etching reaction.

4.3 Inkjet Patterning

In this section, an inkjet patterning technique is described. The effect of etchant volume, etching duration, etching temperature, and surface topography on the size and quality of etched features are discussed. Figure 4-10 shows the inkjet patterning process. Droplets of H_3PO_4 were deposited to localised areas on an AAO surface [Figure 4-10 (b)]. The low surface energy of the AAO reduces the spreading of the H_3PO_4 droplets. After printing, the substrate was left on a heated platen for a certain period of time until etching in the printed area was completed [Figure 4-10 (c)]. Finally, residue from the etching process was removed by DI water rinse, leaving a well-defined patterned AAO layer [Figure 4-10 (d)].

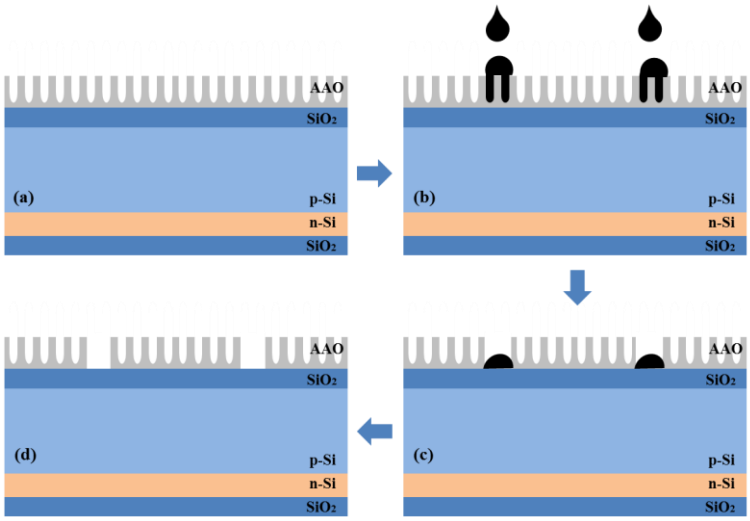


Figure 4-10 Schematic drawing of the patterning process by inkjet printing H_3PO_4 (not to scale).

4.3.1 Effect of Etchant Volume and Etching Duration

The volume of etchant and etching duration play an important role in determining the size and resolution of the etched features. This section contains a study of the effect of etchant volume in the measurement of number of printed layers and the total etching duration counted from jetting of the first droplet to the unload of wafer from the heated platen.

4.3.1.1 Experimental

The inkjet patterning experiments were performed using 40 mm × 40 mm wafer fragments of: (i) 240 µm thick polished 10 Ω cm *p*-type Cz wafer; and (ii) 200 µm thick alkaline-textured 1 - 3 Ω cm *p*-type Cz wafers. Half of the textured wafers underwent a 7 min saw damage etch in 25% (w/v) NaOH at 80 ± 2 °C to simulate a rear-etched planar surface. A 15 nm thermal SiO_2 layer was grown on both surfaces of all wafers. This layer acted as an effective barrier layer to prevent anodisation of the silicon substrate when the aluminium layer was fully anodised [127]. A 600 nm aluminium layer was then evaporated on one side of the wafers, followed by clip anodisation as described in Section 4.2.3.1.

A 50% (w/v) H_3PO_4 solution was inkjet-printed using a inkjet printer using a 1 pL ink cartridge. Printing was performed at 5 kHz, and the firing voltage was varied between 11.2-12.8 V. These settings were selected in order to maintain a drop velocity of 10 m s^{-1}, monitored using the printer's drop watcher application. A single nozzle was used for each printing process to improve the accuracy of alignment between multiple

printed layers. The platen temperature during printing was controlled at 60 °C and the cartridge temperature at 30 °C to mitigate the temperature variation of the ink during the printing. Following the printing, the wafers remained on the heated platen for 10, 30, 45 and 60 min to facilitate the etching process. Wafers were then rinsed in DI water and visually inspected. The etching process was characterised using optical microscopy, atomic force microscopy (AFM) and SEM. Etched point opening arrays were achieved by increasing the drop spacing applied to a pattern of lines. Larger drop spacing enables fast printing speeds over each printed line. In these experiments, the typical test pattern consisted of a 20 mm × 20 mm array of point openings with 250 μm spacing.

4.3.1.2 Results and Discussion

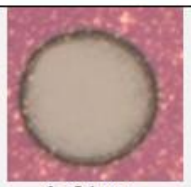
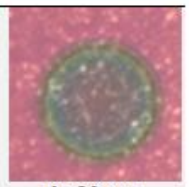
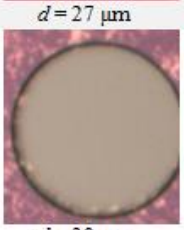
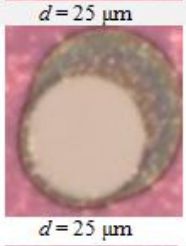
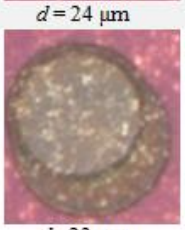
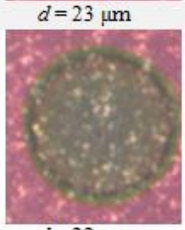
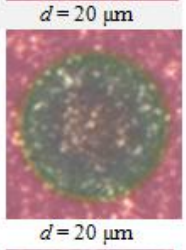
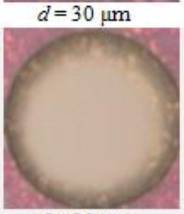
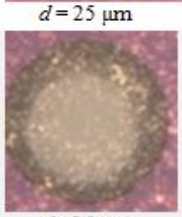
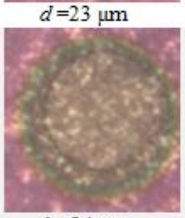
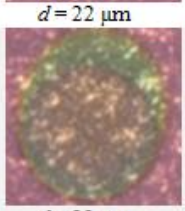
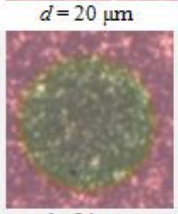
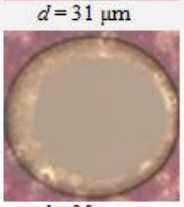
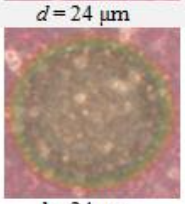
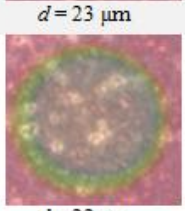
The amount of etchant deposited was directly related to the number of layers printed. To increase the etching duration, after printing the wafers were left on the 60 °C heated platen for 10, 30, 45 and 60 min. The etching duration was assumed to start when the first droplets were deposited and to end when the wafers were removed from the heated platen. After rinsing, the wafers were observed under an optical microscope to measure the point opening diameter and assess the depth, or extent, of etching.

Table 4-2 shows the relationship between the etched point opening diameter and the amount of AAO etched for a polished wafer surface. As fewer layers were printed, which corresponded to less etchant being deposited, the extent or depth of etching was reduced as evidenced by AAO remaining visible in the regions where etchant was deposited. Furthermore, as the number of layers decreased, the diameter of the point openings was reduced. This is because the etchant typically spreads as more layers are applied to the same location. The diameter of the point openings was also affected by the drop placement accuracy. Misaligned droplets increased the area being exposed to etchant and hence the opening diameter. Those misaligned droplets are clearly evident in the optical images from substrates etched for 45 mins in Table 4-2. Clearly good alignment between printed layers is important for the etching of small well-defined point openings. The reported drop placement repeatability for the DMP2831 is specified as ± 25 μm [249] which limits the minimum feature size to be 50 μm. In practice, however, the drop placement accuracy was much higher since point openings with diameter between 20 - 30 μm were reliably reproduced in the experiments.

Increased etching duration resulted in an increased depth of AAO etching for a given number of layers but did not appear to increase the etched point opening diameter.

Longer etching durations did not appear to increase the etched point opening diameter. This would suggest that the spreading of the etchant, which occurred as increased layers were printed, had a more significant effect on the diameter of the etched point openings than the time over which etching occurred.

Table 4-2 Effect of etching duration on the depth of etching and etched -point opening diameter (d), for different numbers of printed layers of etchant. The platen temperature was set to 60 °C for all experiments. Etched-point opening diameters represent the mean of three individual measurements.

Etching Duration	8 Layers	6 Layers	4 Layers	2 Layers	1 Layer
t = 60 min	 d = 27 µm	 d = 25 µm	 d = 24 µm	 d = 23 µm	 d = 20 µm
t = 45 min	 d = 30 µm	 d = 25 µm	 d =23 µm	 d = 22 µm	 d = 20 µm
t = 30 min	 d = 31 µm	 d =26 µm	 d = 24 µm	 d = 23 µm	 d = 21 µm
t = 10 min	 d = 30 µm	 d = 29 µm	 d = 24 µm	 d = 22 µm	

4.3.2 Effect of Etching Temperature

Higher temperatures usually have an accelerating effect on the etch rate. Given this effect, the temperature of the wafers during printing was varied to study the effect of temperature on the etch rate, as well as the quality of the etched patterns. This is to determine if the reliance on etch time and the volume of etchant can be reduced, the reduction can be offset by increasing the etching temperature.

4.3.2.1 Experimental

Williams showed that H_3PO_4 etches SiO_2 layers faster at temperatures of ~160 °C in a wet process [221]. Based on this fact, in initial experiments, substrates were heated in a pre-heated oven for 15 min at 160 °C directly following deposition of etchant, however only partial etching was observed in these experiments (see Figure 4-11). This presumably occurs because at 160 °C, the rate at which the water in the etchant evaporates is significantly faster resulting in a lower effective water concentration in the etchant. Inkjet printing is an etchant-limiting process, as during the process only small volumes of etchant (~ 8 pL) are deposited at the surface where the solution is prone to evaporation. The higher etch rate at high temperatures observed for immersion etching may not be valid for inkjet patterning, because the previous is less affected by water evaporation due to the near-infinite etchant supply at localised areas.

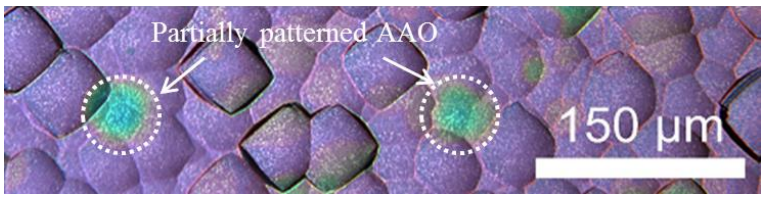


Figure 4-11 A 250 µm array printed on a planarised substrate with 8 layers of etchant. The wafer was heated in the pre-heated oven at 160 °C for 15 min after printing. The greenish points are showing partial etching of the AAO layer.

In subsequent experiments, the effect of temperature was ascertained by varying the etching temperature at 30, 60 and 75 °C and leaving substrates on the platen for different durations as described in Section 4.3.1.1. The much lower temperature range comparing to 160 °C was studied to avoid excessive evaporation of water. The effect of increased etching temperature was simulated by varying the platen temperature. For temperatures higher than 60 °C, due to limitations on further heating the printer platen, the wafer was printed on the platen at 60 °C, and then transferred to a hot plate heated at 75 °C to maintain the higher etching temperature. The actual wafer temperatures were measured by an infrared thermometer and are listed in Table 4-3.

Table 4-3 Set printer platen temperatures and corresponding wafer temperatures measured by infrared thermometer.

Platen Temperature (°C)	Sample Temperature (°C)
30	26
60	46
75	64

4.3.2.2 Results and Discussion

Optical microscope images of selected point openings from wafers etched at the different temperatures are shown in Table 4-4. It is clear that as the platen temperature was increased from 30 to 60 ºC, given the same etching duration and number of printed layers, the etching rate increased significantly and more of the AAO was etched in the point opening regions. According to the Arrhenius equation, the etch rate is,

$$k = Ae^{-\frac{E_a}{RT}} \tag{4.3}$$

where, k is the etching rate at absolute temperature T, A is a pre-exponential constant, E_a activation energy, and R universal gas constant. The amount of etched AAO (Q_{AAO}) can be determined by the following equation,

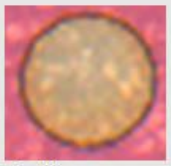
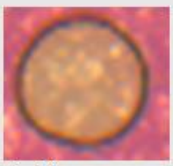
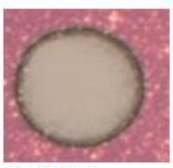
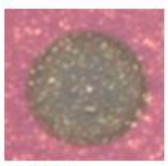
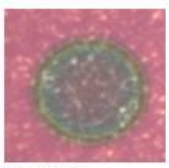
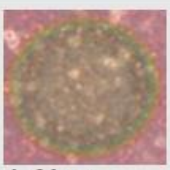
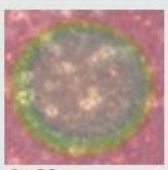
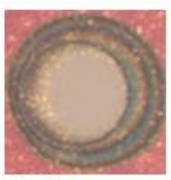
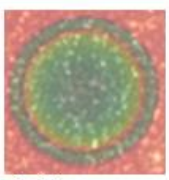
$$Q_{AAO} = kt \tag{4.4}$$

where, t is the etching time. The effect of temperature appeared to be more critical than that of etching time and suggests that higher platen temperatures can be used to offset the requirement for a longer etching duration.

However, there is a limit to how much the etching process can be accelerated through increased platen temperature. Increases in temperature above 60 ºC appeared to not increase the etching rate due to enhanced evaporation of water from the deposited H_3PO_4, indicating that water is necessary for the reaction. The presence of water is important in many etching reactions. Seidel *et al.* showed in the anisotropic etching of silicon in alkaline solutions, a decrease of the etch rate with the fourth power of the water concentration was observed for highly concentrated KOH solutions [218]. In the alkaline etching reaction, the four electrons that are injected into the conduction band due to formation of silicic acid [$Si(OH)_4$] react with water molecules close to the silicon surface evolving hydrogen gas.

Substrates etched at 75 °C exhibited ‘rings’ of graduated etching with the most-etched regions occurring in the centre. This etching pattern is consistent with water evaporating at the perimeter of the printed droplet and causing the circumference of the etched droplet to decrease as etching proceeds leaving partially etched regions at the perimeter of the area wetted by the deposited drops. The result is conical etch profiles in the AAO layer with a smaller central point opening diameter.

Table 4-4 Effect of platen temperature and the number of printed layers on the etched hole diameter (d) and the completeness of etching.

Platen Temperature	8 Layers	6 Layers	4 Layers	2 Layers	1 Layer
T= 30°C t = 60 min	 d = 33 µm	 d = 26 µm	 d = 24 µm		
T= 60°C t = 60 min	 d = 27 µm	 d = 25 µm	 d = 24 µm	 d = 23 µm	 d = 20 µm
T= 60°C t = 10 min	 d = 30 µm	 d = 29 µm	 d = 26 µm	 d = 22 µm	
T= 75°C t = 10 min		 d = 22 µm	 d = 22 µm	 d = 20 µm	 d = 22 µm

The appearance of clearly defined rings in the etched opening profile as the etch temperature increased was also noted by Lennon *et al.*, when inkjet patterning SiN_x layers with a formed HF solution was conducted [185]. In these experiments, the evaporation of the droplet caused a transient flow of the reactants to the perimeter of the wetted area. However, the etched profiles obtained with higher platen temperatures appear to graduate inwards, with the centre of the etched opening being the most etched, unlike the 'donut shaped' profile observed in Lennon *et al.*'s experiments, which became more prominent as the temperature increased. Further increases in platen temperature may produce similar 'donut-shaped' structures, however it is possible that the lateral flow of the etchant may be disrupted by the porous structure of the AAO layer. Therefore, rather than a single 'coffee-ring' structure or a donut profile being observed, a series of coffee rings forms as a result of the simultaneous processes of etchant being trapped in the porous layer as water evaporates from the edge inwards, creating a series of 'coffee ring' structures around the etched opening.

4.3.3 Effect of Surface Topography

The surface topography (e.g., polished, planar or textured) affected the way point openings were etched in AAO layers. Polished surfaces resulted in the smallest etched point openings, with diameters of 20 - 30 μm. In comparison, planarised surfaces required more layers of etchant to etch through the same thickness of AAO, which increased the diameter of the etched point openings. This observation is supported by the trends shown in Table 4-2 and Table 4-4. The etching on textured surfaces with random pyramids required the largest amount of etchant and longest etching duration. Figure 4-12 shows the patterned point openings in the AAO layer on three different wafer surfaces.

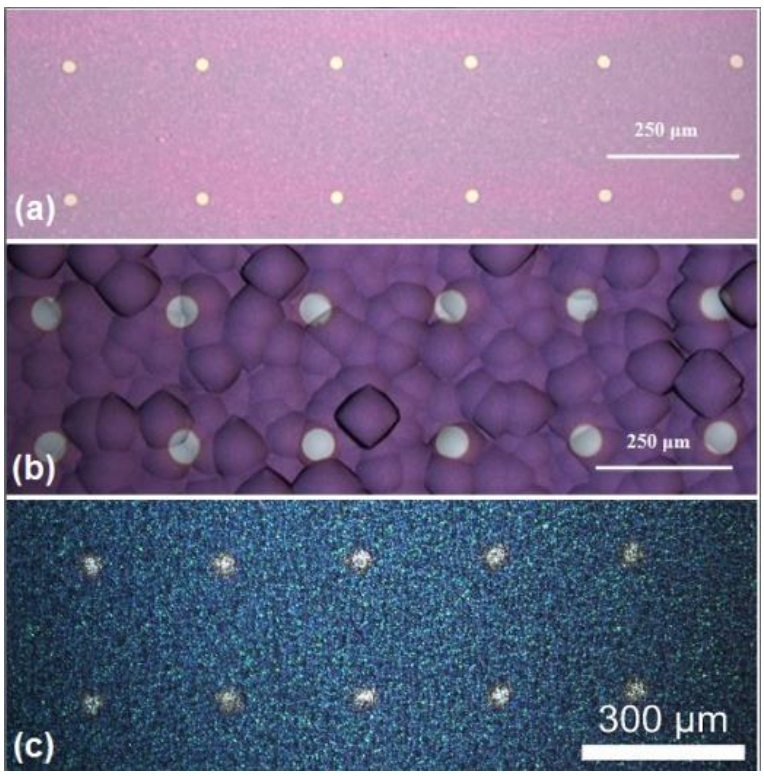


Figure 4-12 Array of point openings etched in an AAO layer formed on: (a) a polished wafer by depositing 6 layers of etchant; (b) a planar wafer by depositing 12 layers of etchant; and (c) a textured wafer by depositing 12 layers of etchant. The etchant in all cases was 50% (w/v) H_3PO_4, and it was deposited using a 1 pL cartridge of the DMP2831.

As the roughness of the surface increased, the uneven topography of the pyramids, which created troughs where etchant could pool, most likely disrupted the surface tension of the droplets on the wafer surface and therefore caused more spreading of etchant over the surface. The variations in the size of the pyramids, resulted from

different texturing processes adds further complexity to the patterning process. It is shown in Figure 4-13 that on another textured wafer, which had different sized pyramids, the required volume of etchant was doubled. Moreover, significant spreading was observed around the point openings. The etchant spreading reduced the amount of effective etchant per unit area, thus more layers of etchant were required to etch through the same thickness of AAO. Although the etching process is not as effective on alkaline-textured surfaces, this may not present a problem as a planarised surface typically results from rear etch tools frequently used in manufacturing. Furthermore, planarised surfaces enable improved surface passivation over an alkaline-textured surface. Consequently, the etching on planar surfaces was considered to be of most practical concern. The etching time and number of printed layers required to successfully etch point openings in a 600 nm thick AAO layer on different surfaces are summarised in

Table 4-5. The printing parameters also demonstrate the possible choice between reducing the number of layers printed and the etching duration.

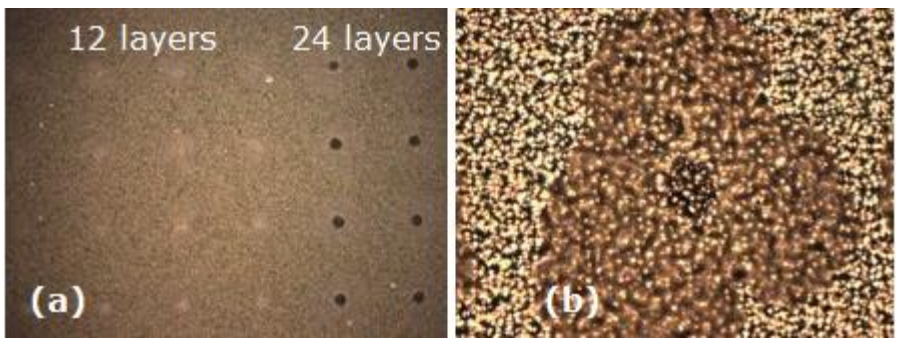


Figure 4-13 Array of point openings etched in an AAO layer on textured wafer. (a) Comparison of different levels of inadequate etching with 12 and 24 layers of printed etchant, respectively, (b) A higher magnification image showing significant spreading of the etchant around the point opening.

Table 4-5 Printing parameters required to etch holes in a 600 nm AAO layer on different surfaces.

Surface Topography	Number of Layers	Etch Time (min)
Polished	4	30
	6	13
Planarised	6	45
	8	30
Textured	12	70
	24	45

4.3.4 Conclusions

The diameter of point openings was directly related to the volume of etchant deposited (i.e., the number of layers printed). Too little etchant resulted in partial etching, however excessive etchant tended to spread on the AAO surface resulting in larger openings. Increased etching duration did not increase the opening diameter, suggesting that the etchant, once deposited, did not spread to any significant extent. The AAO etching rate increased with increased temperature if the quantity of etchant was maintained. However, higher temperatures also increased the evaporation rate of water and excessive evaporation of water reduced the etching rate. Therefore, the determination of the optimal platen temperature represents a compromise between etching rate and maintaining sufficient hydration of the etching environment. The inkjet patterning technique developed is capable of patterning AAO on polished, planarised and textured surfaces, however the process is less effective on textured surfaces. The amount of etchant and etching duration required are largely determined by the surface topography, with increased surface roughness requiring a longer etching duration. Optimised printing parameters for patterning a 600 nm AAO layer on a planarised substrate are summarised in Table 4-6.

Table 4-6 Optimised printing parameters for 600 nm AAO layer on planarised substrate.

Parameters	Value
H_3PO_4 Concentration	50% (w/v)
Jetting Frequency	5 kHz
Firing Voltage	11.2-12.8 V
Drop Velocity	10 m s^{-1}
Volume of Droplet	1 pL
Platen Temperature	60 °C
Relative Humidity	< 50 %
Number of Layers	8
Etching Duration	30 min

4.4 Rear Local Contact Formation

The ultimate goal of these experiments was to form reliable localised rear contacts through the openings of the patterned dielectric layer. After having established

a repeatable process to create point openings in the AAO by inkjet printing in Section 0, this section reports on experiments which explored the local contact formation by alloying evaporated aluminium through point openings in the patterned AAO. The effect of contact spacing and the peak firing temperature on the physical properties of the formed contact regions were investigated. Scanning electron microscope and EDS analyses were performed to study the physical properties of the local contacts.

4.4.1 Impacts of Patterning on Surface Passivation

One of the advantages of inkjet patterning over laser patterning is the elimination of process-induced damage to the crystalline silicon, which is detrimental to the quality of surface passivation and therefore cell V_{oc} and also, in some cases *FF* [258]. An experiment was therefore conducted to investigate how the inkjet patterning affected surface passivation. The iV_{oc} of wafers at 1-sun was measured to determine this impact.

4.4.1.1 Experimental

A group of (100)-oriented boron-doped *p*-type Cz, 1 Ω cm wafer fragments (40 mm × 40 mm) were processed as described in Section 4.2.3.1, up to the anodisation step. The test structure after anodisation is shown in Figure 4-14. A 20 mm × 20 mm array of point openings was inkjet-patterned using the printing conditions summarised in Section 4.3.4. Wafers were etched for 30 min on the 60 °C platen. After etching, wafers were rinsed in DI water for 5 min. An AFM (Dimension Icon, Bruker) scan was performed over the point openings to illustrate the edge resolution of the point openings. Photoconductance (PC) measurements were performed using a WCT-100 lifetime tester (Sinton Instruments) and effective carrier lifetimes were measured using the generalised method [259] before and after inkjet patterning and represented as 1-sun iV_{oc}, using the relationship:

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{N_A \Delta n}{n_i^2}\right) \tag{4.3}$$

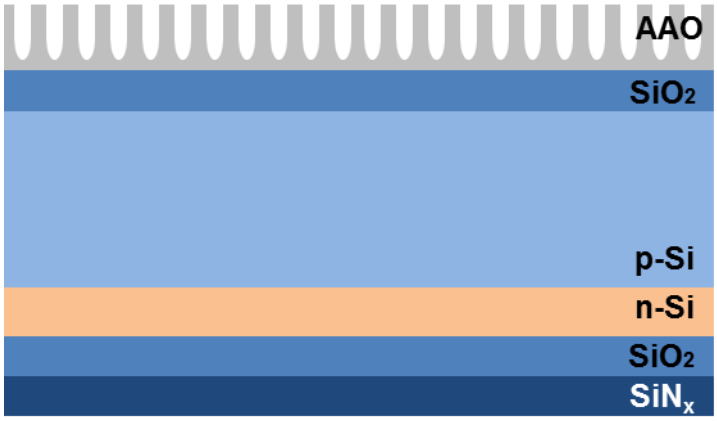


Figure 4-14 Test structure for inkjet patterning and LBSF formation. The thickness of the *p*-type substrate was 157 µm and the thickness of SiO_2, SiN_x and AAO layers were 18, 65 and 600 nm, respectively.

4.4.1.2 Results and Discussion

The iV_{oc} estimated by PC before and after the etching process are compared in Figure 4-16. The iV_{oc} values did not vary significantly, which can be attributed to: (i) inkjet patterning not inducing any damage in the dielectric in the non-patterned areas (see Figure 4-15); and (ii) the thermal SiO_2 layer remaining after complete etching of AAO due to the slow etch rate of the thermal SiO_2 in the concentrated H_3PO_4 (0.18 nm min^{-1} at 160 °C [221]) thus leaving the silicon surface in the opened areas passivated even after opening formation.

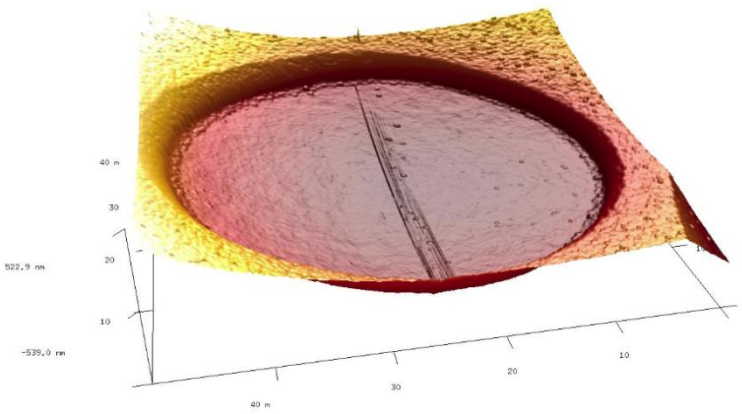


Figure 4-15 Three-dimensional (3D) representation of AFM scan in the point opening of the patterned AAO layer, showing a smooth surface of point opening and a well-resolved edge of patterned area. The scratch in the middle of the opening was due to the scanning tip of AFM.

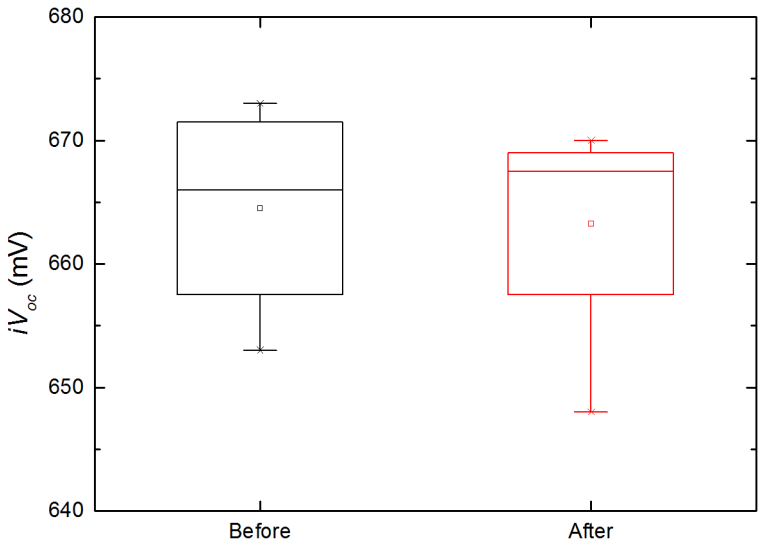


Figure 4-16 The iV_{oc} of wafers before and after inkjet patterning of AAO. For all wafers, the point openings were spaced 250 µm apart and the box is showing the standard deviation of six wafers.

4.4.2 Effect of Contact Spacing

Contact spacing is an important parameter in local contact design, as it determines the contact fraction at a given contact opening size. However there is a compromise in determining the contact fraction. On the one hand, the fraction has to be minimised such that most of the surface is passivated and the effective rear *SRV* is reduced. This also acts to increase the internal reflectance of long wavelength light due to the presence of a displaced rear reflector. On the other hand, due to the practical limitation of reducing the contact opening size, the reduced contact fraction usually requires the contacts to be spaced further apart. In this case, carriers need to travel laterally in the bulk to be collected which can result in current-crowding in the contact area and a decrease in *FF* [227]. Furthermore, as discussed in Chapter 3, the contact spacing also affects the formation and physical properties of the LBSF regions, therefore it is of considerable importance to investigate the effect of contact spacing on the LBSF formation through inkjet-patterned AAO layers.

4.4.2.1 Experimental

A batch of nine wafers was processed as described in Section 4.2.3.1. Point openings in a 20 mm × 20 mm array were inkjet patterned in 600 nm AAO layers formed on planarised wafer surfaces with a spacing between adjacent points of 125, 177

and 250 μm, which corresponded to contact fractions of ~ 8%, 4%, and 2%, respectively, assuming a circular metal contact area having a diameter of 40 μm.

After patterning the 600 nm thick AAO layer, a 2 μm thick aluminium layer was evaporated over the patterned surface, followed by firing in a Centrotherm belt furnace with a peak temperatures of 850 °C and a belt speed of 4800 mm min^{-1}. This corresponded to the wafers being exposed to the peak firing temperature for duration of 5 s. For all wafers, the LBSF regions were exposed by laser cleaving from the non-patterned surface and etching for 20 s in a CH_3COOH: HNO_3: HF = 6:3:1 solution which selectively etches *p*+ silicon at a much faster rate than lightly-doped bulk silicon. The wafer cross sections were then imaged by SEM to visualise the formed *p*+ LBSF and to estimate their dimension and uniformity. An EDS elemental analysis was performed to determine the mass percentage of elements in the area of interests. The interfaces in the non-contact and contact area were exposed by focused ion beam (FIB) to investigate if AAO could withstand the high temperature firing process.

4.4.2.2 Results and Discussion

After inkjet patterning the completeness of etching was visually inspected under microscope, with the grey colour showing exposed silicon (see Figure 4-17). To further confirm, SEM top down imaging was performed. As shown in Figure 4-18, the opened areas appear brighter than neighbouring area covered by AAO, which is because the silicon substrate is more conductive than the dielectric, therefore provides stronger electron signals. The high magnification SEM image illustrates a clean and smooth opening area, indicating the complete etching of the AAO in the opening.

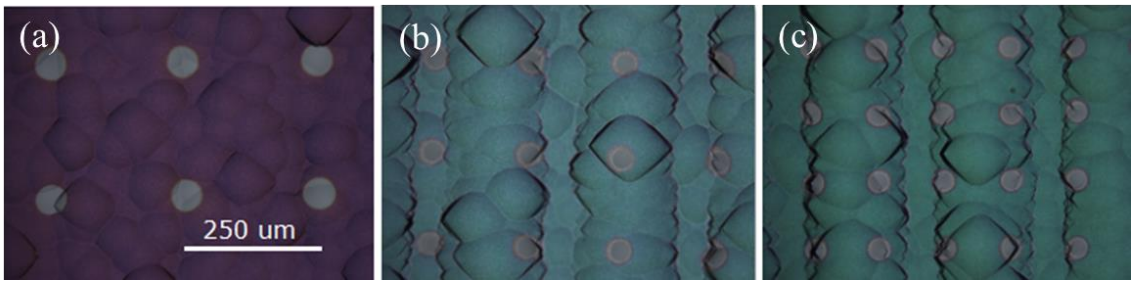


Figure 4-17 Optical microscope image of inkjet patterned AAO with 250, 177 and 125 μm contact spacing. The difference in the film colour is due to a variation in the AAO thickness from different aluminium evaporation batches and the line in (b) and (c) represent residual saw lines from the wafering.

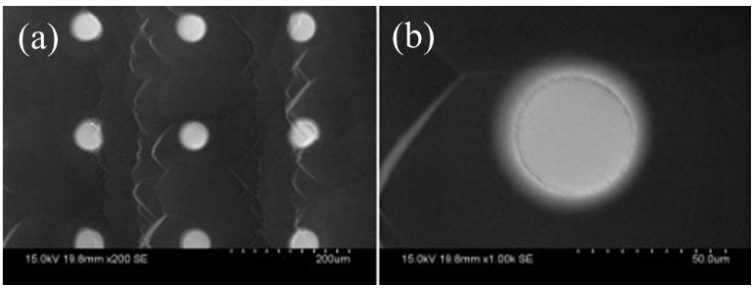


Figure 4-18 SEM top down image of inkjet patterned AAO with 177 m point spacing. Strong electron signal in the point openings indicates that the AAO layer is fully removed, as the silicon substrate is more conductive than the AAO. The high magnification image on the right shows the uniformity of etching within the point opening.

Figure 4-19 shows the point opening diameter before and after firing, the contact depth and the thickness of the LBSF regions with different contact spacing. Firing increased the contact diameter over a wide range of contact spacing. Although all the wafers had similar initial diameter of 40 μm before firing, the diameter of 125 μm spaced contacts experienced significantly more increase in diameter than the contacts spaced 250 μm apart, which was in good agreement with [260]. This trend was useful for the rear contact design, with the contact widening effect becoming less evident towards 1% contact fraction [227].

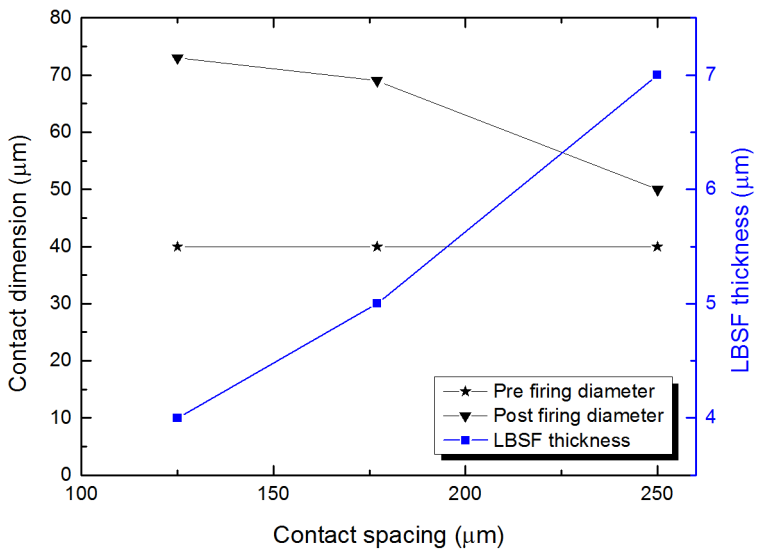


Figure 4-19 Contact dimension and LBSF thickness graphed as a function of contact spacing. All wafers were fired at peak temperature of 850 °C in an inline firing furnace where the peak firing temperature was experienced for a time of 5 s.

There are two hypothesised causes for the contact widening. First, similar to the findings in Chapter 3, it is possible that saturation of aluminium with silicon above the dielectric regions adjacent to the line openings may result in increased dissolution of silicon on heating due to the increased fluidity of the surrounding molten alloy. Therefore silicon dissolution proceeds laterally to effectively extend the diameter of the opening (see Figure 4-20). Anodic aluminium oxide acts as an effective barrier for high temperature firing of aluminium in the non-contact area, however although at the edge of the contact area the layer remains, the aluminium/silicon eutectic region is extended underneath it due to lateral dissolution of silicon. Second, the spreading of the etchant during inkjet patterning, which can be caused by misalignment of droplets, over supply of etchant, or high relative humidity, weakens the AAO layer at the edge of openings. This effect is suggested in the SEM image in Figure 4-18 where there is a transition of the signal intensity at the edge of point opening, indicating a varied thickness of the AAO layer.

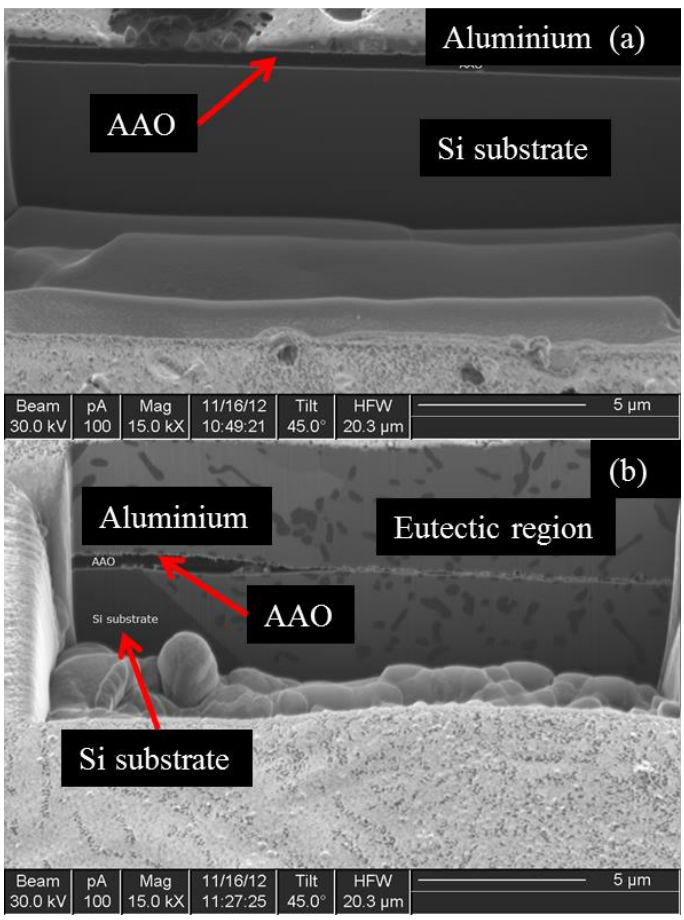


Figure 4-20 Cross-sectional SEM images of: (a) metal/AAO/silicon interface in a non-patterned area; and (b) metal/silicon interface at the edge of the contact area. Both interfaces are exposed by an FIB cut.

The thickness of LBSF regions increased with increased contact spacing. This trend is in reverse to the trend observed in Chapter 3 with screen-printed aluminium. These experiments used thin (2 μm) evaporated aluminium which appears to be more reactive at high temperatures. A blistering effect was observed in the evaporated aluminium layer in the non-contact area [see Figure 4-20(a) and Figure 4-21], which was believed due to the volume expansion and escape of the air from the pores of the AAO at high temperatures. An EDS line scan across the surface showed the black spots were areas where the capping aluminium had been removed. The AAO layer was exposed in these local areas, which would have disrupted the dissolution of silicon in aluminium in the alloying process, and therefore possibly affected the formation of LBSF regions.

Similar to the discussion in Section 3.4.2.1, redistribution of aluminium was also observed, with thicker aluminium resulting in the contact areas (see Figure 4-20). The accumulation of aluminium in the contact area may be due to the driving force of the alloying at high temperatures, but further investigation is needed before conclusions can be drawn. The redistribution of aluminium mitigates the difference caused by varied contact spacing, which yields the inversed trend of the LBSF thickness. However, the increase in the LBSF thickness was largely dominated by the peak firing temperature which will be discussed further in the next section.

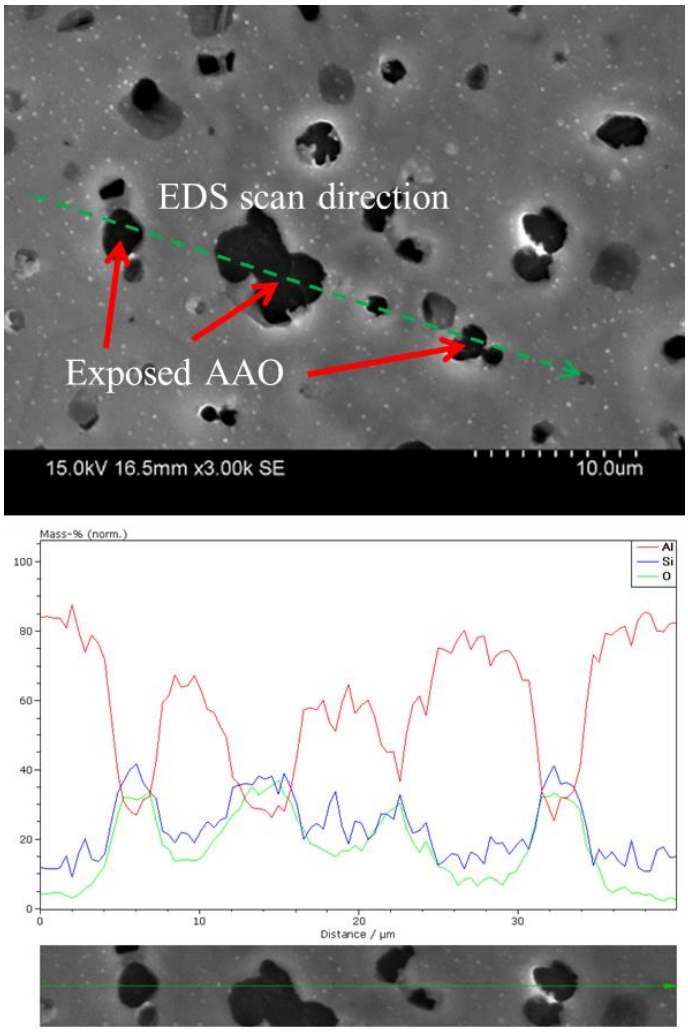


Figure 4-21 SEM top down image and normalised mass percentage of elements extracted from EDS line scan analysis of evaporated aluminium layer after firing at 800 °C and a belt speed of 4800 mm min^{-1}.

4.4.3 Effect of Metallisation Firing Temperature

The amount of silicon which forms the LBSF is dependent largely on the peak firing temperature, with the thickness increasing with increased peak temperature. At higher peak temperatures, the solubility of aluminium in the silicon increases, hence resulting in a higher concentration of aluminium at the initial silicon-liquid interface during liquid phase epitaxial growth. Moreover, given an identical cooling rate, a higher peak firing temperature allows longer time for the sample to cool to the eutectic temperature, thus resulting in more time for epitaxial growth and therefore a thicker LBSF regions [261]. This section investigates the effect of firing temperatures on the dimensions of the LBSF regions.

4.4.3.1 Experimental

A batch of wafers was processed as described in Section 4.2.3.1. Point openings in a 20 mm × 20 mm array were inkjet patterned in 600 nm AAO layers formed on planarised wafer surfaces with a spacing of 250 μm, in order to simulate the most appropriate contact fraction. An aluminium layer of 2 μm was evaporated over the patterned AAO layer. Wafers were then fired in the Centrotherm belt furnace with a belt speed of 4800 mm min^{-1} and the peak firing temperature varied from 600 to 850 °C with an increment of 50 °C. The physical properties of the LBSF regions were characterised as described in Section 4.4.2.1.

4.4.3.2 Results and Discussion

From Figure 4-22 it is clear that the depth, width and thickness of the LBSF regions increased with the increased peak temperature. These effects occurred markedly at temperatures greater than 700 ºC. In contrast, no *p+* region were evident for samples fired at temperatures ≤ 650 ºC, as the aluminium melt begins at temperatures in excess of 660 ºC [262]. This confirms the findings of Urrejola *et al.* that temperature determines the inter-diffusion of the aluminium and silicon during the firing process [263].

The increase in contact area occurs because, at higher peak temperatures, the inter-diffusion of silicon and aluminium are both increased [204]. A more extensive alloying process occurs at the aluminium/silicon interface, therefore forming a large reservoir of molten alloy in the contact area. However during cool down, once the eutectic temperature is reached, a eutectic layer of approximately 12% silicon and aluminium immediately solidifies [262]. Consequently, the size of the eutectic region reflects the amount of silicon dissolved into the aluminium and hence a higher temperature results in larger contact widths and depths.

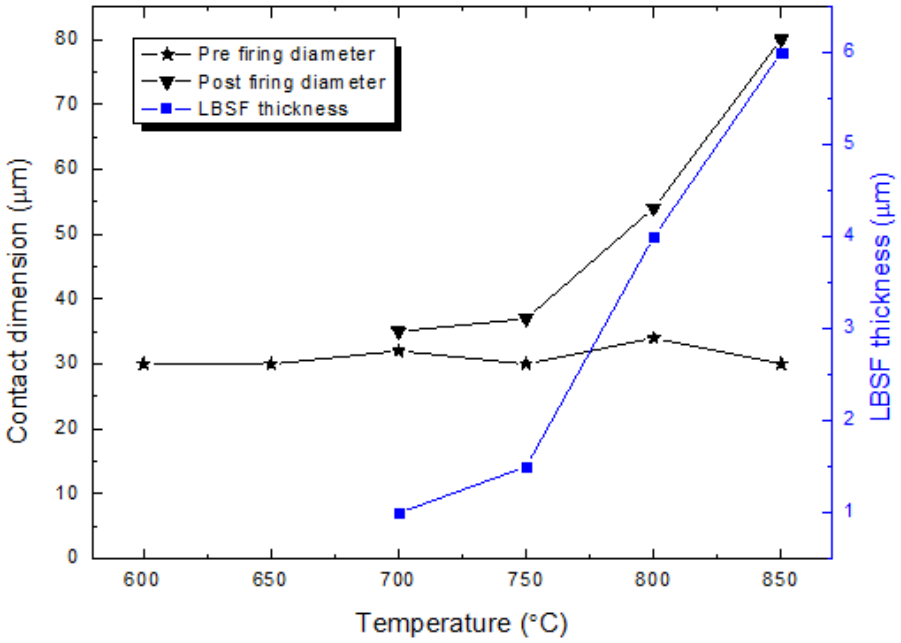


Figure 4-22 Contact dimension and LBSF thickness graphed as a function of peak firing temperature. All wafers had a contact spacing of 250 µm and were fired in an inline firing furnace with a belt speed of 4800 mm min^{-1}, where the peak firing temperature was experienced for a time of 5 s.

Figure 4-23 shows the SEM cross sectional images of LBSF regions formed by firing evaporated aluminium at high temperatures through inkjet-patterned point openings of AAO. Unlike the semicircular shape of line contacts presented in Chapter 3, the alloyed contacts through point openings were triangular in shape. It is because the dissolution of silicon into aluminium occurs faster along (100) planes, leading to the formation of LBSF regions that expose the (111) silicon planes. This faster silicon dissolution from (100) planes compared to (111) planes is similar to what occurs for anisotropic alkaline etching of silicon [264]. The truncated triangular shape of some contacts is because the exposed cross section does not coincide the centre of the contact. On the one hand, the triangular shape contact increases the actual contact area and the ratio of actual contact area over opening area is inversely proportional to the cosine function of the pyramid's characteristic angle. Given a typical characteristic angle of 54.74°, the actual contact area is ~ 1.73 times larger than the opening area, which adds error in the contact fraction calculation. On the other hand, the increase contact area may reduce current-crowding and therefore the spreading resistance associated with the rear local contact. However, further analysis is required to study the impact of this effect.

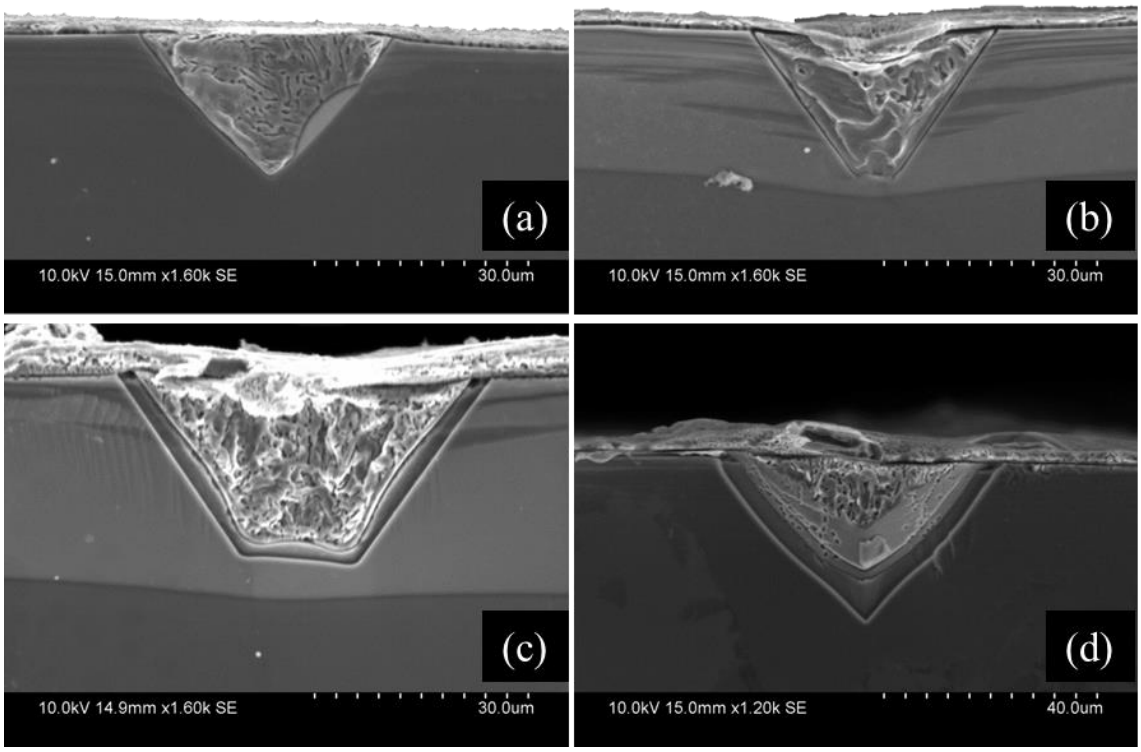


Figure 4-23 Cross-sectional SEM images showing the local contacts formed at (a) 700 °C; (b) 750 °C; (c) 800 °C; and (d) 850 °C.

Although thicker LBSF regions were formed by firing at high temperatures, there were side effects that were detrimental to the cell performance. First, at very high temperatures, aluminium can penetrate through the AAO and alloy with the silicon substrate in the non-contact areas. These unintended contacts are usually small in size with very thin LBSF regions formed. Therefore minority carriers are not effectively shielded causing a very high *SRV*. Figure 4-24 shows such a contact formed by aluminium spiking at 850 °C, which is 10 µm wide and 6 µm deep. However the LBSF is not visible.

Second, Kirkendall voids start to form at very high temperatures, which is similar to what was observed with line contacts and is discussed in Section 3.3.2.5. A high density of voids in the local contact area would increase the R_s, and therefore limit the *FF* of cells. Figure 4-25 shows the EDS elemental mapping of alloyed local contacts formed at 750 and 850 °C, respectively. At 750 °C, a strong aluminium signal in the eutectic region was observed, as in the region contains the alloy of ~ 12% silicon in

aluminium. At 850 °C, however, silicon signal from the silicon substrate behind the eutectic region was detected, indicating void formation in the region.

Third, high temperatures result in more severe blistering presumably due to escape of air from the pores. This effect is more pronounced when evaporated thin aluminium layer is used. Blistering reduced the coverage of metal and this disruption of the capping metal layer increased the resistance in the metal layer. Furthermore, the exposed AAO layer may experience degradation in the environment and limit the reliability of the cell.

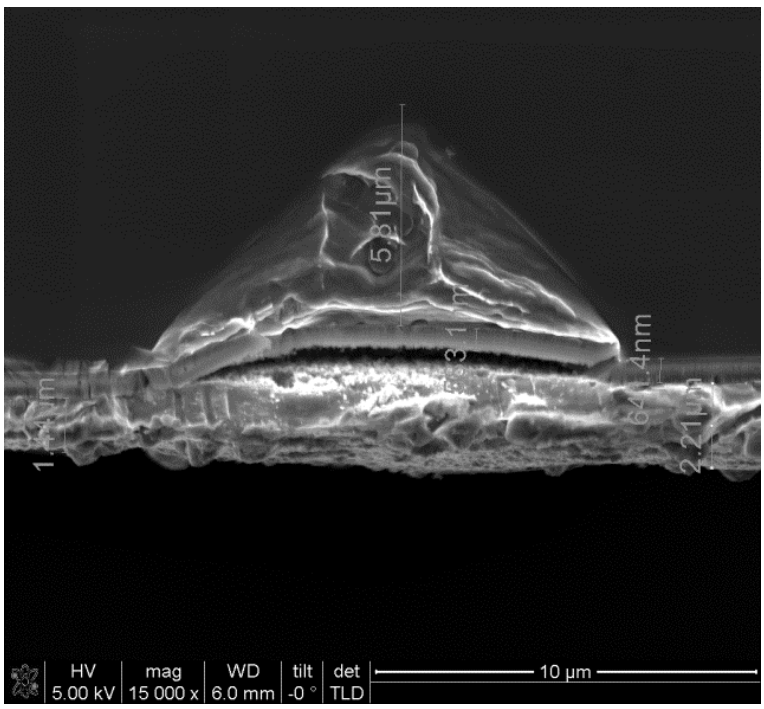


Figure 4-24 Cross-sectional SEM image showing unintended local contact formation due to aluminium spiking through the AAO layer after firing at 850 °C with belt speed of 4800 mm min^{-1}.

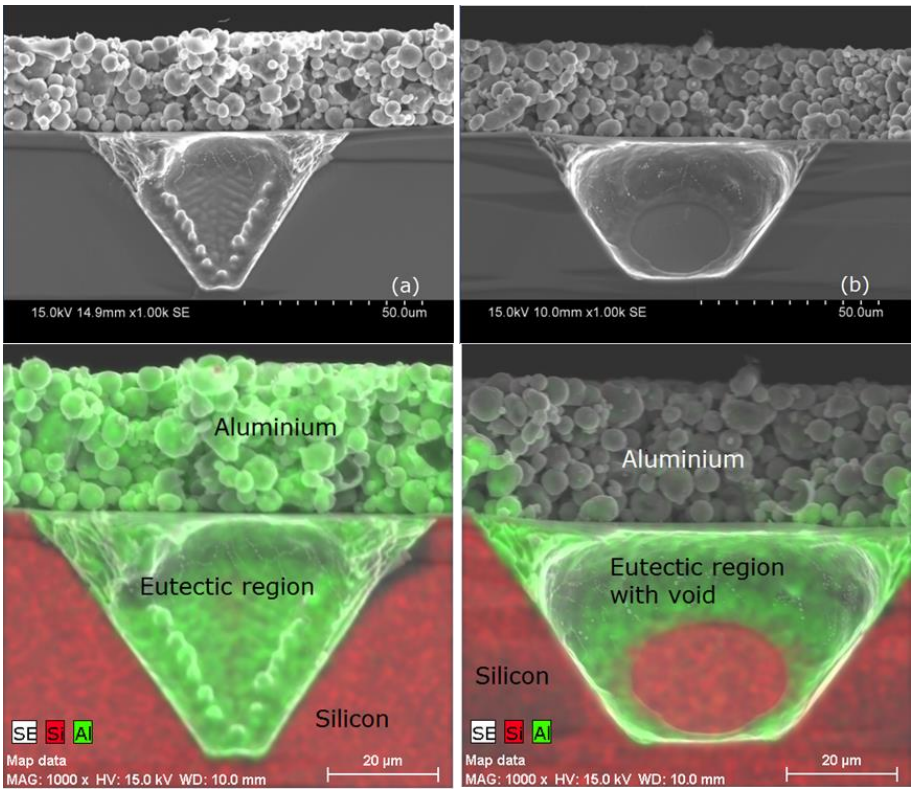


Figure 4-25 Cross-sectional SEM images and EDS mapping of local contacts formed via firing screen printed aluminium paste at (a) 750 °C and (b) 850 °C. A void formed in the eutectic region of the 850 °C fired contact is visualised by detecting the silicon signal in that region.

The optimised firing temperature should be determined by the balance of the LBSF thickness and parasitic detrimental effects. Chen *et al.* showed that a uniform LBSF region with a thickness of at least 2 µm was required to achieve effective local contacts on the rear surface of a solar cell [225]. Therefore, the optimised peak firing temperature should be between 750 and 800 °C.

4.4.4 Conclusions

The physical properties of LBSF regions formed through inkjet-patterned point openings in AAO layers are primarily determined by the peak firing temperature and the contact spacing. Firing at high temperatures resulted in an increase in the diameter of the local contact regions for all contact spacing values investigated, however the extent of the increase was reduced with larger contact spacing (i.e., 250 µm). Reverse of trend, which has been previously observed for aluminium-alloyed LBSF in line contacts [260], is believed to be due to the saturation of aluminium with silicon above the dielectric regions adjacent to the opening may result in increased dissolution of silicon on heating due to the increased fluidity of the surrounding molten alloy.

Since larger contact spacing resulted in both less contact widening and a thicker LBSF it was concluded that a contact spacing of 250 μm or greater was desirable. Contacts spaced further apart than 250 μm were not investigated because they would have required the use of discrete point patterns, rather than linear patterns with a large drop spacing as employed in these experiments. However, it should be noted that such input patterns for printing can be generated and future work will involve the use of discrete point patterns with adjacent point openings being spaced further than 250 μm apart.

Higher firing temperatures facilitated more active inter-diffusion of aluminium and silicon, yielding a thicker LBSF. On the other hand, at high temperatures the probability of Kirkendall void formation, aluminium spiking and blistering of the aluminium capping layer were dramatically increased, all of which would be detrimental to the cell performance. Furthermore, the contact diameter was significantly increased at high temperatures which increased the metal contact fraction. In order to achieve high V_{oc} values for finished devices, the contact fraction is desirably maintained small (e.g., 1%), therefore a moderate peaking firing temperature of ~ 800 °C would be preferable for cell fabrication.

4.5 Limitations of Clip Anodisation

It was demonstrated in the previous sections of this chapter that AAO layers can be effectively patterned by inkjet printing of H_3PO_4. Furthermore, LBSF regions can be formed through these point openings by aluminium alloying. If the patterning method could be implemented reliably and with high processing throughput, then it is interesting to consider whether AAO layers could represent a potential alternative to PECVD SiN_x as a rear surface passivation layer for PERC solar cells. It has been demonstrated that these layers can provide effective passivation for both *n*-type [265] and *p*-type silicon surfaces [206]. Additionally they have been demonstrated to provide a source of hydrogen that can act to passivate interface state defects [207]. Consequently, it was decided to investigate the compatibility of the clip anodisation of aluminium method with industrial-sized wafers and available electroplating toolsets. A group of FZ wafer fragments and commercial-grade Cz wafers were anodised using an industrial in-line metal plating tool with appropriate changes for the clip anodisation

process. The quality of surface passivation after anodisation and annealing is reported and the limitations of the clip anodisation are outlined.

4.5.1 Experimental

A batch of 290 µm thick, 100 Ω cm, 40 mm × 40 mm FZ wafers fragments was used for lifetime tests and to benchmark the lab process [see Figure 4-26 (a)]. Saw damage was removed from the wafers by etching in 25% (w/v) NaOH at 80 °C for 10 min. Following a full RCA clean, the wafers were oxidised in a quartz tube furnace at 980 °C for 18 min to form a 17 nm dry thermal SiO_2 layer, which acted as a barrier for subsequent anodisation process. A layer of aluminium with thickness of either 300 and 600 nm was evaporated on both wafer surfaces.

The full-sized wafer tests were performed using 180 µm, 3 - 5 Ω cm, 156 mm × 156 mm commercial grade boron-doped Cz wafers with a $POCl_3$ diffused emitter (~100 Ω/□), thermal SiO_2 and PECVD SiN_x on front surface [see Figure 4-26 (b)]. Half of these wafers underwent a rear etch process, which removed the shallow diffused junction on the rear surface as well as the thermal SiO_2 layer [see Figure 4-26 (c)]. A layer of 600 nm aluminium was evaporated to the rear surface of all these wafers for anodisation.

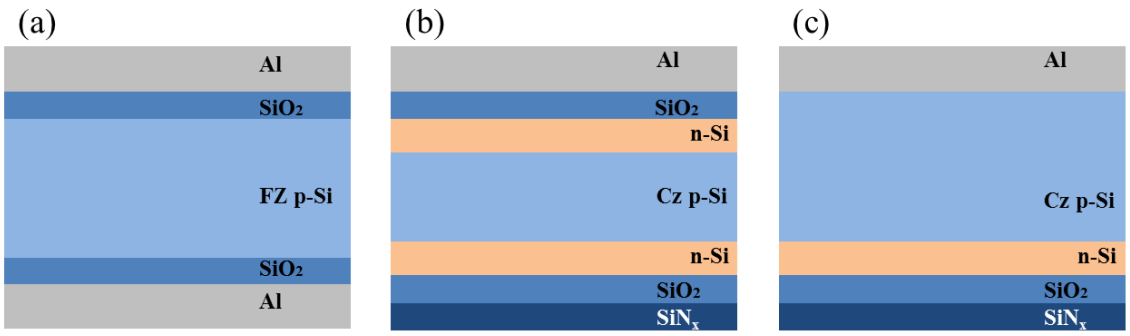


Figure 4-26 Schematic diagram of wafers used for clip anodisation tests using an industrial in-line metal plating tool.

The wafers were then anodised using an industrial in-line metal plating tool. Wafers were positioned vertically in the electrolyte contacted by a group of stainless steel clips on the upper edge. A titanium mesh positioned in parallel with the wafer was used as the cathode. The distance between the anode and the cathode was adjusted to be between 0 to 10 cm. Bias voltages of either 25 or 30 V were applied across the stainless steel clips and the titanium cathode. Anodisation was performed at a bath temperature of

25 ºC in electrolyte containing 0.5 M H_2SO_4, which was agitated by a pump circulation system.

After anodisation, wafers were annealed in nitrogen in a quartz tube furnace at 400 °C. Effective minority carrier lifetimes were assessed using PC and photoluminescence (PL) imaging both after anodisation and after anneal. Cross-sectional SEM imaging was performed to investigate the uniformity and completeness of the anodisation process.

4.5.2 Results and Discussion

4.5.2.1 FZ Wafer Anodisation

Planar FZ wafer fragments were anodised under 25 V bias voltage and 10 cm anode to cathode distance, however they were not uniformly anodised with the industrial tool. As shown in Figure 4-27, the aluminium layer at the electrolyte/air interface oxidised faster, thereby 'cutting off' the channel for current to flow to the rest of the aluminium surface. The uniformity of the anodisation was poor, and varied between wafer fragments. The poor uniformity was found not to depend on the thickness of the aluminium layer, although thinner aluminium layer was expected to be anodised more uniformly.

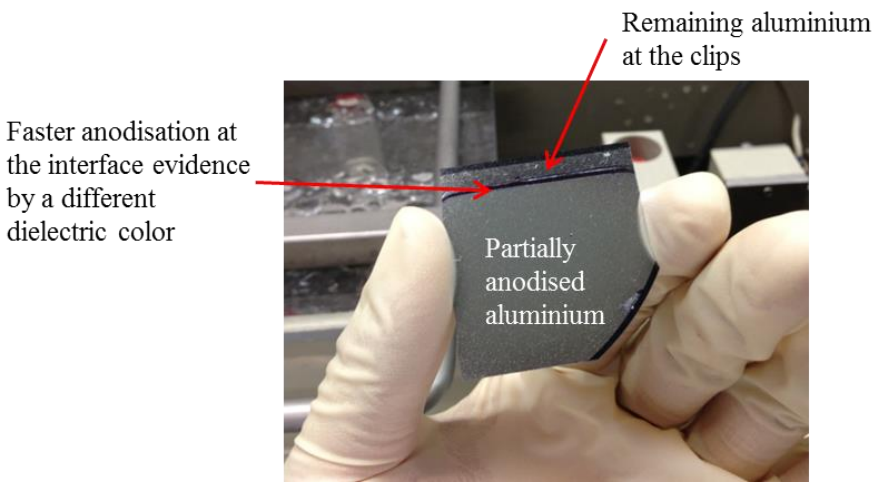


Figure 4-27 An anodized FZ wafer fragment showing non-uniform anodisation at the electrolyte/air interface.

The problem of a non-uniform anodisation rate at the interface and a large remaining area of aluminium at the clips were addressed by clamping the wafer between two titanium plates, and immersing the wafer completely into the electrolyte. The

titanium was readily oxidised in the electrolyte and formed a dense oxide layer which prevented further anodisation (of titanium). This effectively eliminated local heating at the electrolyte/air interface, and enabled full area contact between the wafer and electrolyte. Although it resulted in improved uniformity, the area covered by the titanium plate remained un-anodised.

4.5.2.2 Commercial Grade Cz Wafer Anodisation

In general, anodisation on 156 mm × 156 mm commercial grade Cz wafers demonstrated increased uniformity in thickness according to visual inspection. It was attributed to the increased surface roughness of the alkaline textured surfaces. The aluminium at the intersection between neighbouring pyramids was likely to assist the lateral current flow across the wafer, therefore enhancing the anodisation. This finding was consistent with the lab process where more uniform anodisation of textured rather than planar or polished wafers was also observed.

As with the lab process, the anodisation current was used as an effective indication of the anodisation process. For the 156 mm × 156 mm wafers, once the current stabilised below 200 mA, it was assumed that anodisation of aluminium was complete. Figure 4-28 illustrates the anodisation current as a function of time for a textured and rear etched Cz wafers. Significant variation in the anodisation current was observed from wafer to wafer. Textured wafers showed better uniformity by visual inspection and shorter anodisation time (< 4 min) than rear etched wafers. The longer anodisation time for rear etched wafers was hypothesised to be due to anodisation extending into the silicon substrate once the aluminium was anodised, as there was no thermal SiO_2 layer under aluminium for the rear etched wafers.

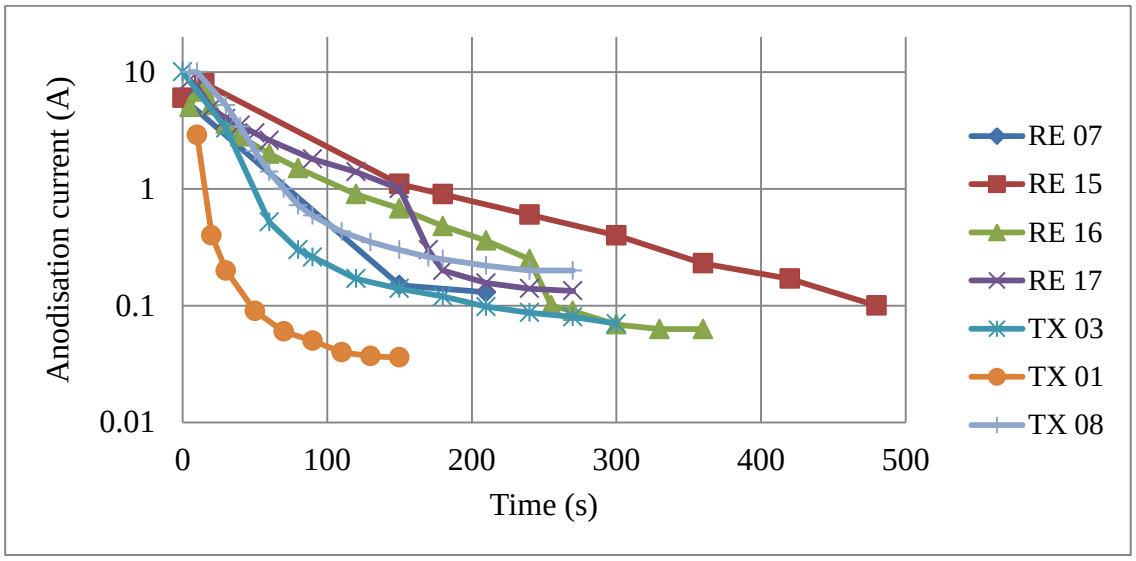


Figure 4-28 Anodisation current graphed as a function of time for textured (TX) and rear etched (RE) 156 mm × 156 mm Cz wafers.

Interestingly, under appropriate bias voltage (e.g., 30 V), the initial current was as high as 10 A. When this high current flowed through the clip contacts, significant amounts of heat were generated locally at the clip/wafer contacts. In the experiment, this resulted in the melting and deformation of the polypropylene part of the clip and resulted in wafer breakage due to locally-changed mechanical stress. This is clearly a weakness of the clip contacting method, which not only causes part of the wafer to remain un-anodised but also reduces the anodisation efficiency because a significant amount of power is dissipated as heat. It also necessitates a careful selection of clip contacting materials.

4.5.2.3 Surface Passivation

The effect of surface passivation was then investigated. As shown in Figure 4-29, the textured wafers with the thin thermal SiO_2 intervening layer experienced increased iV_{oc} of ~ 20 mV directly after anodisation and a small further improvement of 5 mV after the subsequent anneal. The improvement in effective lifetime was also partially attributed to the junction passivation for the non-rear etched wafers. On the contrary, the rear etched wafers without thin thermal SiO_2 had a significantly lower initial iV_{oc} due to the lack of rear surface passivation. The iV_{oc} was then degraded after anodisation and the annealing process. This comparison agreed with the observation in the lab process, which highlighted the significance of the intervening SiO_2 during anodisation process [256]. The thin SiO_2 acts as a barrier layer to prevent current from anodising the silicon

substrate when aluminium was fully anodised. If anodisation extends into the silicon substrate then it is reasonable to expect a very high D_{it} to result as the porous silicon has an increased effective surface.

Another notable disadvantage of anodising without an intervening SiO_2 layer was the poor adhesion between AAO and the silicon substrate. The AAO layer peeled off from the silicon surface after anodisation, especially on the planar and polished surfaces. The cause of the poor adhesion was believed to be due to the stress resulting from the different volume expansion coefficient of the anodised silicon and aluminium. This issue was solved by growing a layer of thermal SiO_2 or anodic SiO_2 on the silicon surface before depositing aluminium. This SiO_2 intervening layer prevents silicon from being anodised once the aluminium is fully anodised, therefore significantly improved the adhesion of AAO.

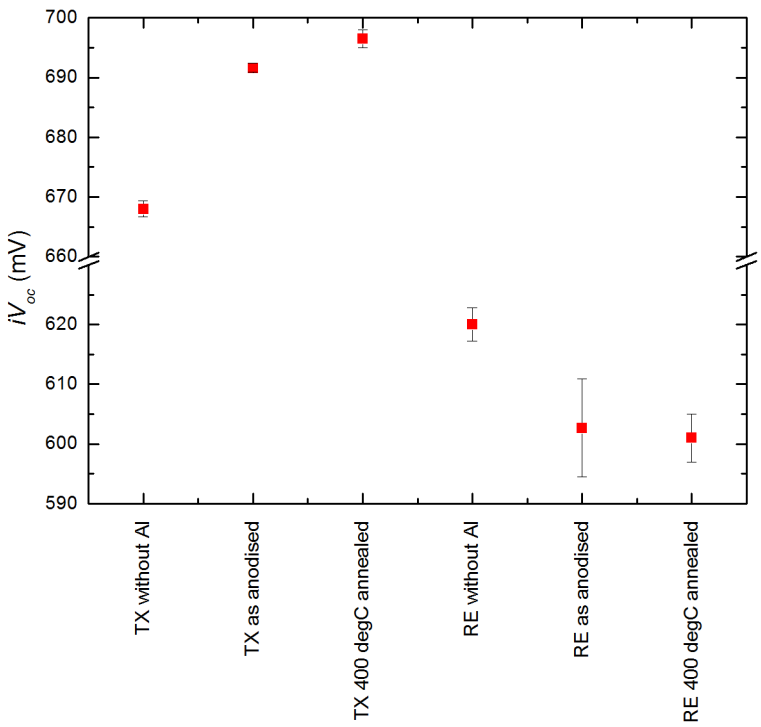


Figure 4-29 Implied V_{oc} measured by PC after anodisation and subsequent annealing process of representative textured (TX) and rear etched (RE) wafers.

The PL measurements confirmed the abovementioned finding. In the open circuit PL images shown in Figure 4-30, brighter regions indicated less non-radiative recombination, therefore higher iV_{oc}.

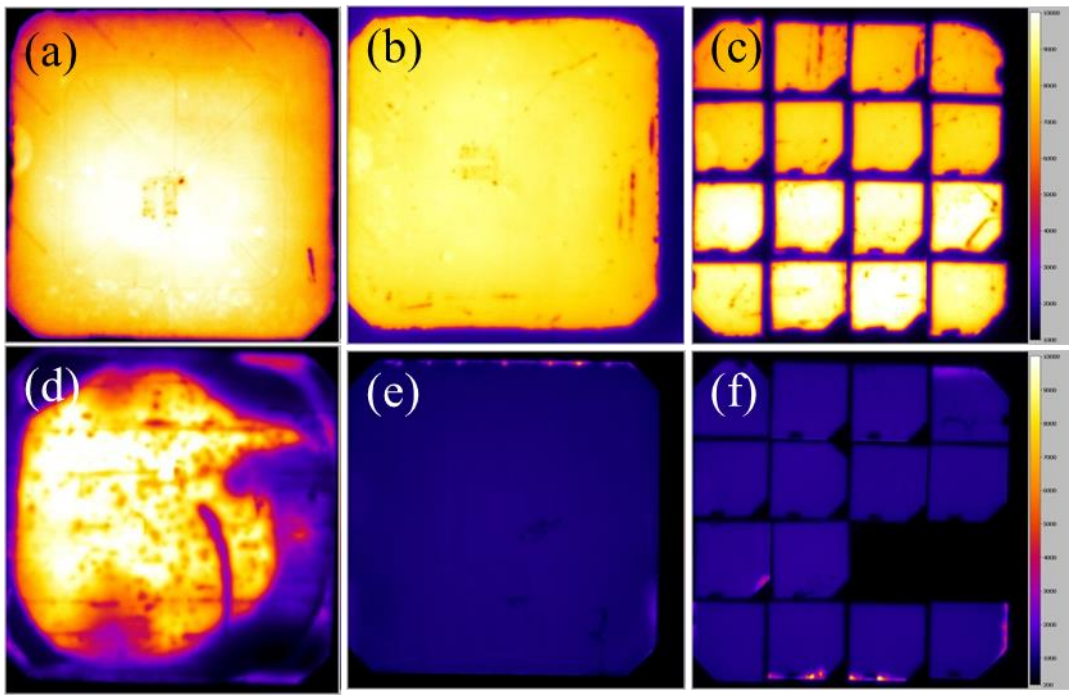


Figure 4-30 Open circuit PL images taken with 1-sun illumination and 1 s exposure time. The PL counts are plotted using the same scale showing textured wafers (a) without aluminium; (b) as anodised; (c) after 400 °C anneal (bottom eight wafers). And rear etched wafers (d) without aluminium; (e) as anodised; (f) after 400 °C anneal (bottom six wafers). In (c) and (f) the wafers in the two top rows were not annealed to establish a baseline.

High resolution SEM cross sectional imaging was performed to investigate the interface of AAO and silicon substrate. Illustrated in Figure 4-31, a layer of material with strong electron signal was commonly observed between AAO and silicon substrate, especially at the intersection of the pyramids. This material was attributed to the aluminium residue due to incomplete anodisation. Without the intervening SiO_2 layer, the residue aluminium was directly in contact with the silicon substrate, resulting in high *SRV* sites on the surface, which degraded the iV_{oc}. After annealing, the aluminium residue would have formed ohmic contact with silicon in the localised area (as reported in [206]), however the *SRV* was still high, therefore the iV_{oc} of the rear etched wafers measured by PC and PL was strongly limited by surface recombination.

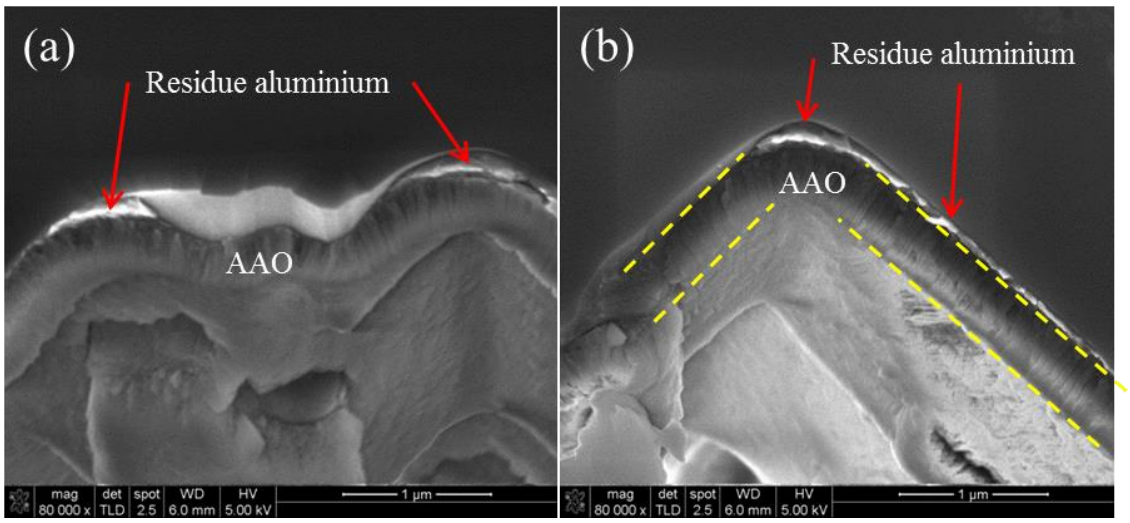


Figure 4-31 High resolution cross-sectional SEM images of rear etched wafers as anodised (a) and after 400 °C nitrogen annealing (b) showing the aluminium residue at the intersection and wall of the pyramids. The AAO is shown in between the light-yellow dash lines.

Figure 4-32 shows cross sectional SEM images of AAO on textured wafers with an intervening SiO_2. Although the uniformity in thickness was significantly improved, aluminium residue was still observed at the intersection of pyramids. This observation highlighted another limitation of the clip anodisation method, which was the incomplete anodisation of aluminium on wafers with rough surfaces. The improvement in iV_{oc} was attributed to the presence of the intervening SiO_2, which acted to prevent the anodisation current from anodising the silicon substrate and also prevented residual aluminium from contacting the silicon surface.

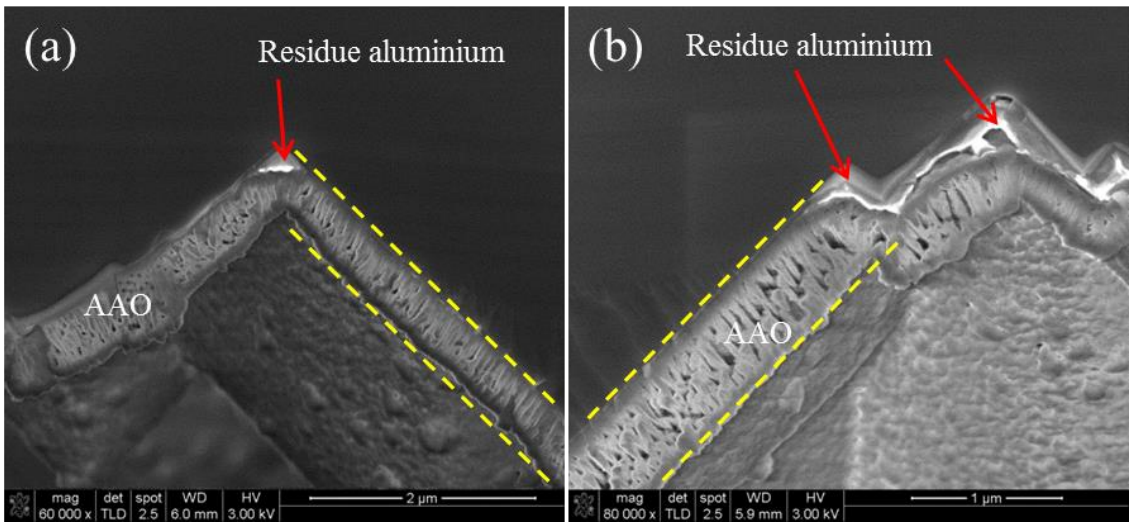


Figure 4-32 High resolution cross-sectional SEM images of textured wafers as anodised (a) and after 400 °C nitrogen anneal (b) showing the aluminium residue at the intersection and wall of the pyramids. The AAO is shown in between the light-yellow dash lines.

4.5.3 Conclusions

It was demonstrated that it was possible to anodise 600 nm of aluminium on 156 mm × 156 mm commercial grade Cz wafers using an in-line plating tool. If a belt speed of 3 m min^{-1} is used, then the clip anodisation process has a through put of ~ 900 wafers per hour by using a 10 m long in-line tool. An intervening SiO_2 layer between aluminium and silicon substrate was found to be essential for improved surface passivation. The issue of remaining aluminium at the clips can be addressed by using titanium clips and fully immersing the wafer and clips into the electrolyte. This adaptation improved the uniformity of anodisation, however would result in a higher tool and consumable (i.e., clips) cost.

Several limitations of the clip anodisation method were outlined. First, the uniformity of anodisation is strongly dependent on the surface roughness of the wafer. Increased surface roughness increases the uniformity and reduces anodisation time. Second, high surface roughness leads to a higher risk of leaving aluminium residue at the intersection of pyramids. The aluminium residue will contact the lightly doped bulk silicon when fired at high temperatures for LBSF formation and hence form high *SRV* sites which limit the cell voltage. Finally, power dissipated in the R_c locally heats up both the wafer and the clips, resulting in increased risk of mechanical breakage and reduced anode efficiency.

4.6 Chapter Conclusions

In this chapter, an inkjet patterning technique for patterning AAO layers was developed. Inkjet-printed H_3PO_4 can pattern AAO layers into an array of point openings that may be used to facilitate localised rear metal contacts for silicon solar cells. This technique could also be used to pattern line openings by reducing the drop spacing to less than 20 μm. Point openings of diameter of ~ 30 μm was etched in 600 nm AAO layer on planarised silicon surfaces. On polished silicon surfaces, even smaller openings with a diameter of ~ 20 μm were demonstrated. Localised metal contact regions were formed by aluminium alloying through the inkjet-patterned point openings, resulting in LBSFs of thickness up to 7 μm. Consequently, it was concluded that AAO layers can

serve to both passivate surfaces and facilitate small-area metal contacting by way of their porosity leading to reduced etchant spreading for chemical patterning processes.

Although dielectric stacks comprising SiO_2/AAO may represent a possible alternative to SiO_2/SiN_x or AlO_x/SiN_x for rear local contact solar cells, the findings of the anodisation trials using an industrial inline plating tool suggested that the limitations of the clip anodisation technique would hinder this application. Although adequate processing throughput should be possible for large area anodisation, uniform anodisation of aluminium over large areas and independent to surface roughness is required. The presence of residual aluminium, that can penetrate the intervening dielectric layer on firing, limits the usefulness inkjet patterning method developed in the reported experiments in this chapter. In order to overcome the limitations of clip anodisation, a new way of anodising was developed. This method, which uses the light-induced current of the solar cell, is described in the next chapter. Initial experiments focussed firstly on anodising a silicon surface, and then based on the success in growing anodic SiO_2, the technique was then applied to anodising aluminium to from AAO as reported in Chapter 6.

Chapter 5 Light-Induced Anodisation of Silicon

Low-cost surface passivation is a key to reducing the cost per Watt of power reduced by silicon PV devices. Anodic oxides have been shown to electronically passivate silicon wafer surfaces effectively and, if able to replace existing thermal or plasma processes, may enable significant cost savings for the manufacturing of a range of electronic devices and be of particular value to large-area devices such as silicon solar cells. This chapter reports a new method for forming anodic oxides on silicon surfaces using the light-induced current of pn-junction solar cells. The LIA process enables anodic SiO_2 to grow at a rate of 4 nm min^{-1} at RT in a faster, more uniform, and controllable manner compared to previously reported clip anodisation. After annealing in oxygen and then forming gas, the τ_{eff} of 3 - 5 Ω cm, boron-doped Cz wafers with a LIA anodic SiO_2 passivated p-type surface was increased by two orders of magnitude to 150 µs. Capacitance-voltage (C-V) measurements demonstrated a very low Q_f of 3.4 × 10^{11} cm^{-2} and a moderate D_{it} of 6 × 10^{11} eV^{-1} cm^{-2}. This corresponded to a rear SRV of 62 cm s^{-1}, which was comparable with other anodic SiO_2 films that were grown at higher temperatures and longer times. Additionally, a very low leakage current density of 3.5 × 10^{-10} and 1.6 × 10^{-9} A cm^{-2} at 1 and -1 V was measured for LIA anodic SiO_2 suggesting its potential application as insulation layer in IBC solar cells or a barrier for potential-induced degradation. The passivation provided by anodic SiO_2 was stable for a period of 50 days provided the oxide was protected by a 75 nm SiN_x capping layer.

5.1 Introduction

The aim of this thesis was to examine low-cost rear contact schemes that were applicable to commercial grade or lower-quality (e.g., seeded-cast, high performance multi) silicon wafers. Therefore the effectiveness of passivation on these wafers was studied as part of this work (refer to Appendix E). However, the discussion in Section 2.2.1.3 highlights the detrimental effect of thermal oxidation to these wafers, therefore alternative processes that grows high quality SiO_2 layers, with D_{it} comparable to

thermal SiO_2, at low temperatures and atmospheric pressure will be of special interest in this thesis. Previous chapters identified anodisation as a suitable candidate.

Chapter 4 reported a promising rear patterning process which exploited the porous surface properties of AAO layers to achieve fine resolution patterning. However it was shown that, when these layers were formed using clip anodisation, residual aluminium in the AAO caused spiking during a subsequent high temperature firing step when the intent was to form alloyed aluminium regions in the patterned openings in the AAO layer. It was also shown that, although clip anodisation could be performed using an industrial in-line metal plating tool, anodisation of 156 mm × 156 mm wafers required large initial current of up to 10 A to be passed through the clips. The joule heating arising from this current was shown to 'melt' the polypropylene part of the clips used to electrically contact the wafer. Although the magnitude of the current could be reduced by having several clips along one side of the wafer, this would complicate the process and result in increased wafer handling. For this reason it was decided to investigate whether it was possible to apply lessons learned through the development of LIP processes to develop a LIA process. This chapter reports on the development on this new process. Initial experiments focussed on the anodisation of silicon in order to investigate the relationship between anodisation conditions and oxide growth, because the presence of intervening SiO_2 in the case of aluminium anodisation complicates the characterisation. Furthermore, the ability to form anodic SiO_2 has many possible applications in silicon PV.

This chapter begins with a review of existing anodisation techniques, in which the limitations of each technique are identified. Then it describes the development of the LIA method that enables uniform anodic SiO_2 formation on large areas. The focus moves then to investigating the use of LIA to uniformly anodise *p*-type silicon surfaces for surface passivation. The mechanism of anodic SiO_2 growth as well as its physical and electrical properties is reported. Finally, potential applications of the anodic SiO_2 in silicon PV are evaluated and discussed.

5.2 Anodisation Techniques

This section reviews three existing anodisation techniques which can be applied to anodise a silicon surface, in order to identify their advantages and limitations. These methods are:

- Clip anodisation of silicon where anodisation proceeds from one or more points and the anode contacts the substrate to be anodised using a conductive clip;
- Photo-induced preferential anodisation (PIPA) which uses the light-induced current from a pn junction device to anodise the *p*-type surface; and
- Field-induced anodisation (FIA) which can be used to anodise *n*-type surfaces of pn-junction devices.

5.2.1 Clip Anodisation

Anodic formation of oxide films on silicon wafers was first studied by Schmidt and Michel in 1957 [266]. The oxide was formed by anodising a silicon surface in concentrated HNO_3, concentrated H_3PO_4 and in N-methylacetamide under constant current density. Anodisation was performed using arrangements very similar to those used to anodise metal, where a DC bias was applied through conductive clips that electrically contacted the wafer (anode) and a platinum cathode, both electrodes being immersed in an electrolyte which was magnetically stirred during anodisation with its temperature being controlled by a thermostat (see Figure 5-1). The silicon wafer in this case was fully-immersed in the electrolyte with electrical contact achieved using a special treated tantalum electrode, which was previously oxidised at 300 V [115].

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 5-1 Schematic diagram of the single compartment cell used to anodise silicon in [115].

This clip anodisation arrangement became the most commonly used technique for forming silicon oxides by anodising silicon surfaces. The advantages of the method include: (i) mechanically simple to perform; and (ii) oxidation is achieved on both surfaces of the silicon wafer instantaneously [267]. Moreover, when multiple anodes are in use, as shown in Figure 5-1, a number of wafers can be anodised in one batch.

However, there are also distinct disadvantages in terms of the physical and electrical quality of the grown anodic oxides, especially for solar applications. Usually

the clips cannot contact the electrolyte, because otherwise the electrochemical circuit will be shorted, bypassing the anodisation circuit. Consequently, a fraction of the wafer that is in contact with the clip remains un-anodised, which is undesirable when the grown oxide is to be used as a surface passivation layer for silicon solar cells. Although a fully-immersed arrangement as shown in Figure 5-1 helps to mitigate the issue of leaving an un-anodised area, the pre-treated tantalum clips used in this case are very expensive and the wafer surfaces in contact with the clips still remain un-anodised. Furthermore, the bias voltage applied through a conductive clip at one side of the wafer generates a gradient of potential across the wafer. This potential gradient varies the oxidation rate and results in non-uniform anodisation. The extent of this non-uniformity depends on the wafer resistivity. Figure 5-2 shows the open circuit PL images of silicon wafers passivated by clip anodisation grown anodic SiO_2 and thermal SiO_2. Figure 5-2 (a) shows that the effective carrier lifetime degrades from the area close to the clip (white line) to area further away from the clip. Last but not least, as the wafer thickness decreases, the mechanical force induced by the clip contact scheme is likely to result in lower processing yields with increased wafer breakage.

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Figure 5-2 Open circuit PL images of: (a) an anodic SiO_2 passivated silicon wafer; and (b) a thermally-oxidised silicon wafer. The white line in (a) represents the interface of the immersed and non-immersed part of wafer (reproduced from [267]).

5.2.2 Photo-Induced Preferential Anodisation

In 1992, Yoshida *et al.* reported the PIPA technique in which localised *p*-type silicon regions in an *n*-type silicon surface are preferentially anodised in aqueous HF under illumination [268] as shown in Figure 5-3. The light-induced current resulted in an anodic *p*-type surface and a cathodic *n*-type surface, with external current flowing through the HF solution and making a closed electrochemical circuit. The oxidised *p*-type silicon was then dissolved in the HF exposing further *p*-type silicon to be anodised. The reaction continues until the *p*-type region is removed (i.e., completely anodised and then subsequently dissolved). The selective oxidising and removing of *p*-type regions was found to be beneficial in micromechanical fabrication [268].

In PIPA the potential for generating an anodisation current is created by the pn-junction rather than a bias voltage provided via a metal electrode (e.g., a conductive

clip). Consequently the wafer cannot be contaminated with metallic ions released from electrodes. Moreover, by engineering the location and size of the *p*-type regions, only the *p*-type regions are anodised and they are anodised at the same time.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 5-3 Schematic diagram showing the PIPA technique [268].

Despite the advantages of PIPA compared to clip anodisation, it was originally designed for the purpose of micromechanical fabrication, hence there were many limitations hindering its application to anodising silicon surfaces for solar cells. First, the *p*-type silicon acts as a sacrificial layer in the process of PIPA, being anodised and the subsequently dissolved in the aqueous HF. Although Yoshida *et al.* showed that the etching of the anodised silicon could be suppressed by using a high HF concentration and weak light intensity, the anodised silicon was porous and therefore would not be suitable for use as an impervious passivating dielectric layer. Second, as the substrate was fully-immersed in the electrolyte, applying a bias voltage or current was not possible. Consequently the anodisation current density was determined by the voltage of the pn-junction and the interfacial potentials at the *p*-type and *n*-type silicon surfaces with respect to the electrolyte. According to [268]:

$$J_L = \frac{(V - \phi_n - \phi_p)}{R_L} \tag{5.1}$$

where J_L is the light-induced current density, V is the operating voltage of pn-junction, ϕ_n interfacial potentials between the *n*-type silicon and electrolyte and ϕ_p interfacial potentials between *p*-type silicon and electrolyte, and R_L load resistance (Ω cm^2) in the circuit. The anodic oxide growth rate was positively correlated to the positive charge delivered to the *p*-type surface and hence J_L. Therefore the variation in anodisation rate between samples can be significant because V, ϕ_n and ϕ_p would all vary with the dopant concentration in silicon and R_L would depend on the type and concentration of electrolyte.

In summary, the PIPA technique creatively utilises the photovoltaic effect of a pn-junction cell to achieve self-limited anodisation of *p*-type silicon without the requirement of contacting metal electrodes. However, the anodised *p*-type silicon is eventually dissolved in the electrolyte and so the method cannot be used for the

formation of high quality dielectric layers that can be used to passivate silicon surfaces. Furthermore, there is limited control over the anodisation rate as that is determined by properties of the silicon doping concentration and electrolyte.

5.2.3 Field-Induced Anodisation

Field-induced anodisation was developed in parallel with the work of this thesis in order to grow anodic oxides on the *n*-type silicon surfaces. It is first reported by Lennon *et al.* [269], which involves forward-biasing a solar cell such that the *n*-type surface becomes anodic and anodising the aluminium layer deposited on that surface. Figure 5-4 shows the schematic diagram of the FIA technique. In FIA, only the wafer's *n*-type surface is in contact with the electrolyte. The pn-junction is forward-biased by a DC voltage applied on the *p*-type surface (with respect to the cathode). Passivation dielectrics on the *p*-type surface are usually patterned by laser to enable electric contact.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 5-4 Schematic depiction of the FIA process for anodisation of aluminium (reproduced from [269]).

Schottky diodes, and hence depletion regions, can potentially form at both the *n*-type and *p*-type silicon surfaces due to the work function mismatch [270]. It was shown that heavy doping was required at both the *n*-type and *p*-type surface to reduce the resistive loss and increase the anodisation rate. The Schottky diode effect in FIA can also be addressed by applying illumination to generate a photo current in the depletion regions at the interfaces, which flows out of the depletion region by applied bias [270]. Although initially demonstrated to anodising aluminium, FIA can potentially be used to anodise silicon and grow anodic SiO_2 on *n*-type silicon surfaces.

One of the notable drawbacks of the FIA technique is that the anodisation rate and uniformity of oxide thickness are sensitive to the placement of the electrode on the *p*-type surface. Because local doping/patterning is required to reduce the Schottky diode, the current may flow directly from these patterned areas to the *n*-type surface, causing a variation in the anodisation rate. Therefore the pattern on the *p*-type surface, such as line or point spacing, needs to be specially designed to mitigate this non-uniformity. Alternatively, FIA can be formed using a thin oxide layer under the electrode, with the current tunnelling through this layer to enter the silicon.

5.3 Development of Light-Induced Anodisation

As discussed in Section 4.5.3 and Section 0, the limitations of the conventional clip anodisation in respect to the formation of passivating dielectric layers for silicon PV applications can be summarised as: (i) part of the substrate remains un-anodised due to contact with the conductive clip; (ii) a potential gradient across the wafer results in non-uniform anodisation, a problem that is exacerbated with the use of larger (e.g., 156 mm × 156 mm) wafers; and (iii) localised mechanical pressure from the clip causes wafer breakage especially for thin wafers. Although the PIPA technique eliminates the metal electrode contact by using photovoltaic effect of the pn-junction, its application is hindered by: (iv) the dissolution of or introduction of porosity in the formed anodic oxide which is required for sustained anodisation; and (v) the inability to control the anodisation voltage or current thus providing little control over anodic oxide growth rate.

These limitations restrict the use of anodic oxidation in silicon PV applications. In order to be viable in commercial production, anodisation needs to be performed on industrial-sized wafers, at high throughput with high yield. The formed oxides should be of uniform thickness and n_r. This section introduces the LIA method which combines the advantages of both clip anodisation and PIPA, by utilising the photovoltaic effect of a pn-junction solar cell and the application of a bias voltage to anodise *p*-type silicon surfaces. It addresses many of the five limitations of the above mentioned anodisation techniques.

5.3.1 Single-Side Contact Scheme

One of the novel aspects of LIA over the PIPA technique is the use of a single-side contact scheme, with only the *p*-type surface contacting the electrolyte, such that a bias voltage or current can be applied to the silicon wafer on the other surface. A schematic diagram of the apparatus designed for LIA is shown in Figure 5-5. In this arrangement the wafer is supported by a holder and stays about 2 mm above the air/electrolyte interface, with *p*-type surface facing the electrolyte. Wetting of the *p*-type surface is initiated by locally contacting the electrolyte with the surface (e.g., by agitation of the electrolyte). Then due to surface tension, wetting of the *p*-type surface extends outwards from the contact point until the entire surface is in contact with the electrolyte. With this single-side contact, only the surface to be anodised is in contact

with the electrolyte, while the other surface (*n*-type surface) is kept dry during anodisation to allow electrical contact and application of a bias voltage.

The single-side contact addresses the first and third limitation mentioned above by eliminating the use of metal clips. There is no local mechanical stress from the clip and the full area of *p*-type surface is anodised. The ability to apply a bias through the anode to control the anodisation rate also addresses one of the main drawbacks of PIPA.

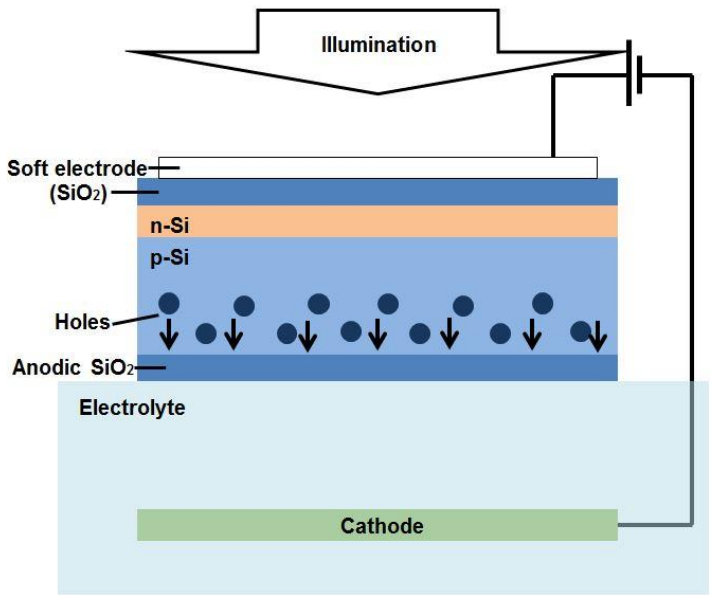

Figure 5-5 Schematic diagram of apparatus for LIA of silicon.

5.3.2 Anode Contact Design

In PIPA, the *n*-type silicon acts as cathode of the electrochemical circuit. However, a separate cathode is used in LIA and a bias voltage is applied between the anode and the cathode. An anode contact was designed to contact the *n*-type silicon surface so that it was: (i) electrically conductive; (ii) transparent to the used light source; and (iii) soft and does not scratch the silicon wafer surface. Although the resistivity of conductive rubbers can be as low as 0.008 Ω cm for military and aerospace grade silver/copper silicon conductive rubber [271], these rubbers are typically opaque to visible light and of very high cost. Graphite, with a resistivity along the hexagonal axis about 1 Ω cm [272] and low material cost, was considered a viable alternative. Although graphite is not transparent, it can be trimmed into grids, such that light passes through the open regions and the graphite strips provides electrical contact. Finally extended graphite, in the form of graphite foils or mats, is soft and flexible. It does not

damage the silicon surface if it is compressed to or moved across the surface. This is especially advantageous, as the *n*-type emitter surface is the illuminated surface of *p*-type silicon solar cells and any process-induced surface damage may limit the cell performance. Consequently graphite was selected as the material for the anode contact in the experiments reported in this thesis. In the long term, graphite may not be the ideal material as it can degrade with use as an electrode, with sheets of graphite exfoliating on the silicon surface after frequent use. Although this exfoliation does not impact the anodised cells as the exfoliated material is simply rinsed off, alternative soft contact materials with longer effective working lifetimes would be desirable.

5.3.3 Constant DC Potential

Anodic SiO_2 can be formed using either constant current density or constant potential or combination of both. Earlier reported studies on anodic oxide formation typically used constant current density mode to maximise process control [115, 266]. By controlling the current, the quantity of charges delivered to the anode can be accurately determined. However, the increased oxide thickness raises the resistance of the ionic current flow, which increases the bias voltage. In some cases, the voltage is as high as 560 V [266], which requires a high voltage power supply and excessive safety protection. Application of very high voltages may also cause oxide breakdown, resulting in damage to the oxide [266].

A combination of current and constant potential control was used in [273, 274], where a three-step anodisation process was reported. First, the current was exactly zero; second, the current increased linearly at a rate of 0.5 mA cm^{-2} min^{-1}; and third, once the voltage had increased significantly, a voltage limiter maintained a constant voltage across the anode and cathode until an anodic SiO_2 of desired thickness was formed. The reason for using the combined current and voltage control was not explained, however the requirement for a programmable power supply adds complexity to the system design, therefore three-step anodisation was not considered in this thesis.

Under constant potential, the anodisation current will gradually reduce with increased oxide thickness because of the increased resistance experienced by the ionic current. Due to the reduced current, the time required for anodic oxide growth of the same thickness is longer. However since the constant potential can be controlled within the safety regulations of the laboratory, it was preferable for the anodisation experiments reported in this thesis.

5.3.4 Illumination

The LIA process addresses the second limitation raised at the beginning of Section 5.3 by utilising the light-induced current of the pn-junction under illumination. A built in potential is created across the junction resulting in electrons accumulating at the *n*-type surface and holes accumulating at the *p*-type surface. This means that a uniform current can be delivered to the *p*-type surface irrespective of the size of the wafer. As mentioned in Section 0, this cannot be achieved using clip anodisation due to the high resistivity of silicon wafers, and therefore it represents a major advantage of LIA over previously reported methods of anodisation of *p*-type surfaces.

The idea of using the light-induced current to assist anodisation arose from the LIP process [275, 276]. Figure 5-6 illustrates the equivalent circuit for a non-contact LIP process. In the plating bath, the *n*-type surface acts as a cathode, where metal ions, such as Ni^{+} and Cu^{2+}, accept electrons and are reduced on exposed regions of the silicon surface [229]. Simultaneously, the aluminium layer on the *p*-type surface acts as a sacrificial anode in the plating bath, which is anodised and dissolved.

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Figure 5-6 Equivalent circuit for non-contact LIP showing the solar cell in an electrochemical circuit with the plating electrolyte [229].

In LIA, the reactions in the electrochemical circuit occur at the anode, with the light-induced current deliberately used for anodising the *p*-type surface of silicon wafer. The cathode is replaced by a metal plate where hydrogen ions are reduced to hydrogen gas. In the experiments performed in this chapter, an array of nine compact fluorescent light bulbs with total power of 180 W and 6500 K colour temperature were used as the light source. The light intensity was adjusted by altering the distance between the light source and wafer. The maximum light intensity delivered to the wafer surface was 150 W m^{-2}. This intensity was achieved when the wafer was located a distance of 5 cm from the light source. Alternative light sources, such as xenon lamps, halogen lamps and high power white light emitting diode (LED) are also applicable though were not tested in this thesis.

5.3.5 Bias Voltage

Although anodisation can occur during non-contact LIP, the process is not controllable and anodisation rate is very low due to the small anodisation current. Furthermore, once a thin oxide forms on the *p*-type surface, the metal plating rate would significantly decrease as the resistances in the electrochemical circuit are too large to sustain a metal plating reaction.

Figure 5-7 depicts the equivalent circuit of LIA, showing the resistive components in the circuit. From the *n*-type to *p*-type surface, there are anode contact resistance R_c, cell series resistance (R_s), and varying oxide resistance (R_o) in the formed anodic SiO_2. Moreover, the ohmic resistance of the solution (R_Ω) and the interfacial potentials (ϕ) at the anode/electrolyte and cathode/electrolyte interfaces are in series with all other resistances. The interfacial potential ϕ can be represented as a charge-transfer resistance (R_{CT}) in parallel with a capacitance (C_{DL}) using a Randles equivalent circuit model [277]. Therefore, the total load resistance (R_L) in the electrochemical circuit is usually very high, such that only a very low current less than 100 µA is generated by potential created by illumination of the cell. The low current results in a very low anodic SiO_2 growth rate that is difficult to measure with acceptable accuracy.

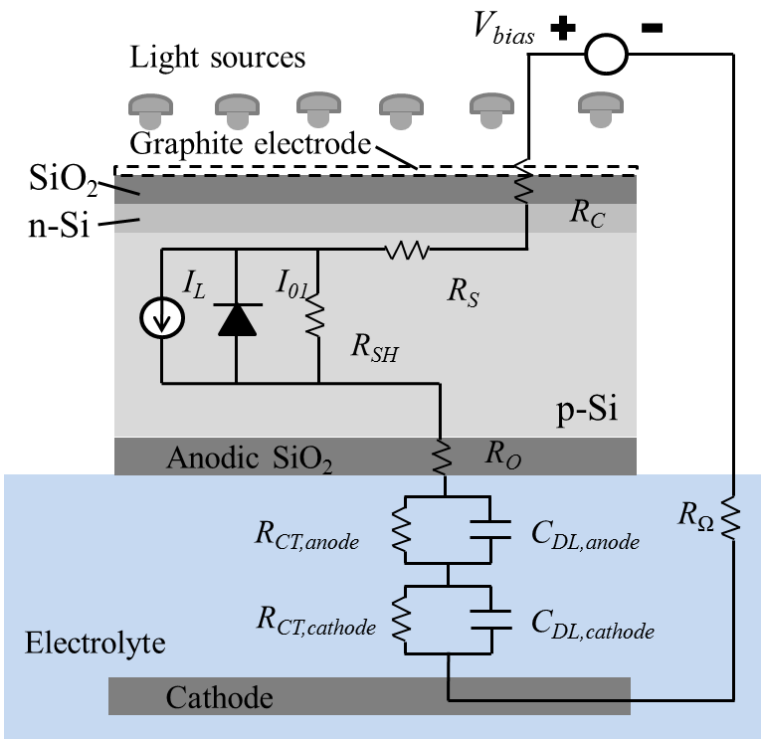

Figure 5-7 Equivalent circuit for LIA showing the solar cell in an electrochemical circuit with the electrolyte.

Therefore, the key to realise LIA is to use a bias voltage to offset the load resistance in the electrochemical circuit. Figure 5-8 shows an *I-V* curve and the operating point of the pn-junction under different bias conditions in LIA. The analysis has been simplified by assuming that the load on the cell is dominated by the interface potentials, collectively represented by ϕ, which is assumed not to depend on the cell voltage (V_{cell}). In other words, ϕ is large with respect to the voltage drop due to R_{Ω}. The operating point is determined by V_{cell}, the bias voltage (V_{bias}), ϕ and the above mentioned R_L. If $V_{cell} < (V_{bias}-\phi)$, there is no anodisation current flowing to the *p*-type surface and hence no anodisation will occur. It is notable that without V_{bias}, the V_{cell} may be smaller than ϕ and hence anodisation will not occur. When $V_{cell} > (V_{bias}-\phi)$, current flows though the p-type surface and anodise the silicon at that surface. The operating point is then determined by the intersection of the load current curve and the *I-V* curve of the pn-junction. As the anodic oxide growth rate is proportional to the anodisation current density [268, 278], a higher V_{bias} is desirable for anodisation as it results in the operating point of the cell being close to short circuit conditions (point A in Figure 5-8), therefore a higher anodisation current results. When the V_{bias} is low, or zero, the operating point will be close to open circuit (point B in Figure 5-8) due to the large R_L in the electrochemical circuit, which leads to a very low anodisation current.

Although a very large reverse V_{bias} can also make the *p*-type surface anodic and initiate anodic SiO_2 formation on that surface, it was found that the junction non-uniformly entered reverse breakdown resulting in non-uniform anodisation and reduced τ_{eff} of the cell. Therefore, the bias voltage should be selected such that the pn-junction operates in the first quadrant of the pn-junction *I-V* curve, not in the reverse bias.

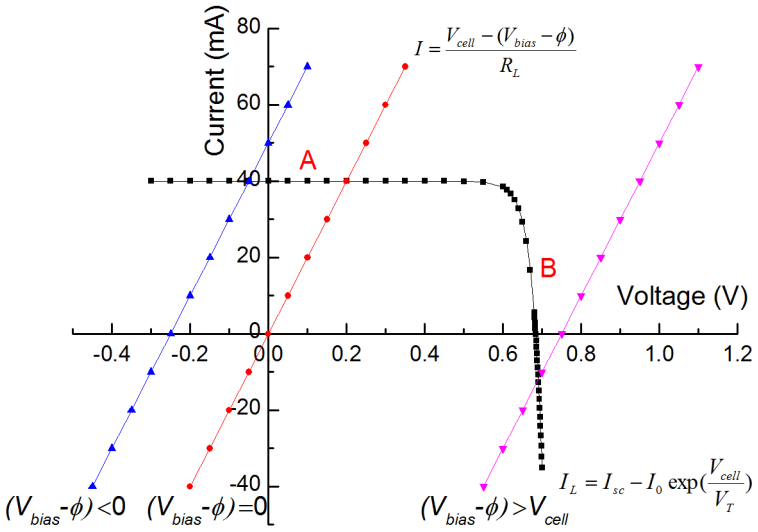

Figure 5-8 *I-V* characteristic of a pn-junction during LIA under different bias conditions, V_{bias}. Point A indicates the preferable operating point of LIA. Point B shows the operating point when insufficient or no V_{bias} is applied. Note, this simplified analysis assumes that ϕ and R_L are constants which will not be the case as they will change with as the oxide thickness increases.

The uniformity of the anodic SiO_2 is further improved by the fact that the anodisation current is flowing in a direction perpendicular to the silicon wafer surface. It is more effective because the *p*-type surface becomes equal potential regardless of the bulk resistivity. Furthermore, the through-wafer current flow is not disrupted by the surface roughness of the wafer surface and hence mitigates the variation between different wafer surfaces (e.g., polished, planar or textured). This differs from clip anodisation where the current flows in a direction that is parallel to the wafer surface.

The bias voltage was provided by a dual-track DC power supply (Instek SPS-1820). In constant voltage operation, the output voltage was adjusted from 0 to 18 V with continuous adjustment. The voltage ripple and noise were less than 5 mV_{rms} and 100 mV_{p-p}, respectively. Bias voltages exceeding 18 V were realised by connecting two power supplies in series. Anodisation current was measured by a built-in amp meter on the DC power supply. The resolution of the current reading was then improved to 100 µA by using a multi-functional amp meter and data logger (Hantek 365A) connected in series in the anodisation circuit. A further improvement in the process control could be realised by using a high precision potentiostat with a reference electrode (see Figure 5-9), with which the V_{bias} between anode and the electrolyte could be determined, rather than the V_{bias} between anode and cathode in the arrangement used for the experiments reported in this thesis.

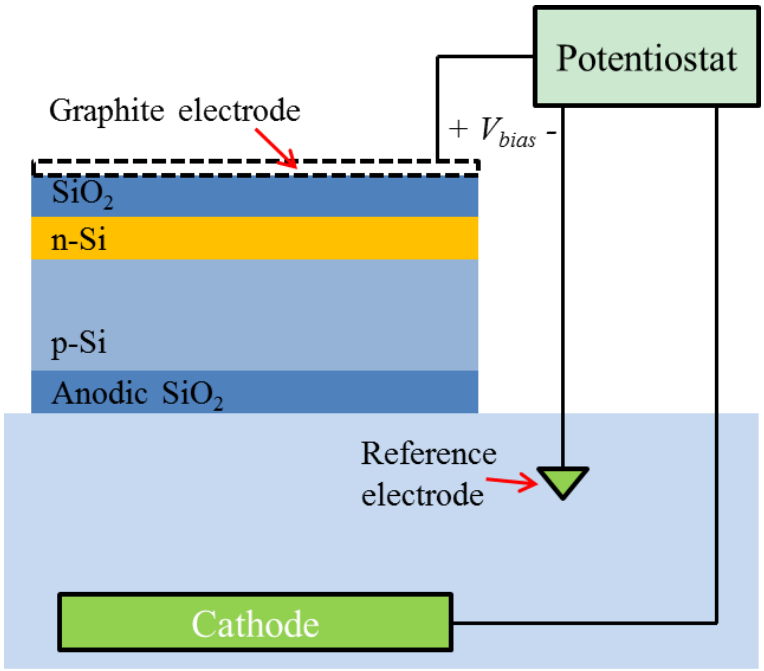

Figure 5-9 Schematic diagram showing the anodisation circuit using a potentiaostat. The V_{bias} is applied to the *n*-type surface with respect to the electrolyte rather than the cathode.

5.3.6 Cathode Material Selection

In the electrochemical circuit of LIA, the cathode is preferably inert. Inert metals such as platinum and palladium are ideal because they do not corrode in most anodisation electrolytes and therefore minimise metal contamination of the electrolyte. However the high cost of these precious metals made them undesirable for use in this work. Nickel was used as the cathode in the experiments performed for this thesis as it is a low cost metal that has reasonable corrosion resistance. Electroless nickel is widely used as a barrier-coating to protect metal parts from the corrosion in alkali, salt, organic and inorganic acids, with the only exception being strong oxidising agents. In the experiments reported in this chapter, electronic grade 0.5 M H_2SO_4 (J.T. Baker) was used as the electrolyte. At RT, H_2SO_4 is a reducing acid when its concentration is less than 16 M. The corrosion rate of nickel in diluted H_2SO_4 is reported to be as low as 28 µm per year [279, 280], which is negligible in the time scale of the anodisation process. The rate can be even slower in the anodisation circuit as the electrode is under cathodic potential during anodisation. In order to minimise any chance of contamination, the electrolyte was refreshed after anodising every eight wafer fragments (40 mm × 40 mm), to maintain the reproducibility of the experiments.

5.3.7 Potential Problems

5.3.7.1 Front Surface Wetting

Ideally the *n*-type silicon surface remains dry during LIA to avoid anodising the graphite electrode, which can cause electrode aging and reduced electrode efficiency. Although the *p*-type contact with the electrolyte is enabled by surface tension with the wafer being ~ 2 mm above the air/electrolyte interface, front surface wetting still occurred under some circumstances. The two main causes of front-surface wetting were: (i) the position of the cathode; and (ii) the wetting properties on the *n*-type silicon surface. During anodisation, hydrogen ions are reduced at the cathode resulting in hydrogen formation. Consequently, if the cathode is too close to the wafer or under the wafer (as depicted in Figure 5-7), the generated hydrogen bubbles can agitate the electrolyte and cause wetting of the edge of *n*-type wafer surfaces. If the *n*-type surface is covered by a hydrophilic dielectric (e.g., SiN_x and SiO_2) once the edge of the dielectric is wetted, the electrolyte spreads inwards and can wet larger areas of the *n*-type surface (even under the graphite electrode).

The front surface wetting can be minimised by placing the cathode further away from the wafer or to the side of the wafer, where effusion of gas does not disturb the anodisation process. If the cathode is at the bottom of the bath, a fine isolation net can be used between the wafer and the cathode to reduce the interference of hydrogen effusion to the process. Finally, for wafers with hydrophilic dielectrics on the *n*-type surface, the distance from wafer to air/electrolyte interface can be further increased provided complete wetting of the *p*-type wafer surface is achieved.

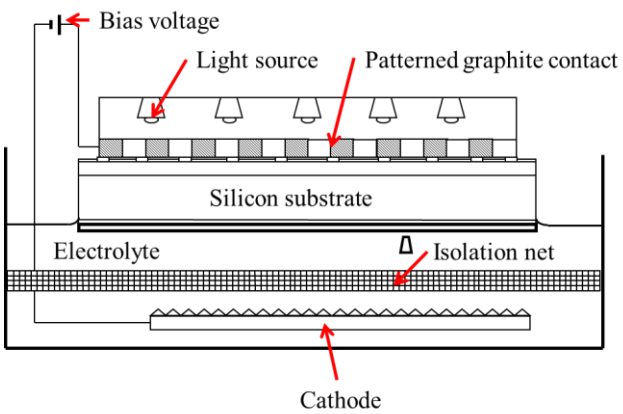

Figure 5-10 Schematic diagram of LIA apparatus with cathode located at the bottom of the bath. An isolation net is shown placed between the wafer and the cathode to minimise the electrolyte agitation of hydrogen bubbles generated at the cathode (reproduced from [281]).

5.3.7.2 Variation in Anodic SiO_2 Growth Rate

The anodic SiO_2 growth rate depends on the anodisation current density, which is determined by the voltages and resistance in the electrochemical circuit under constant bias voltage. A major contributor to the variation in R_L is the R_c between the graphite electrode and the *n*-type surface. It depends on the thickness of dielectric layer on that surface and the condition of the graphite electrode. If the graphite is erroneously oxidised then its resistance can be significantly increased resulting in a low anodisation current density and low anodic SiO_2 growth rate.

To minimise variations in growth rate, the anodisation current density and the quality of the graphite electrode needed to be monitored such that current variation was maintained at less than 5% for wafers with the same size, bulk doping and emitter sheet resistance. Alternatively, anodisation with constant current density eliminates the variation caused by varied total series resistance. However, in order to maintain the constant current, the anodisation voltage increases with increased thickness of anodic SiO_2, resulting in voltages higher than the safety regulation in the lab as discussed previously in Section 5.3.3.

5.3.8 Summary

This section described the development of a LIA method which can be used to anodise *p*-type silicon surfaces thus forming anodic SiO_2 layers. The LIA process is a non-vacuum and RT process that significantly reduces the thermal budget for oxide growth. It does not require specific wafer cleaning procedures such as the RCA clean [217] which are critical for thermal oxidation. Furthermore, the process uses commonly-available chemicals such as diluted H_2SO_4, making it a potentially low-cost alternative to thermal oxidation. The range of standard anodisation parameters that were investigated in these initial experiments are summarised in Table 5-1.

Table 5-1 Range of standard operating parameters of LIA

Parameters	Values
Light Intensity	33-1000 W m^{-2}
Bias Voltage	10-25 V
Electrolyte	0.5 M H_2SO_4
Electrolyte pH	0.3
Electrolyte Temperature	25 °C

5.4 Anodic SiO_2 by Light-Induced Anodisation

This section reports on experiments which examined the properties of anodic SiO_2 layers formed using LIA. Initial studies investigated the effect of illumination and bias voltage on anodic SiO_2 growth. Attention is then paid to the mechanism of anodic SiO_2 growth and the control of the process.

5.4.1 Effect of Illumination

Illumination plays an important role in the LIA process as it generates the light-induced current uniformly across the wafer, which is essential for uniform growth of anodic SiO_2. The experiments reported in this section investigated the effect of illumination on anodic SiO_2 growth.

5.4.1.1 Experimental

Double-side polished *p*-type 1 - 10 Ω cm Cz silicon wafer fragments (40 mm × 40 mm) of thickness of 190 µm were phosphorus-diffused to form 100 Ω/□ emitters. The phosphosilicate glass was removed using 1% (w/v) HF, and then the rear emitter was removed by immersing the wafers in 'Trilogy Etch' [221] for 5 min while the emitter surface was protected by FSC-M novolac resin surface coating (Shipley Company Inc.). As depicted in Figure 5-11, a thermal oxide layer of 17 ± 1 nm thickness was formed by dry oxidation at 980 °C for 18 min in a quartz tube furnace. After oxidation wafers were single-side dipped in 1% (w/v) HF for 2 min to remove any native oxide on the *p*-type wafer surface before LIA.

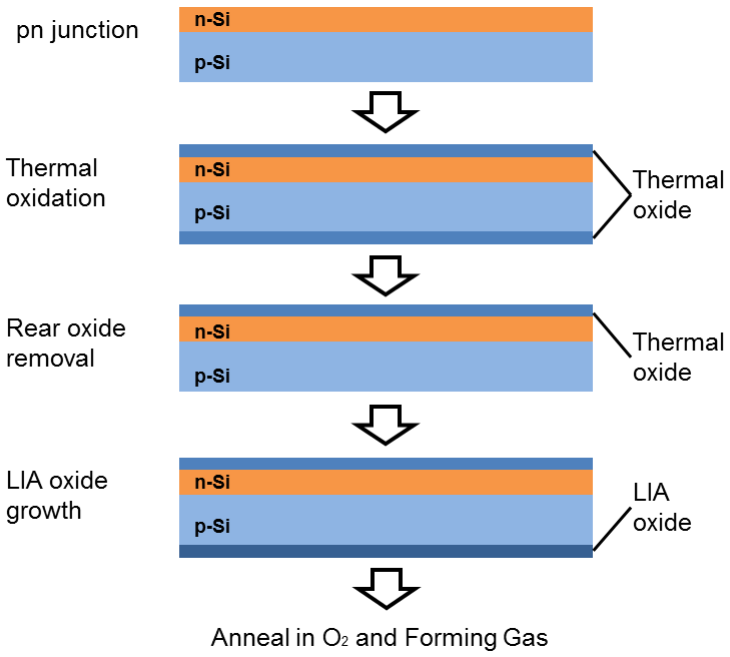

Figure 5-11 Process flow for sample preparation.

Two wafers were prepared following the above mentioned procedure. Both wafers were anodised with 15 V bias voltages. One wafer was illuminated with a light intensity of 150 W m^{-2}, while the other wafer was anodised without illumination. The ambient light had an intensity of less than 2 W m^{-2} on the wafer surface, which corresponded to ~ 2 mA current difference and therefore had negligible impact on the anodisation process. Consequently, the anodisation performed with ambient light was considered as anodisation without illumination. During anodisation, the current-time (*I-t*) curve was recorded by a data logger that was connected in series in the electrochemical circuit. After LIA, wafers were rinsed in DI water to remove traces of electrolyte and then dried under nitrogen.

5.4.1.2 Results and Discussion

Figure 5-12 compares the anodisation current of the wafers anodised with and without illumination. The current of the wafer anodised with illumination started simultaneously at 60 mA once the bias voltage was applied and decreased exponentially with time, which was in good agreement with the *I-t* characteristic formation of a barrier layer type anodic oxide [278]. Without illumination, the current became unstable. This was partially because the anodisation current without light was solely from the drift current when the pn-junction was operating in the reverse bias, as discussed in Section 5.3.5. The bias was applied using a patterned graphite electrode as described in Section

5.3.2. Consequently the electric field may have varied across the wafer resulting in non-uniform pn-junction breakdown and hence non-uniform current flow through the device. This result demonstrated that light-generated current of the cell enabled current flow in the electrochemical circuit.

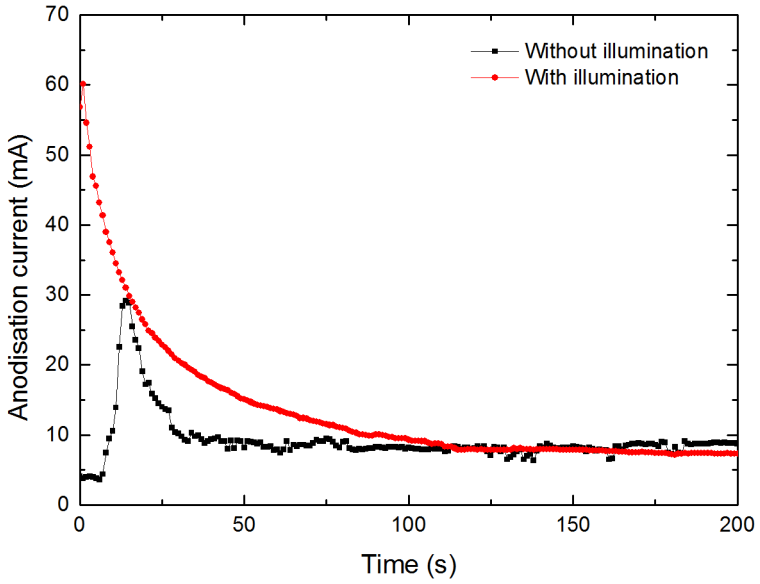

Figure 5-12 Anodisation current graphed as a function of time for a wafer anodised with (red circles) and without (black squares) illumination. The bias voltage used was 15 V for both wafers and the illumination intensity was 150 W m^{-2} for the illuminated wafer.

5.4.2 Growth Rate and Effect of Bias Voltage

The 'Deal-Grove Model' [60] for thermal silicon oxidation assumes that the oxidation reaction occurs at the interface between the oxide and the silicon and is limited by: (i) transport of the oxidant from the ambient gas to the surface; (ii) transport of the oxidant across the oxide layer towards the silicon; and (iii) reaction at the silicon surface to form a new layer of silicon dioxide. This model predicts that the oxide thickness has a parabolic relationship with time. In the LIA process oxide growth is limited by three similar factors: (i) diffusion of the oxidant through the formed oxide layer; (ii) supply of positive charge at the silicon oxide interface; and (iii) reaction at the interface. Therefore, it was hypothesised that: (i) the oxide growth rate would be controlled by the anodisation current (and consequently the bias voltage and light intensity); and (ii) the formed oxide thickness would have a parabolic relationship with anodisation time.

This section reports on experiments which investigated the rate of anodic SiO_2 growth as a function of anodisation time and bias voltage magnitude. Results were

compared to what is expected for growth of a thermal SiO_2. The effect of the bias voltage was also assessed.

5.4.2.1 Experimental

A batch of wafers was prepared according to procedure described in Section 5.4.1.1 up to the anodisation step. Then wafers were sorted into four groups with three wafers in each group and were anodised with 10 V to 25 V bias voltages. The illumination intensity for all wafers was 150 W m^{-2}. The anodisation current was recorded by the data logger with 1 or 5 s intervals then integrated with respect to time to estimate the total charge, Q_{total}, delivered to the anode using:

$$Q_{total} = \int I(t)dt\,, \tag{5.2}$$

where $I(t)$ is the anodisation current as a function of t. Assuming 100% reaction efficiency of the anodisation process, Q_{total} can be converted to the ideal thickness of anodic oxide by:

$$t_{ideal} = \frac{Q_{total}}{4 \times q} \times \frac{M}{6.02 \times 10^{23}} \times \frac{1}{\rho} \times \frac{1}{A} \tag{5.3}$$

where q is the charge of an electron, M molar mass, ρ density of the anodic SiO_2 and A total wafer area. The value of ρ was assumed to be the same as for a thermal SiO_2 (2.20 g cm^{-3} [282]). The anodic oxide thickness was measured using an ellipsometer (M-2000VI, J.A Woollam Co., Inc.).

5.4.2.2 Results and Discussion

Figure 5-13 shows Q_{total} graphed as a function of $t^{1/2}$ for the different bias voltages. At least for the lower bias voltages, the relationship between Q_{total} (t_{ideal} according Equation 5.3) and $t^{1/2}$ appears to be linear as predicted by the Deal-Grove model. The slope of the curve was an indication of the oxide growth rate, increasing with bias voltage as was expected from Faraday's law.

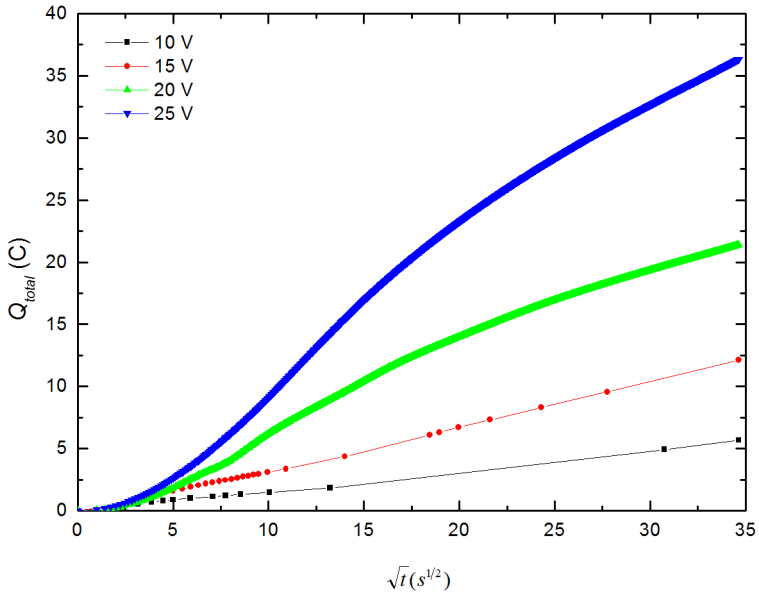

Figure 5-13 Graph of the total charge delivered to the anode during anodisation, Q_{total} as the function of $t^{1/2}$. Data for the 20 and 25 V bias conditions were recorded using a data logger with 1 s interval between sequential current readings.

Figure 5-14 compares the oxide thickness after 20 min anodisation, calculated from Equation 5.3, to the thickness of the oxide layer measured by ellipsometer. For each 16 cm^2 wafer, the thickness was measured at four locations over the surface to assess the uniformity of the layer. The variation increased with increasing thickness of the oxide, with the standard deviation for the 79 nm anodic SiO_2 being 1.1 nm.

As expected from Faraday's Law the measured oxide thickness increased with bias voltage. The efficiency of the anodisation process, estimated by the ratio of measured oxide thickness to the t_{ideal}, decreased with increased bias voltage with the highest efficiency of 10.1%, occurring at a 10 V bias voltage. The relatively low efficiencies indicated that the majority of the charge delivered to the surface was consumed in other competing reactions (e.g., oxidation of water at the anode) instead of anodising silicon. The competing reaction rate was also positively correlated to the bias voltage, therefore resulted in reduced efficiency at higher bias voltages. Moreover, the power loss due to R_s in the circuit was increased.

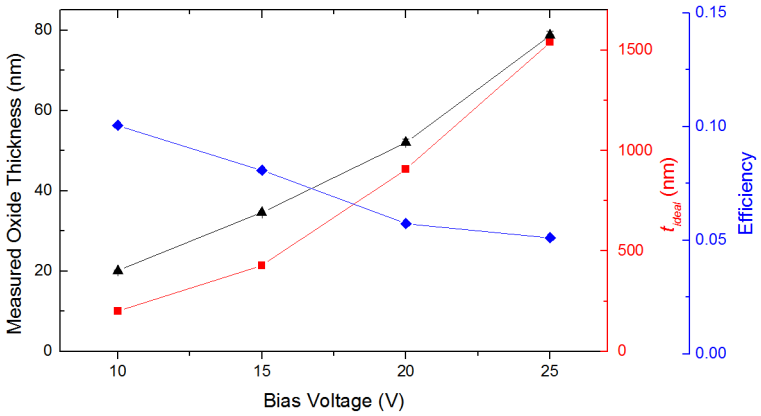

Figure 5-14 Measured LIA oxide thickness (black triangles) and the thickness calculated using Equation 5.3 (red squares) both in nm graphed as a function of bias voltage. The efficiency (blue diamonds) of the LIA process is calculated as a ratio of the two thicknesses (right axis). All wafers were anodised under 150 W m^{-2} illumination for 20 min.

5.5 Composition and Uniformity of Anodic SiO_2

This section reports on experiments which investigated the composition and the uniformity of the anodic SiO_2 formed by LIA. Composition of bonds and the depth profile of elements of the anodic SiO_2 are presented, followed by the analysis of uniformity in oxide thickness and n_r at a range of bias voltages.

5.5.1 Experimental

A batch of wafers was prepared as described in Section 5.4.1.1. After LIA, wafers were then annealed at 400 °C in oxygen and then forming gas for 30 min each as reported in [127]. Fourier transform infrared spectroscopy (FTIR) measurements were performed using FT-IR NICOLET 5700 (Thermo Electron Corporation) before and after annealing to compare the oxide composition. For all FTIR measurements, the same wafer substrate without any dielectric layers on its surfaces was used to establish a background. X-ray photoelectron spectroscopy (XPS) was performed using an ESCALAB250Xi instrument (Thermo Scientific) after annealing to investigate the depth profile of the anodic SiO_2 formed by LIA. The n_r of the formed anodic oxides was measured using an ellipsometer. A WVASE model was used to analyse the ellipsometry data. The anodic SiO_2 was modelled as a 200 µm silicon substrate and an effective medium approximation (EMA) layer consisting thermal SiO_2 and void. The fraction of void was to simulate the porous nature of thick anodic SiO_2. The thickness, n_r and fraction of the voids in the EMA layer were estimated using the model.

Uniformity was also examined using cross-sectional transmission electron microscopy (TEM).

5.5.2 Results and Discussion

Figure 5-15 shows the FTIR spectrum of the anodic SiO_2 formed by LIA on a double-sided polished *p*-type Si wafer with the bias voltage being varied from 10 to 25 V. For comparison, the spectrum of a thermal oxide that was grown on a similar wafer at a temperature of 980 °C is shown. The three characteristic IR absorption bands that occur at frequencies of 1075, 800 and 450 cm^{-1} correspond to the stretching, bending, and rocking motions, respectively, of twofold-coordinated oxygen atoms [261]. The frequency of the stretching band scales linearly with composition in SiO_2 from 940 cm^{-1} for a low concentration of oxygen in amorphous silicon to about 1075 cm^{-1} in stoichiometric SiO_2. Consequently, this stretching vibration provides a way of determining the extent to which deposited films approach stoichiometric SiO_2 [283]. Figure 5-15 demonstrates that the stretching motion is dominant in all cases and the location of the stretching peak is very close to 1075 cm^{-1} indicating that the formed oxide is very close to being stoichiometric for oxides formed at all bias voltage.

However, with closer inspection the stretching valley shifts from 1072 cm^{-1} when anodised at 10 V (15.5 nm) to 1068 cm^{-1} when anodised at 25 V (79 nm). Although this shift is small, it suggests that as the anodic oxide grows thicker it becomes less stoichiometric, with the x in SiO_x reducing from 2 with increased oxide thickness. Similar findings were reported Sigmon *et al.* [284] and Clark *et al.* [285].This effect may be explained by the mechanism of anodic oxide growth, where the oxidant from the acidic electrolyte diffuses through the formed oxide to the silicon/oxide interface to oxidise the silicon. When the thickness increases, the oxide becomes more resistant to oxidant diffusion, which can consequently result in a less dense oxide to maintain the ionic current flow.

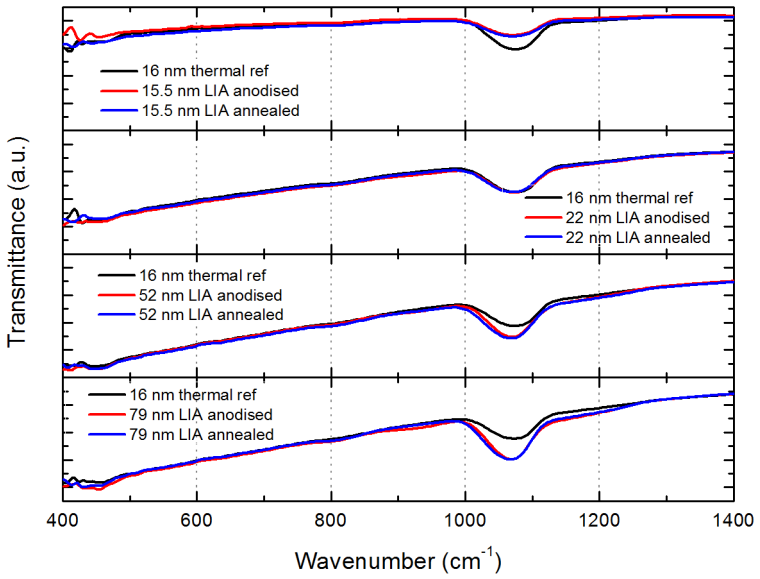

Figure 5-15 FTIR spectra of anodic oxides formed by LIA using different bias voltages. The bias and final oxide thickness are: (a) 10 V, 15.5 nm; (b) 15 V, 22 nm; (c) 20 V, 52 nm; and (d) 25 V, 79 nm.

Figure 5-16 depicts the XPS depth profile that was recorded for a wafer with: (a) 79 nm; and (b) 10 nm anodic SiO_2. The 'Si 2p ox' refers to silicon where the p orbitals electrons are bonded to oxygen atoms (i.e., oxidised) and 'Si 2p' represents the non-oxidised silicon where the p orbital electrons are bonded to other silicon atoms. The ratio of silicon to oxygen in the anodic oxide film was 1:1.7, which correlates with the shift of the stretching peak of the FTIR spectrum recorded for the anodic oxide film of similar thickness. The similarity of the silicon to oxygen ratio throughout the oxide film indicates the high uniformity of the oxide layer formed by the LIA method. There is a sharp transition at the interface from the silicon oxidised state to crystalline silicon. Suspected contaminants such as sulphur from the electrolyte and nickel from the cathode were not detected by XPS, however this may be due to the concentration of these possible impurities being lower than the detection limit of XPS which is 1×10^3 to 1×10^4 ppm [286].

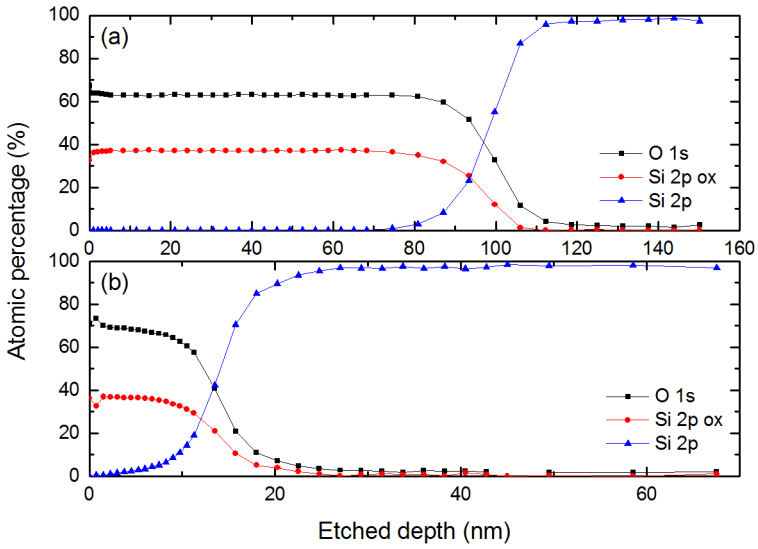

Figure 5-16 XPS depth profile of a 79 nm (a) and a 10 nm (b) thick anodic oxide formed by LIA under 150 W m^{-2} illumination, 25 V bias and 20 min of anodisation.

A similar trend was found with the n_r of the anodic oxide. As shown in Figure 5-17, when the oxide thickness increased from 20 to 79 nm, the n_r of anodic oxide decreased from 1.55 to 1.4, with the reference n_r of thermal oxide being 1.46 [282]. Normally, a porous SiO_2 film would have a lower n_r [287]. For the thicker oxide layers increasing the percentage of voids in the ellipsometry model resulted in a better fit of the measured data, an observation that was consistent with the decreased refraction index. The uniformity of the layer was further confirmed by TEM, with Figure 5-18 showing a cross-sectional image through a 79 nm thick anodic SiO_2 layer.

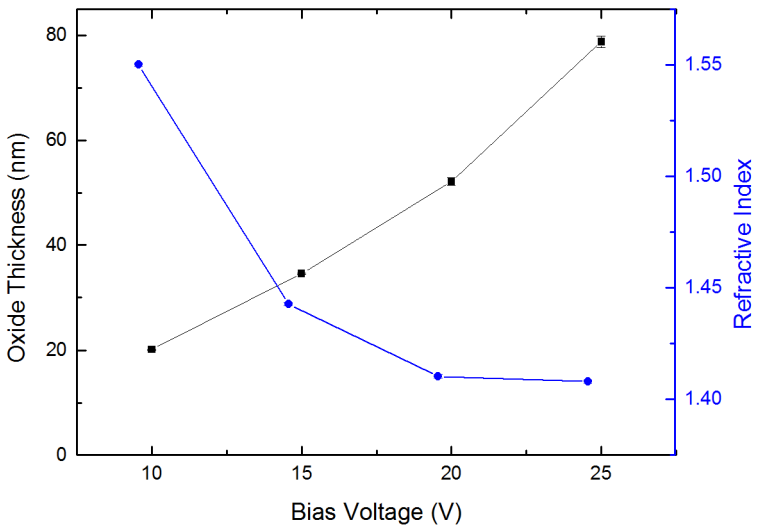

Figure 5-17 Thickness (black squares) and n_r (blue circles) of anodic oxide formed by LIA graphed as a function of bias voltage in a range from 10 to 25 V. The maximum percentage error of the oxide thickness and n_r are shown in

Table 5-2 because the error bars were too small with respect to the symbols.

Table 5-2 Maximum percentage error of the oxide thickness and n_r (measured by ellipsometry) of anodic oxide formed by LIA.

Bias voltage (V)	Thickness (nm)	Max. % error	n_r	Max. % error
10	20.1	1.2%	1.55	0.07%
15	34.6	1.0%	1.44	0.06%
20	52.1	1.6%	1.41	0.07%
25	78.7	1.0%	1.41	0.04%

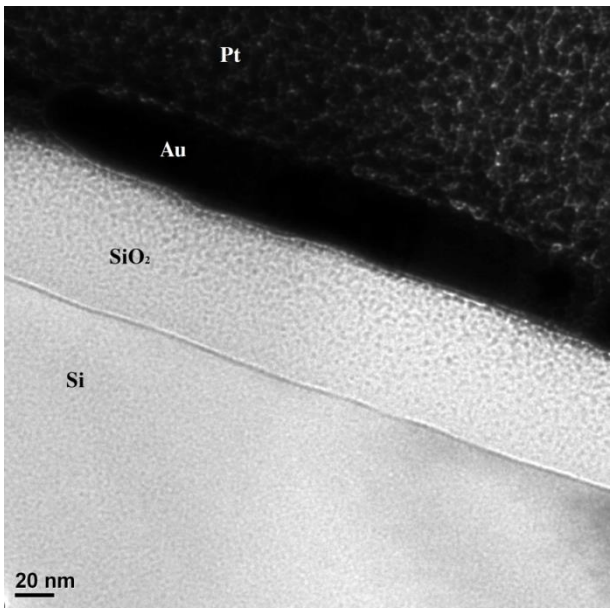

Figure 5-18 Cross-sectional TEM image of 79 nm anodic oxide formed by LIA, under 150 W m^{-2}, and a 25 V bias for 20 min.

5.5.3 Conclusions

It was demonstrated that 10 nm anodic SiO_2 layers formed by LIA were near stoichiometric. However, the layer became silicon rich from the thickness of approximately 25 nm and less dense with an increased layer thickness. Consequently, the n_r reduced from 1.55 to 1.4 in the range of 20 to 79 nm. The ellipsometry analysis showed the anodic SiO_2 layer is of high uniformity with the maximum percentage error of thickness and n_r of 1% and less than 0.1%, respectively.

5.6 Electrical Properties of Anodic SiO_2

Several low-temperature oxidation processes have been developed, which have resulted in effective surface passivation (see Table 5-3). The CVD techniques have

demonstrated *SRV*s less than 100 cm s^{-1}, however the reactors used in these deposition systems require a large amount of maintenance and the precursors used to form SiO_2 are both dangerous and expensive. Although a *SRV* as low as 42 cm s^{-1} have been reported using concentrated HNO_3, the advantage of a low temperature wet chemical oxidation was mitigated by a slow oxidation rate and the requirement for a high temperature anneal. Therefore, it is of significant importance to study the electrical properties of anodic SiO_2 layers formed using the LIA method. If a low *SRV* is achieved through low temperature annealing, the LIA method could be a competitive method for growing surface passivation dielectrics for not only PV but also the semiconductor industries.

Table 5-3 A summary of the *SRV* of SiO_2 formed by different techniques.

Ref.	Oxidation Technique	Deposition Temp/ (Anneal Temp)/ Ambient	*SRV* (cm s^{-1})
[288]	Thermally-grown	1050 °C, (450 °C), forming gas	30
[84]	PECVD	350 °C, (400 °C), forming gas	500-1300
[289]	APCVD	400 °C, (400 °C), forming gas	1.2×10^5
[290]	Expanding Thermal Plasma (ETP)	400 °C, (600 °C), forming gas	54
[291]	HNO_3	108 °C, (1100 °C), nitrogen	107
[291]	HNO_3	108 °C, (1100 °C), nitrogen and (400 °C), forming gas	42
[127]	Anodisation (DC bias)	25 °C, (400 °C), O_2 and forming gas	35
[125]	Anodisation (AC bias)	25 °C, (400 °C), O_2 and forming gas	15

This section reports on experiments which investigated the passivation of *p*-type silicon surfaces by anodic SiO_2 formed by LIA after annealing in oxygen and forming gas at 400 °C for 30 min. Photoconductance and quasi steady state photoluminescence (QSS-PL) measurements were conducted to determine the τ_{eff} and an upper limit to the *SRV*. The *C-V* measurements were performed to assess the charge density (Q_{eff}) associated with the anodic oxide and the D_{it} at the silicon/SiO_2 interface.

5.6.1 Experimental

5.6.1.1 Sample Preparation

Anodic SiO_2 films were prepared on alkaline-textured 3 - 5 Ω cm *p*-type Cz 40 mm × 40 mm silicon wafer fragments having a thickness of 180 µm and with a

$POCl_3$-diffused emitter sheet resistance of 80 Ω/□. The *p*-type surfaces of the wafers were planarised by etching in 25% (w/v) NaOH (J.T. Baker) at 80 °C for 7 min. A 18 nm thermal SiO_2 was grown on both surfaces by dry oxidation at 980 °C for 18 min in a quartz tube furnace. After oxidation, the *p*-type surfaces of the wafers were single-side etched in 1% (w/v) HF for 2 min to remove any native oxide before LIA SiO_2 formation and annealing.

The LIA SiO_2 growth was performed in 0.5 M H_2SO_4 (J.T. Baker, where trace metal levels were less than 100 ppb) for 15 min as described in [292], which resulted in an 23 nm thick anodic SiO_2. A constant illumination of 150 W m^{-2} was provided by an array of compact fluorescent light bulbs at a distance of 5 cm from the *n*-type surface of the wafer. The wafers were anodised under constant positive bias of 15 V. After anodisation, the wafers were annealed in a quartz tube furnace at 400 °C. In order to identify the most effective annealing condition to achieve the best surface passivation, the samples were annealed in either oxygen, forming gas or both.

To perform *C-V* measurements, the thermal SiO_2 was removed from the *n*-type surface via HF fuming [293], and 150 nm of aluminium was evaporated onto the rear surface to enable electrical contact to the silicon wafer. Finally, circular aluminium contacts with a diameter of 0.70 mm were evaporated on the front surface to complete the metal-oxide-semiconductor (MOS) structures.

5.6.1.2 Characterisation

The τ_{eff} of the wafers were measured after thermal oxidation and after the post anodisation anneal to enable a direct comparison of surface passivation between the thermal SiO_2 and the anodic SiO_2. Photoconductance measurements were performed using a lifetime tester WCT-120 (Sinton Instruments) under quasi-steady-state illumination and the generalized analysis [294]. In some comparisons, the τ_{eff} was represented as 1-sun iV_{oc} using the relationship [259]:

$$V_{oc} = \frac{kT}{q} \ln\left[\frac{(N_A + \Delta n)\Delta n}{n_i^{\,2}}\right] \tag{5.4}$$

where *k*, *T* and *q* represent Boltzmann's constant, the absolute temperature and the electronic charge (1.602×10^{-19} C), respectively. The carrier injection level, Δn was calculated from the sheet PC under 1-sun irradiation, N_A represents the boron dopant density of the wafers used and n_i is the intrinsic carrier concentration of silicon ($8.3 \times$

10^9 cm^{-3} at 25 °C [295]). The iV_{oc} (at 1-sun excitation levels) was used as an indicator of the passivation quality in some cases. Since QSS-PL measurements are not affected by depletion-region modulation [296, 297], accurate τ_{eff} data at low injection levels was acquired. The QSS-PL measurements were conducted on a modified Sinton Instruments WCT-120, which enabled simultaneous measurements of the excess conductance, the PL intensity, and the generation rate [298].

The wafers used for lifetime measurements contained a phosphorus-diffused emitter on one surface, so the measured τ_{eff} contains contributions from bulk recombination, surface recombination and emitter recombination, and can be represented by:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} + \frac{1}{\tau_{emitter}}, \tag{5.5}$$

where the bulk recombination lifetime τ_{bulk} was measured by a HF passivation method [51], and the emitter recombination lifetime $\tau_{emitter}$ at high injection levels was estimated as described by [299] using:

$$\frac{1}{\tau_{emitter}} = J_{0e}\frac{\Delta n}{qWn_i^2}, \tag{5.6}$$

The surface recombination lifetime was then determined by solving $\tau_{surface}$ in Equation 5.5 and the upper limit of the *SRV* on the *p*-type surface can then be calculated by Equation 5.7 with a high level of accuracy [300]. The τ_{eff} and *SRV* values for LIA anodic SiO_2 reported in this paper are measured/calculated at an injection density of $\Delta n = 1 \times 10^{15}$ cm^{-3}.

$$SRV \le \frac{W}{\tau_{surface}}. \tag{5.7}$$

The *C*-*V* measurements were performed at high frequency (1 MHz) using a 4284A Precision LCR meter and low frequency was using a 4014B pA meter. From these measurements, Q_{eff} was determined from the flat band voltage of the high frequency curves, while the D_{it} was calculated using the Terman [301] and Castagne [302] methods, with the latter technique being the more accurate.

5.6.2 Results and Discussion

5.6.2.1 Surface Passivation

The τ_{eff} of charge carriers in silicon wafers passivated by the formed anodic oxide layers were measured to ascertain the potential use of these layers as passivation layers for silicon solar cells. Figure 5-19 shows the change in τ_{eff} of the wafers during the process. Immediately after anodisation, all wafers experienced a significant degradation in τ_{eff}. This was presumably due to an increase in the D_{it}, which occurs as new Si-O bonds form at the interface on the surface being anodised. Recombination-active interface states may also form during anodisation at the thermal oxide interface with the *n*-type silicon due to the constant tunnelling of the light-induced electrons through that oxide layer. However, this increased carrier recombination that occurs with anodisation appears to be mitigated by subsequent annealing in oxygen followed by forming gas (see Section 5.6.1.1) as evidenced by the return of the measured τ_{eff} to levels measured for wafers passivated with a thermal oxide on both surfaces.

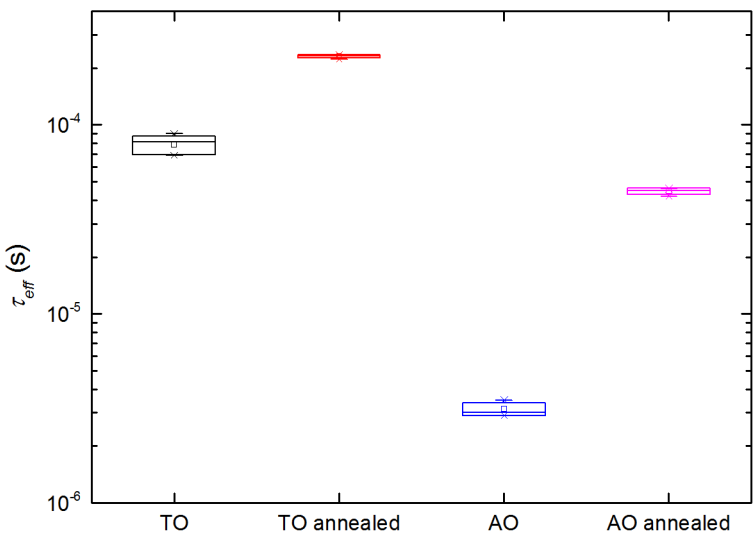

Figure 5-19 The τ_{eff} of wafers symmetrically passivated by thermal SiO_2 (TO); thermal SiO_2 after a post anodisation anneal in oxygen and forming gas both for 30 min (TO annealed); LIA SiO_2 after anodisation (AO) and LIA SiO_2 after a post anodisation anneal (AO annealed). The boxes show the standard deviation of measurements made on 5 individual wafers that were separately anodised and annealed. The bars indicate the maximum and minimum of the measured values.

5.6.2.2 Effect of Annealing Ambient

The effect of annealing ambient was studied to identify the annealing condition that resulted in the most effective surface passivation. Figure 5-20 shows the injection-level dependent τ_{eff} after annealing wafers in oxygen, forming gas and the combination of the two ambients in different sequences. The bulk lifetime of the wafer was measured to be 790 µs by immersing wafer in aqueous HF. Therefore the poor lifetime of as-anodised wafer was primarily due to poor silicon/anodic SiO_2 interface and the subsequent improvements in the effective lifetime were attributed to improved surface passivation. The figure highlights the significant improvement in surface passivation after annealing. However the improvements varied from one to two orders of magnitude in the effective lifetime between different annealing ambients and varied sequences. The experiment demonstrated that the best passivation was attained by first annealing the LIA SiO_2 in oxygen and then in forming gas at 400 °C for 30 min each, which was is consistent with findings reported by Grant *et al.* [127].

The thermal oxidation in dry oxygen stream at 980 °C was used to establish a reference. Figure 5-20 shows the anodic SiO_2 with the oxygen and then forming gas anneal attained comparable effective lifetime to the as-grown thermal SiO_2. However the effective lifetime of thermal SiO_2 was further improved after the same annealing process, suggesting the silicon/SiO_2 interface of anodic SiO_2 was more vulnerable to process-induced defects.

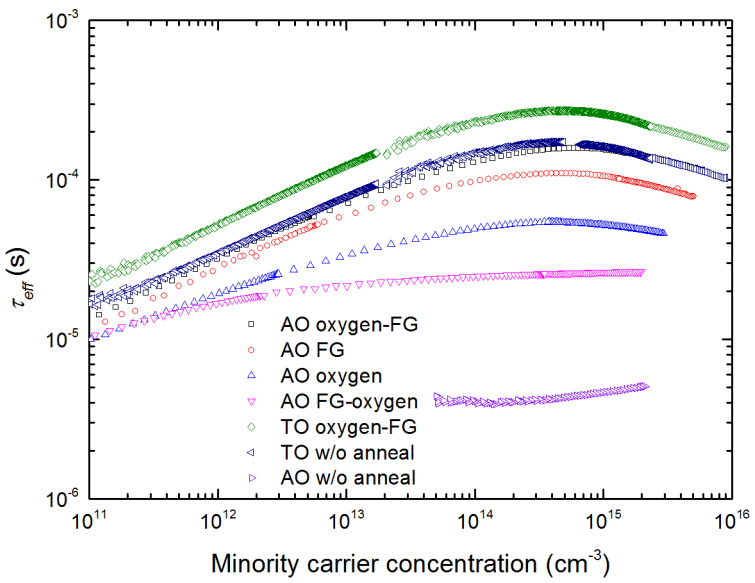

Figure 5-20 Injection-level dependent τ_{eff} of wafers passivated by thermal SiO_2 (TO) and anodic SiO_2 (AO) before and after annealed in either oxygen or forming gas or combinations of the gases.

5.6.2.3 Interface Quality

To determine the reason for a lower τ_{eff} after annealing with anodic SiO_2 compared to thermal SiO_2, the D_{it} and Q_{eff} were measured by *C-V*, where Q_{eff} represents the combined influence of electrostatic charge and mobile charge in the dielectric. Figure 5-21 plots the normalised capacitance as a function of voltage for SiO_2 layers grown by thermal oxidation and LIA. The figure shows that the anodic SiO_2 contained a much lower positive charge (3.4×10^{11} cm^{-2}) than the thermal SiO_2, as determined by the voltage shift in the measured *C-V* curve. Although the LIA process was performed under DC bias, the resulting Q_{eff} was an order of magnitude lower than oxide formed under DC bias with the immersed anodisation technique [303]. Surprisingly, the Q_{eff} was even lower than oxide anodised under AC bias (6×10^{11} cm^{-2}), by which a lower Q_{eff} is usually attained [125]. The low Q_{eff} of LIA anodic SiO_2 may be due to the low bias voltage required during anodisation. A low Q_{eff} is advantageous for a dielectric with stored positive charge when applied to *p*-type silicon surfaces, as the *SRV* is less sensitive to injection level and inversion layer shunting can be mitigated [304].

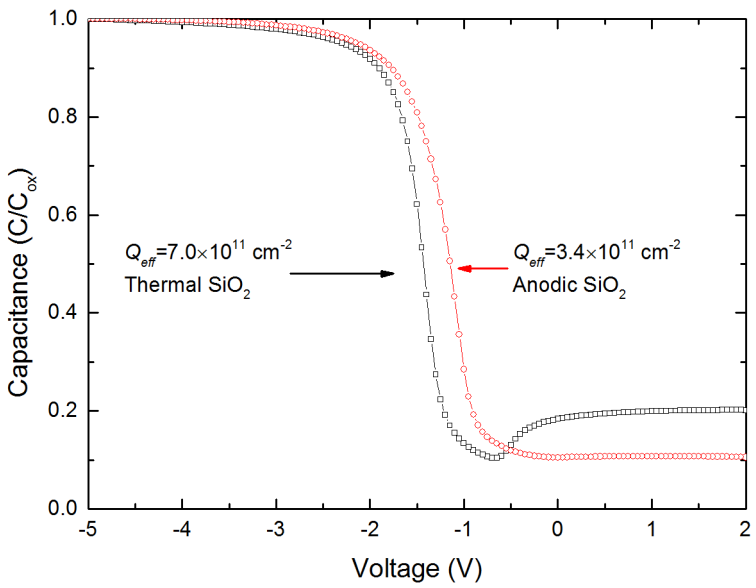

Figure 5-21 Comparison of the measured *C-V* curves of thermal SiO_2 and LIA anodic SiO_2 after oxygen and forming gas anneal at 400 °C for 30 min each.

Figure 5-22 shows the D_{it} of the thermal SiO_2 and LIA anodic SiO_2 determined by the Castagne method. During the anneal in oxygen and forming gas, it is hypothesised that hydrogen present in the oxide film passivated recombination-active

defects at the silicon/SiO_2 interface, therefore decreased the D_{it} at mid-gap to an average value of about 6×10^{11} eV^{-1} cm^{-2}. Although the D_{it} measured was an order of magnitude higher than measured for thermal SiO_2, it was lower than any oxides anodised in an inorganic electrolyte under high DC bias (e.g., 30 - 500 V). This may result because oxidation under very high bias voltages has been reported to also occur at the surface due to cation flow through the growing oxide rather than at the interface [266], therefore the silicon/SiO_2 interface after anodisation was the initial silicon surface, which presented a larger density of interface states. With the LIA technique, however, the low to moderate bias voltage may not have been strong enough to drive the anodic reaction to the surface and therefore anodisation is more likely to have occurred at the silicon/SiO_2 interface where fewer defects are generated. The accumulation of positively-charged carriers close to the *p*-type surface due to light-induced current most likely enhanced the inward movement of the oxidising agent, such as dissociated oxygen ions (O^-) [117]. As shown in Figure 5-23, at the start of anodisation, the process was limited by injection of positively-charged carriers. With the increased thickness of the oxide, the resistance of oxidising agent inward diffusion was increased and the process started to be limited by the supply of oxidising agent. In doing so, it is proposed that the final silicon/SiO_2 interface was formed at the end of the anodisation process, which resulted in improved interface quality.

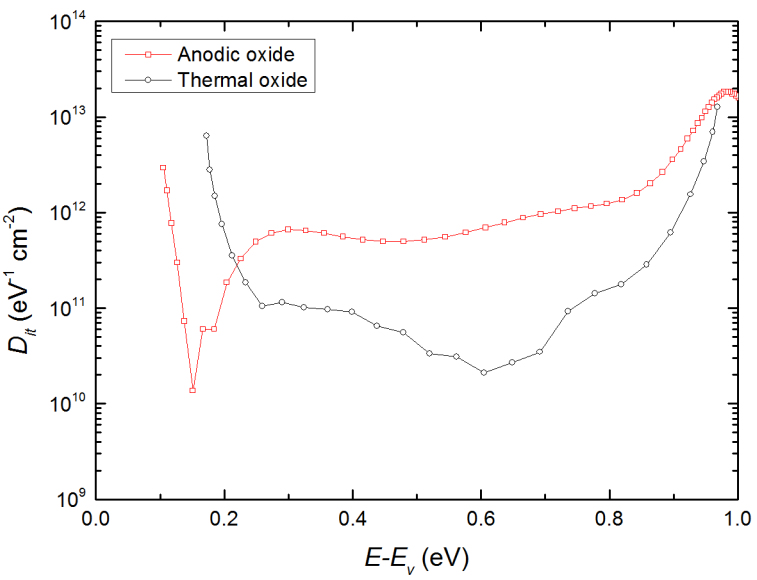

Figure 5-22 The D_{it} of thermal SiO_2 and LIA anodic SiO_2 after oxygen and forming gas anneal at 400 °C for 30 min each.

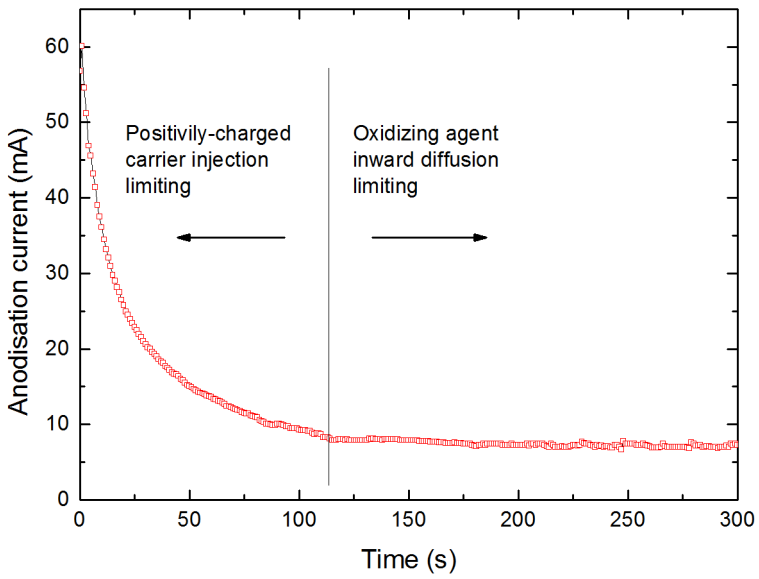

Figure 5-23 Anodisation current graphed as a function of time for LIA anodic SiO_2 growth showing the different growth regimes.

To accurately measure the *SRV* of anodic SiO_2 grown by LIA, the bulk lifetime was measured by a HF passivation method [51]. By immersing the wafer in 20% (w/w) HF during a transient PC measurement, a bulk lifetime of 795 µs was measured, which corresponded to a *SRV* of 62 cm s^{-1} at $\Delta n = 10^{15}$ cm^{-3}. Similar to most of the other anodic SiO_2 films, the *SRV* of the LIA anodic SiO_2 is significantly lower than oxides deposited by CVD techniques, which is primarily due to the improved quality of the anodic-grown interface over deposition. This *SRV* is comparable to the lowest reported *SRV* of anodic SiO_2 layers formed under DC bias at the same injection level (e.g., 65 cm s^{-1} [125]). Further reduction of the *SRV* may be realised by applying an alternating bias during anodisation, which increases the probability that the defect sites and interface traps of anodic SiO_2 are repaired by driving O^- and OH^- ions back and forth across the growing oxide film [117, 125].

5.6.2.4 Density of Anodic SiO_2

Figure 5-24 plots the leakage current density for three different SiO_2 films. The red diamonds, blue triangles and black squares represent direct current anodic SiO_2 [127], LIA SiO_2 and thermal SiO_2 respectively. From the Figure, it is evident that the LIA SiO_2 has the lowest leakage current density over the voltage range examined. Although the LIA SiO_2 film had the highest oxide thickness, it is not expected that such a large difference in leakage current density would result purely from the different

thickness. Consequently we attributed the large differences in leakage current density to physical differences in the films. The leakage current density demonstrated by the LIA SiO_2 is also lower than measured for anodic SiO_2 grown in nitric acid either at much higher grown temperature (113 °C) [305] or with high annealing temperature (600 °C) [124].

From Figure 5-24, it is surprising to see that the thermal SiO_2 has a relatively high leakage current when compared to the anodic SiO_2 films (DC and LIA), even though its measured D_{it} was the lowest of the three films. Therefore, even though the LIA anodic SiO_2 film exhibits higher surface recombination due to a higher D_{it} and lower Q_{eff}, the film appears to be quite dense and with relatively few defects, as evident by the much lower leakage current densities. In the literature, the interface-trap-related leakage current is found to be an important leakage mechanism at the lower field region [306], and the trapping density of positive charges determines the final level of the leakage currents [307]. Therefore, although the D_{it} of anodic SiO_2 is higher one magnitude higher than thermal SiO_2, which might correlate to a higher leakage current, the low positive Q_{eff} of anodic SiO_2 determines the final level of leakage current to be lower. This result is also consistent with the ellipsometry measurements, which demonstrate that the LIA SiO_2 films have a higher n_r of 1.49 than thermal SiO_2. The apparent zero-current shift in the *I-V* curve of the LIA SiO_2 is most likely related to the trapped charges at the silicon/anodic SiO_2 interface. When the voltage is zero, current still flows because the trapped charge acts like a negative offset voltage, thus until a voltage opposing the trapped charge is reached, the current does not achieve the minimum current. Mobile charges in the oxide film are hypothesised to be another cause of the shift to negative voltage bias, which has been observed in an oxygen-plasma oxidised AlO_x film [308], Another possible explanation could result from the accuracy of the 4140 pA meter at such low leakage current values. It is possible that a very small offset current could exist in the system, which may impact the zero current along the voltage axis and cause a large ‘apparent’ voltage shift. This however still implies that the leakage current for LIA anodic SiO_2 is still much lower than that measured for thermal and DC anodic SiO_2.

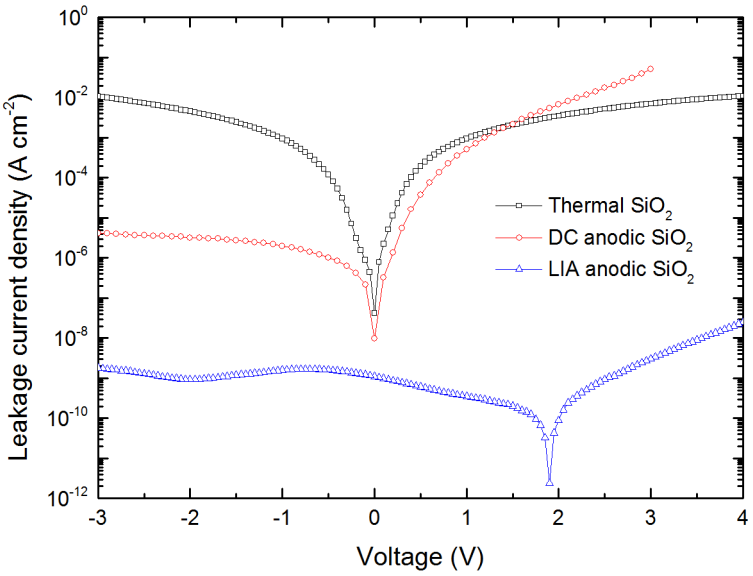

Figure 5-24 *I-V* curves for the MOS diode with thermal SiO_2, DC anodic SiO_2 and LIA anodic SiO_2 being the intervening dielectric.

The high growth rate of the LIA SiO_2 is also advantageous. Figure 5-25 shows the thickness of the LIA SiO_2 films as a function of the anodisation time under 15 V bias voltage and 150 W m^{-2} illumination. An LIA SiO_2 layer 23 nm thick was formed at 25 °C after 15 min anodisation, which contrasts to 3 hours [127] and 4 hours [124] for immersion anodisation in the HNO_3. The growth rate can be further improved by increasing the light intensity or bias voltage [292].

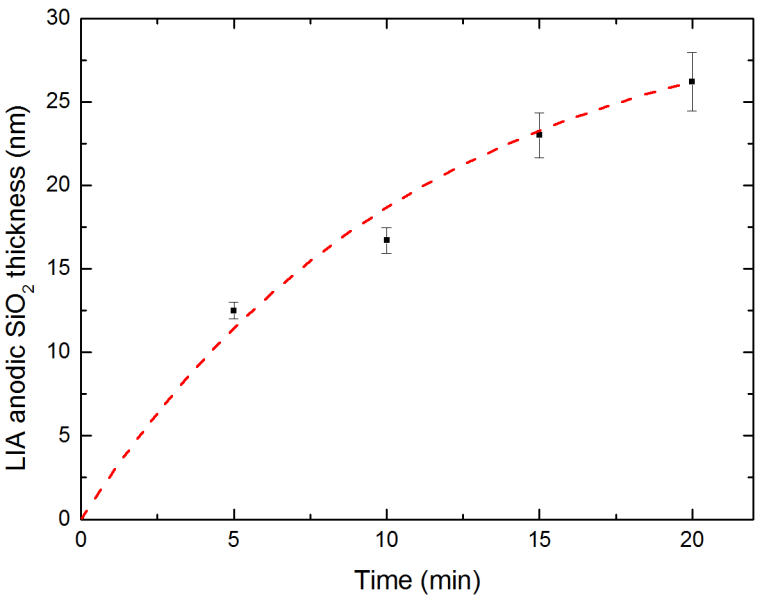

Figure 5-25 Thickness of LIA SiO_2 layers graphed as a function of the anodisation time. Error bars show the standard derivation of five points measured on each wafer.

Featuring excellent low leakage current and high growth rate, the LIA SiO_2 films could potentially find applications in interdigitated back contact (IBC) solar cells, where it is imperative to isolate *p*- and *n*-type contacts from one another, in order to inhibit shunting and maintain high solar cell efficiencies. The low leakage current also suggests that they may provide an effective barrier for metal plating and potential-induced degradation (PID).

5.6.2.5 Stability

The annealing process used was reported by Grant [267] for use with anodic oxides formed in HNO_3 using clip anodisation. Grant suggested that the oxygen-forming gas anneal was most effective, as the oxygen helped "complete" the electrochemical oxidation and the forming gas hydrogenated the silicon/SiO_2 interface.

As shown in Figure 5-19, after annealing, the LIA oxide provided comparable surface passivation to wafers symmetrically-passivated with a thermal SiO_2. This result demonstrates the potential of the LIA process to be used as an alternative to thermal oxidation. Interestingly, the surface passivation of the thermally oxidised wafers was also dramatically improved by the annealing process. This is believed to be due to the hydrogenation of interface defects during the forming gas anneal [309]. If the order of annealing was reversed (i.e., forming gas followed by oxygen), lower τ_{eff} resulted (data not presented here). It was hypothesised that this was due to the oxygen anneal after the forming gas anneal accelerating the dehydrogenation process and therefore minimising the effectiveness of forming gas anneal in reducing the D_{it} [310].

Grant *et al.* [127] reported significant degradation of their anodic oxide layers exposed to the ambient environment over time due to a reduction in positive fixed charge and an increase in D_{it} at energies near Fermi level. To investigate the degradation of oxide formed by LIA, a batch of wafers that were identically anodised to a thickness of 17 ± 1 nm and annealed were divided into two groups, with one group capped by 75 nm silicon nitride layer deposited by remote plasma PECVD and the other group uncapped. Two wafers with 17 ± 1 nm thermal oxide were used as controls, with one undergoing the same anneal process as the wafers oxidised using LIA and the other left as oxidised. All the wafers were stored in air ambient and the iV_{oc} was measured using PC over a period of 50 days.

As shown in Figure 5-26, the uncapped wafers experienced a degradation in iV_{oc} similar to that reported by Grant *et al.* [127]. The iV_{oc} of the control sample with the annealed thermal SiO_2, did not degrade, however, which implied that the silicon/anodic SiO_2 interface formed by LIA process is more vulnerable to the moisture (e.g., water vapour) when compared to thermal SiO_2. However, the iV_{oc} of capped wafers only degraded slightly and were comparable to the thermally oxidised wafer, suggesting that a capping dielectric layer can protect the silicon/anodic SiO_2 interface from degrading over time. Since the oxide formed by the LIA process will, most likely, be used as an intervening layer under other dielectrics (e.g., PECVD SiN_x or AAO), it was concluded that the passivation properties of these layers were likely to be stable in final devices. Further studies evaluating their performance after encapsulation and under high potential stress are required.

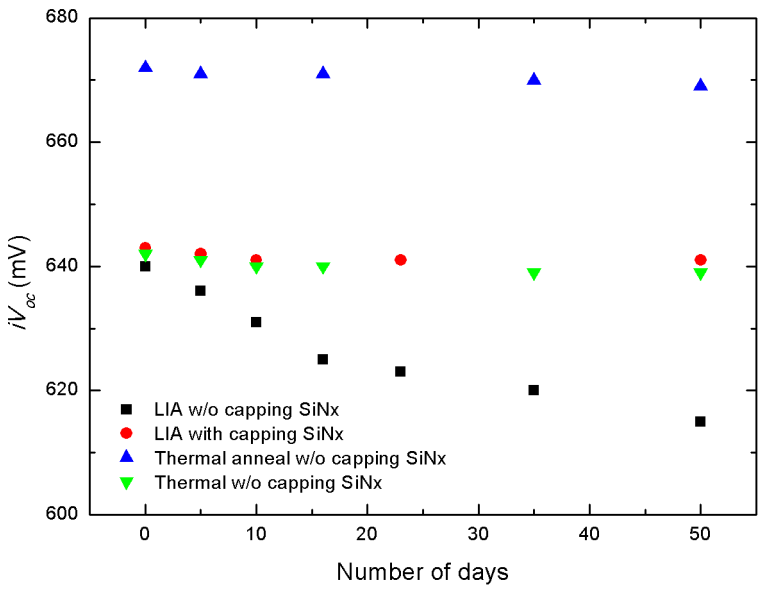

Figure 5-26 Implied V_{oc} measured as a function of time for a LIA oxide with (red circles) and without (black squares) a 75 nm PECVD silicon nitride capping layer. Also shown are iV_{oc} values for wafers symmetrically-passivated with a thermal oxide with (blue up triangles) and without a post anodisation anneal (green down triangles) but without a capping layer.

5.6.3 Conclusions

The electrical properties of anodic SiO_2 layers formed by LIA were investigated in this section. It was demonstrated that anodic SiO_2 formed using LIA achieved comparable τ_{eff} values to thermal SiO_2 after annealing in oxygen and forming gas at 400 °C for 30 min each. The anodic SiO_2 was vulnerable to moisture in the air, however

it was shown that once the oxide was capped by a 75 nm PECVD SiN_x layer, minimal degradation in τ_{eff} was observed in the 50 days following capping.

The quality of the silicon/anodic SiO_2 interface was found to be greatly improved from that reported for anodic SiO_2 layers formed by clip anodisation. The *C-V* measurements showed anodic SiO_2 formed using LIA had a low Q_{eff} at 3.4×10^{11} cm^{-2} and a medium-low D_{it} of 6×10^{11} eV^{-1} cm^{-2} at mid-band gap. The Q_{eff} was lower than that for a thermal SiO_2 and anodic SiO_2 layers formed by AC biased clip anodisation [125]. This was attributed to the low bias voltage used in LIA. Although the D_{it} was one order of magnitude higher than that of thermal SiO_2, it was lower than all the reported anodic SiO_2 layers formed in inorganic electrolytes under DC bias. It was hypothesised that with low bias voltage, the growth of the oxide was limited by the inward diffusion of oxidising agent and the final silicon/SiO_2 interface was formed last, which resulted in improved interface quality. A high quality interface corresponding to a *SRV* of 62 cm s^{-1} was measured at an injection level of 10^{15} cm^{-3}, which was slightly improved from the DC bias clip anodisation but at a significantly improved growth rate, uniformity and repeatability.

Additionally, the LIA anodic SiO_2 had a very low leakage current density (3.5×10^{-10} and 1.6×10^{-9} A cm^{-2} at 1 and -1 V) compared to anodic SiO_2 formed by other techniques, which makes LIA anodic SiO_2 films a promising insulation dielectric for IBC solar cells. It may also find applications in metal plating and PID prevention when integrated in the antireflection coating of silicon solar cells, whilst providing a new alternative for contact passivation.

5.7 Future Applications of Anodic SiO_2

The advantages of low temperature and atmospheric pressure processing make anodic SiO_2 layers formed used LIA suitable for a range of different applications for crystalline silicon solar cells. This section explores potential use of anodic SiO_2 layers, formed using LIA, for contact passivation, a barrier layer for metal plating, passivating epitaxially-grown silicon and a barrier for PID.

5.7.1 Contact Passivation

Metal-insulator-semiconductor (MIS) structures have attracted considerable attention in silicon PV dating from the 1970s [311-313]. In these structures, a thin

insulating layer isolates the metal from directly contacting the silicon and hence improves the device voltage by reducing carrier recombination at the metal/silicon interface. The insulator has a large band gap, which minimises light absorption, and its small thickness (e.g., < 20 Å [312, 314]) facilitates current tunnelling. Based on this concept, pn-junction free MIS-IL solar cells have been demonstrated with V_{oc} values of 655 mV [315] and an efficiency of 18.5 % [316]. Further improvements in cell efficiency were realised by applying the MIS passivated metal contact to pn-junction cells.

The first MIS passivated contact solar cell was reported by Green *et al.* in 1984 [317]. This report described an 18.7% bifacial MIS-n^+p (MINP) cell, featuring a double layer ARC passivated *n*-type emitter and photolithographically evaporated titanium/palladium/silver contacts passivated by a thin thermal SiO_2 layer. The expensive titanium/palladium/silver contacts were then replaced by aluminium contacts [318] and the cell efficiency was improved to 21% [319]. Recently, a cell efficiency of 23% was reported on bifacial silicon heterojunction cell with MIS tunnel oxide junctions, with a very high V_{oc} of 739 mV and a *FF* of 80.5% [320], showing the potential of achieving high cell efficiencies using passivated contacts.

In the previous studies, the insulation layers were mostly thermal SiO_2 layers, however if thermal oxidation can be replaced by a low-temperature anodisation process, the thermal budget and hence the manufacturing cost could be significantly reduced. As demonstrated in Section 5.6.2.3, the LIA anodic SiO_2 achieved a D_{it} at mid-gap of ~ 6×10^{11} eV^{-1} cm^{-2}. This suggests that it can potentially be used as an alternative to thermal SiO_2 for passivation purposes. The current challenges for this application are the control of the LIA process when growing very thin anodic SiO_2 layers with the thickness in the range of 10 - 20 Å and the optimisation of the time consuming oxygen and forming gas annealing processes. Initial experiments showed that when a PECVD SiN_x layer was deposited on an anodic SiO_2 formed using LIA, then following a short anneal at 700 °C the D_{it} was directly reduced. It would be interesting to investigate if similar reductions in D_{it} were possible after the deposition, annealing and hydrogenation of doped amorphous silicon layers.

5.7.2 Barrier for Metal Plating

Self-aligned metal plating of nickel/copper has been used to metallise the front electrode grids for silicon solar cell [156, 275, 321]. Plated contacts have advantages

over screen-printed metallisation in that the fingers can be narrower (e.g., ~ 30 μm [21, 150]) and have a higher metal aspect ratio. However, deposition of unwanted plated metal on the surface of dielectrics in non-patterned areas was reported in both laser-grooved buried contact cells [156, 322] and laser-doped mono-crystalline [323] and multi-crystalline solar cells [324, 325]. This undesirable plating is commonly referred to as 'over-plating' or "ghost plating" and typically it occurs in the presence of sharp edges or pin holes in the dielectric layer. Specific causes include: (i) sharp edges and side walls of the acidic-textured surfaces; (ii) grain boundaries in the multi-crystalline wafers, and more generally; (iii) pin holes in the PECVD SiN_x layers; (iv) surface scratches [324, 325]; and (5) cleanness of the wafer surface before PECVD deposition [323].

Over-plated metal which contacts exposed lightly-doped *p*-type surfaces can result in Schottky contacts, which increases the dark saturation current density (J_0) of the device. The Schottky contacts can cause a high local ideality factor at the medium voltage regions [232, 326], which then reduces the cell *FF*. In extreme cases, the J_{sc} is also lowered as a result of higher shading losses and, if the metal is sintered, shunting between the metal and the base of the cell can occur.

Therefore, several attempts have been made to overcome the over-plating issue. Performing plating at a lower temperature with lower stirring speed was proposed, however this approach cannot completely eliminate over-plating, on the contrary it has the risk of resulting in poor coverage of the laser patterned grooves due to a reduced plating rate [156, 324]. Over-plating can be eliminated by either modifying the topology of the acidic-textured surface by performing a short etch in low concentration alkaline solutions, which smooths the surface, or by incorporating a thin thermal SiO_2 layer prior to the PECVD deposition of SiN_x. However the incorporation of either alkaline etching or thermal oxidation processes can significantly increase the cost due to either maintenance of chemical baths or high temperature furnaces. The high temperatures used to grow thermal oxides can also be detrimental to commercial grade wafers.

A possible way to address over-plating is to grow an anodic SiO_2 on the *p*-type boron emitters for *n*-type cells before deposition of SiN_x. The anodic SiO_2 can also be grown on *n*-type emitters by FIA as discussed in Section 5.2.3. Light-induced anodisation is a RT and atmospheric pressure process, therefore it represents a low-cost alternative that would be with lower-quality wafers. If able to be implemented in inline

wet chemical tools [327, 328], thin anodic oxides should be able to be grown at throughput rates required for industrial production. Moreover, the electrolyte used in LIA process is diluted acid which can be readily removed using a DI water rinse, eliminating the requirement for a dedicated metal ion cleaning process that would be required after alkaline etching.

5.7.3 Passivating Epitaxially-Grown Silicon

Thin silicon solar cells offer the potential of achieving high performance due to reduced bulk recombination, which results in a high cell V_{oc}. This high voltage can be attained if excellent surface passivation and low contact recombination are achieved. Epitaxially-grown silicon, because of its high crystallinity and reasonably high lifetime, is commonly used in crystalline thin silicon solar cells. The growth of epitaxial silicon usually starts on a thermally-treated porous silicon layer deposited on a crystalline silicon substrate. The pores in the porous silicon layer are sealed making an ideal starting point for high quality epitaxy [329], then a defect-free silicon layer, of thickness of 10 - 30 nm, is epitaxially-grown. After epitaxial growth, This silicon layer is then transferred to a low-cost substrate such as glass [330] or steel [331], depending on the cell design.

In the ultra-thin silicon on steel cell structure as depicted in Figure 5-27, a layer of 20 µm epitaxial grown silicon is bound to a steel substrate which acts as rear contact and electrode. To achieve a high cell V_{oc}, the surface is passivated by a thick thermal SiO_2 layer before bonding to steel. The SiO_2 also acts as a dielectrically displaced back reflector. However the growth of thick SiO_2 requires a long thermal oxidation process, which corresponds to not only a high thermal budget but also the risk of redistributing the dopants in the doped epitaxial silicon.

Figure (Text/Chart/Diagram etc.) has been removed due to Copyright restrictions.

Figure 5-27 Schematic diagram of ultra-thin silicon solar cell on steel substrate [331].

Initial experiments were performed to see whether a thin layer of LIA anodic SiO_2 could be grown on the epitaxially-grown p-type silicon surface when it was still attached to the ‘mother wafer’ as shown in Figure 5-28. The XPS depth profile of the formed oxide is presented in Figure 5-29. Although only a very thin layer was grown in this exploratory experiment, thicker layers should be possible by fine tuning the anodisation conditions. One advantage of growing an anodic oxide over performing a

high- temperature oxidation is that dopants are not redistributed as they can be in a thermal oxidation the dopants. This can be of particular importance for very thin silicon cells.

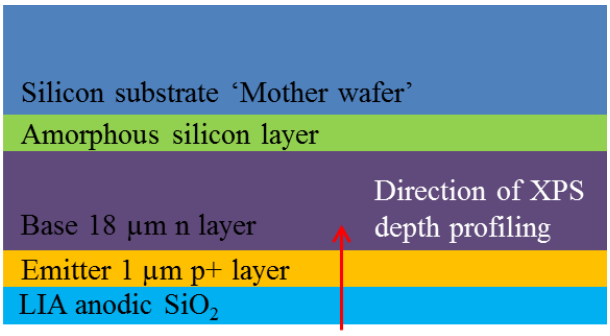

Figure 5-28 Schematic diagram of a sample fabricated for XPS depth profiling. The LIA anodic SiO_2 is grown on the *p*+ layer before bonding to the steel substrate.

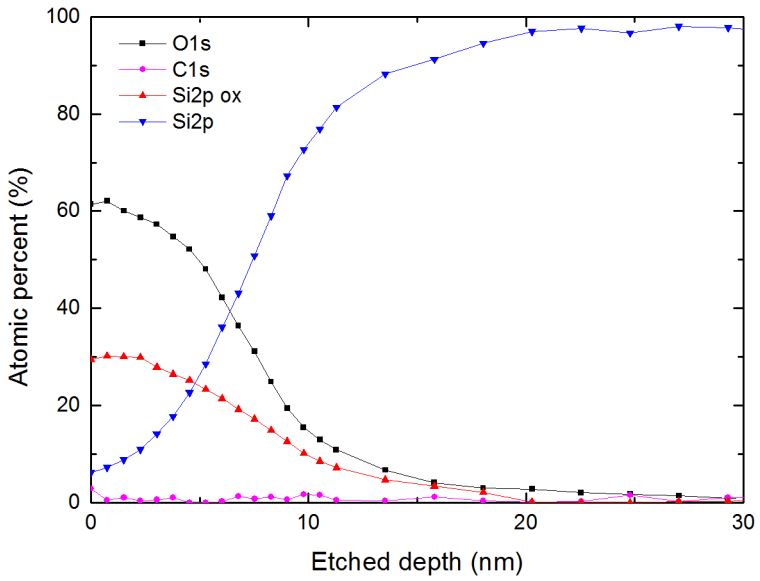

Figure 5-29 XPS depth profile of anodic SiO_2 formed by LIA of the epitaxial grown *p*-type silicon with thickness of 20 µm.

5.7.4 Barrier for Potential-Induced Degradation

Potential-induced degradation is defined as the degradation in PV modules that is caused by leakage current when modules are under high negative voltage with respect to the ground. Humidity, temperature and design of system grounding were found to be major causes of the PID in the previous studies [332, 333]. Although the PID effect can be alleviated by applying proper changes at the system, panel or cell levels, the system

and panel level approaches by either grounding or using different encapsulation material are not always feasible. Therefore, the most practical solution is at cell level [332].

Previous studies have shown that the properties of the SiN_x ARC, such as the refractive index, thickness and homogeneity, can play an important role in eliminating the PID effect [333]. Although SiN_x films with higher refractive index result in reduced PID failure than standard SiN_x, they also have higher absorption which reduces the cell *IQE*. Growing a thin thermal SiO_2 layer before PECVD standard SiN_x deposition can both improve the cell *IQE* and result in less PID failure [334]. The use of a thermal SiO_2 and PECVD SiN_x double layer ARC to mitigate PID effect was also reported by Fraunhofer [335]. This was attributed to the high density and low leakage current density of thermal SiO_2.

According to the discussion in Section 5.6.2.4, LIA anodic SiO_2 has a leakage current density that is 1×10^{-9} mA cm^{-2} at + 1 V, which is six orders of magnitudes lower than a thermal SiO_2. Furthermore, the formation 20 nm LIA anodic SiO_2 requires less than 10 min and the wet chemical surface cleaning (e.g., RCA clean) for thermal oxidation is not required. Therefore, the use of anodic SiO_2 as a barrier layer before PECVD SiN_x deposition can potentially results in improved PID resistance and significant cost savings.

5.7.5 Conclusions

This section explored possible future applications of LIA anodic SiO_2 in a variety of aspects of solar cell design. In most cases, it was shown to be a potential alternative to the thermal SiO_2 film.

Because of the demonstrated low D_{it} and Q_{eff} of LIA anodic SiO_2 for providing effective surface passivation, it can potentially be used as an insulating layer in the MIS passivated metal contacts and the rear surface passivation layer for epitaxially-grown ultra-thin silicon solar cells. The RT processing of LIA may allow application to the passivation of commercial-grade wafers using anodic SiO_2, which otherwise cannot be subjected to high temperature thermal oxidation process. Furthermore, growing a thin anodic SiO_2 before PECVD SiN_x deposition may act as not only a barrier layer for metal plating processes but also a barrier layer to reduce PID failure, due to the very low leakage current densities of anodic SiO_2 layers grown using LIA.

Beyond silicon PV, the LIA anodic SiO_2 may also find its application in the fields such as in passivation of black silicon [336-338] and other pn-junction devices such as light-emitting diodes [339] or integrated circuits required for large-area display devices (e.g., [340]).

5.8 Chapter Conclusions

This chapter reported the development of a novel light-induced anodisation method. This method uses the same principles as the sacrificial anode in LIP, however in LIA the *p*-type silicon surface is deliberately anodised in the electrolyte using the light-induced current and assistance of bias voltage. The wafer to be anodised has to have a pn-junction and only the *p*-type surface contacts the electrolyte during anodisation. The accumulated positively-charged carriers make the *p*-type surface anodic and hence initiate the oxide growth. The starting operating point of the pn-junction is determined by the bias voltage at close to short circuit, therefore maximising the anodisation current.

It is shown that illumination plays an important role in achieving uniform anodisation. Without illumination, the anodisation current relies on the drift current of the cell in reverse bias. Consequently, in order to achieve a high anodisation current, the junction needs to operate in reverse breakdown, which was shown to be detrimental to the cell V_{oc}. The bias voltage is required to overcome the resistive losses in the electrochemical circuit and therefore enables the pn-junction to operate close to short circuit conditions.

The LIA method was used to grow anodic SiO_2 layers and the physical and electrical properties of these layers was investigated. It is found that the growth mechanism of anodic SiO_2 is similar to thermal SiO_2, which can be explained by the 'Deal-Grove' model. The formed SiO_2 thickness has a parabolic relationship with anodisation time. The growth rate of anodic SiO_2 was primarily determined by the anodisation current density, which was controlled by both light intensity and the bias voltage. The LIA anodic SiO_2 is close to stoichiometric, however the silicon to oxygen ratio increases with increased oxide thickness, which is attributed to the outer oxide layer being less dense to maintain the ionic current flow in thicker films. Due to high uniformity of the light-induced current and the fact that the electric field applied in the

LIA process is in perpendicular to the silicon surface, the maximum percentage error in oxide thickness over 16 cm^2 wafer area was only 1%.

Electrical characterisation showed excellent silicon/SiO_2 interface quality of LIA anodic SiO_2, with a low D_{it} of 6×10^{11} eV^{-1} cm^{-2} and a very low Q_{eff} of $+ 3.4 \times 10^{11}$ cm^{-2}. After annealing in oxygen and then forming gas at 400 °C for 30 min each, the LIA anodic SiO_2 demonstrated comparable τ_{eff} to the as-grown thermal SiO_2 and this τ_{eff} was found to be stable if the anodic SiO_2 was capped with an impermeable dielectric, e.g., PECVD SiN_x. Quite surprisingly, the thin anodic SiO_2 has very low leakage current density of 3.5×10^{-10} and 1.6×10^{-9} A cm^{-2} at 1 and -1 V, respectively, which is six orders of magnitude lower than thermal SiO_2.

The advantage of low temperature and atmospheric pressure processing of LIA technique and the excellent electrical properties of anodic SiO_2 opens up the way for applications of LIA anodic SiO_2 in the MIS-passivated metal contacts, passivating epitaxially-grown silicon in thin silicon solar cells, and barrier layer to alleviate metal plating and PID failure. The LIA technique enables the growth of high quality SiO_2 films on commercial grade wafers, which cannot be subjected to high temperature thermal oxidation processes. This paves the way to making higher efficiency solar cells using commercial grade or lower quality silicon wafers.

Chapter 6 Light-Induced Anodisation of Aluminium

The development of a new inkjet patterning method for AAO layers, which could potentially be used to fabricate rear-passivated PERC cells, was reported in Chapter 4. However the application of this new patterning method was limited by the poor uniformity of AAO layers formed by anodising aluminium using clip anodisation as discussed in Section 0. Chapter 5 described the development of a LIA technique, which used the light-induced current of a pn-junction device to anodise a silicon surface to form an anodic SiO_2 layer. Based on the success of growing anodic SiO_2, this chapter reports on experiments which explored the application of LIA to anodising aluminium for the formation of AAO layers. It is demonstrated that uniform AAO layers can be rapidly formed on p-type silicon surfaces by anodising evaporated aluminium. When formed over a thin intervening SiO_2 layer, the LIA AAO layer effectively passivates p-type silicon surfaces primarily due to reducing the interface state density to values as low as 1×10^{10} cm^{-2} eV^{-1}. It is shown that dielectric stacks comprising SiO_2/AAO are capable of passivating silicon surfaces to a level similar to that provided by SiO_2/SiN_x layers which are deposited using PECVD, however at much reduced cost. This new passivation approach for p-type surfaces was trialled in the fabrication of PERC cells resulting in final devices with open circuit voltages as high as 660 mV.

6.1 Introduction

To improve the cost-effectiveness of silicon PV generated power, a reduced cost per Watt of power generated is required. As silicon wafers become thinner for cost-reduction purposes, the surface-to-volume ratio of the wafers increases. Therefore, higher photo-voltages and consequently higher energy conversion efficiencies require that recombination at the wafer surfaces is minimised. The reduction in surface recombination by the application of surface coatings is commonly referred to as electronic surface passivation [341].

The passivation layers that are currently used in silicon solar cell manufacturing are predominantly formed using PECVD, but also ALD and thermal oxidation to much

less extent. The CVD reactors are expensive tools that require high levels of expertise to maintain and multiple chambers in order to achieve high throughput. The cost of depositing a SiN_x ARC for silicon solar cells using a direct PECVD process has been estimated to be 1.54 US cents per Watt of power generated in the first five years (where equipment depreciation costs are appreciable) [342]. Additionally, PECVD of SiN_x and AlO_x requires the use of the pyrophoric gases, silane and trimethylaluminium, respectively, which impose additional costs in terms of worker safety and insurance premiums for manufacturing plants. Furthermore, the application of thermal oxidation furnaces, used to grow SiO_2 layers, is limited in the manufacturing environment as discussed in Section 2.2.1.3.

Alternatively, it is proposed that surfaces could be passivated by anodic oxides, such as AAO. These AAO layers can be formed in solution at RT [206, 265] and can potentially be grown using in-line wet chemical baths similar to those currently used for texturing and etching silicon surfaces in silicon solar cell manufacturing [327]. High-processing throughputs can be achieved by transporting wafers with minimal handling in multiple lanes through these baths. Wet chemical processes can be performed at very low cost, with a value of 0.2 US cents per Watt being proposed for an inline single-side etch wet chemical process capable of processing 7,500 wafers per hour [343].

However, almost all the conventional anodisation methods are primarily based on a clip anodisation technique, which has many limitations, as discussed in Section 0, when applied in PV mass production. To address these limitations, this chapter reports on experiments which investigated the use of the LIA technique, introduced in Chapter 5, to anodise aluminium and form AAO on the *p*-type surfaces of solar cells. In LIA, the anodisation current flows through the wafer and is perpendicular to the surface being anodised. A equal potential is achieved across a wafer surface resulting in the rapid formation of anodic oxides with uniform properties, which is a requirement for silicon PV where wafer sizes are currently 156 mm in width and may increase to 200 mm in the foreseeable future [344].

6.2 Light-Induced Anodisation of Aluminium

The study of aluminium anodisation using LIA process is based on the process developed for anodising silicon in Chapter 5. However, it is important to note that the physical and electronic properties of anodic SiO_2 and AAO are quite different as the growing anodic interface is displaced from the silicon during anodisation of aluminium. This has important implications for the electronic passivation of the silicon surfaces by AAO layers formed using LIA. This section reports on the development of a LIA of aluminium process and investigations into subsequent annealing processes for the formed AAO layers.

6.2.1 Mechanism of Anodic Aluminium Oxide Growth

As reviewed in Section 2.2.5.2, AAO layers have a porous structure with a barrier layer at the substrate/AAO interface. This porous-type property distinguishes it from barrier-type dielectrics (e.g., anodic SiO_2) in the *I-t* curve recorded during anodisation. Figure 6-1 shows a typical *I-t* curve obtained from LIA of silicon and a 300 nm aluminium film under identical anodisation conditions. In barrier-type dielectric anodisation, the thickness of the anodic SiO_2 increases over time. This results in an increased resistance in the oxide, R_o and an exponential decrease in current. In comparison, during growth of a porous-type dielectric by anodising a metal layer, the reaction starts with the formation of a barrier layer, which is evidenced by an exponential decrease in current similar to what is observed with anodisation of silicon. After about 25 s (see Figure 6-1), the current starts to increase again, this increase being attributed to pore initiation [278, 345]. The anodisation current then stabilises until the aluminium is fully anodised into AAO. The barrier layer is continually forming at the aluminium/barrier layer interface whilst simultaneously becoming porous at the barrier layer/porous layer interface. As a result the barrier layer thickness remains unchanged during anodisation. Therefore, unlike the growth of anodic SiO_2, the operating point of the circuit is relatively stable during the porous layer growth phase during aluminium anodisation. Moreover, the thickness of the AAO layer is determined by the thickness of the evaporated aluminium and therefore the anodisation of aluminium is self-limited. In other words, when the aluminium is fully anodised, no current flows in the circuit.

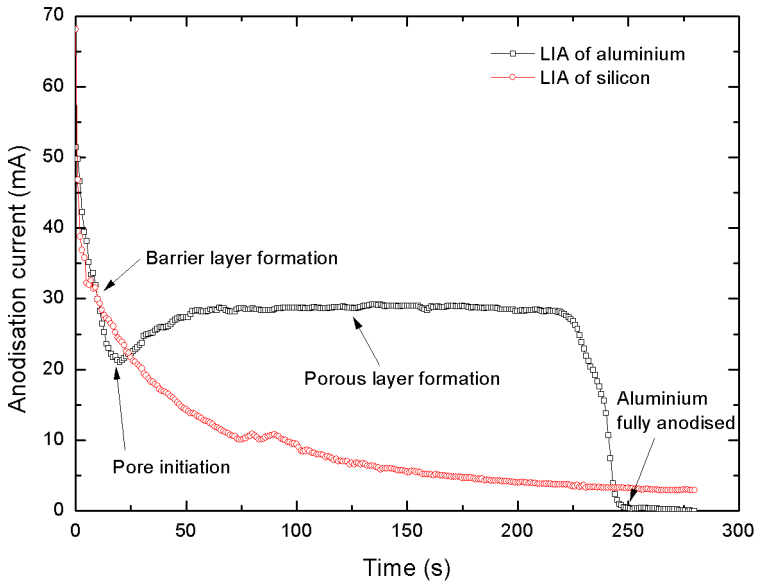

Figure 6-1 Anodisation current profiles resulting from anodising silicon (red symbols) and aluminium on an oxidised silicon surface (black symbols) using LIA. The different current profiles arise due to the different anodisation mechanisms.

Compared to clip anodisation of aluminium, a notable difference in LIA is the current flow through the wafer. In clip anodisation, the silicon substrate is not involved in the anodisation process, as depicted by Figure 6-2(b). The bias voltage is applied directly to the aluminium which is insulated from the silicon substrate by the intervening SiO_2. Therefore, the current is constrained in the aluminium and consequently the uniformity of the AAO is improved from that which is observed for silicon clip anodisation because the current is independent of the resistivity of the silicon wafer. In clip anodisation of silicon the current flows through the silicon wafer. However, in clip anodisation of aluminium rapid anodisation at the electrolyte/air interface can cut off the path of current flow to the remaining aluminium distant to the clip as discussed in Section 0 and in [206].

Figure 6-2(a) shows that LIA of aluminium is a through-wafer process. Electrons generated from anodisation of aluminium tunnel through the intervening SiO_2 and flow through the silicon wafer to the electrode on the other surface of the wafer. Consequently, the aluminium surface will anodise more uniformly than would be possible using the clip method. Furthermore, the interface of anodisation is at equal potential and the path for electron flow is always open until all the aluminium is anodised. A cross sectional transmission electron microscope (TEM) image of the formed porous AAO layer is shown in Figure 6-3.

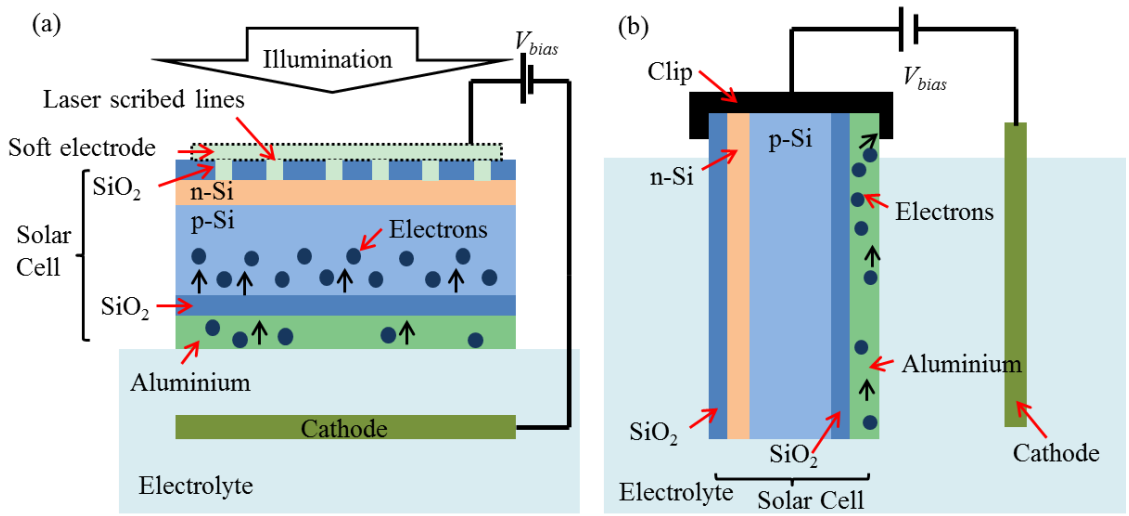

Figure 6-2 Schematic diagram showing the mechanism of: (a) LIA; and (b) clip anodisation of aluminium.

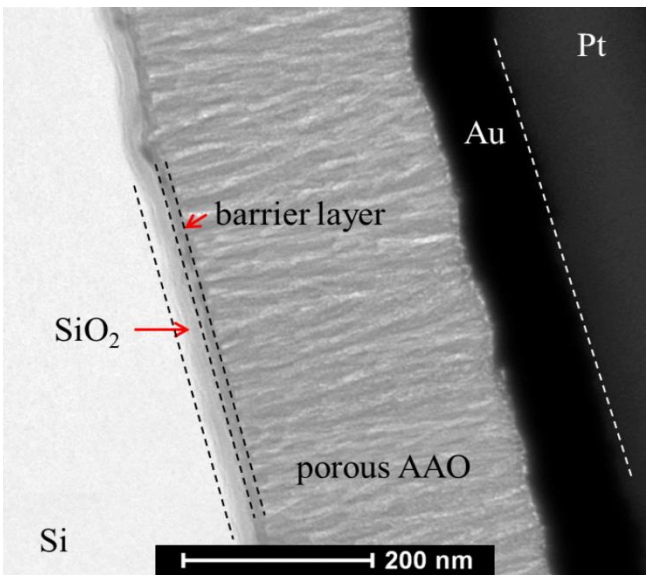

Figure 6-3 TEM cross-sectional image of an AAO layer formed by LIA of a 300 nm aluminium layer. The non-porous barrier layer of the AAO is highlighted between the two red lines at the bottom of porous region.

The function of bias voltage for LIA and clip anodisation is different. Although a DC bias voltage is applied across the pn-junction in a reverse-bias direction during LIA, the polarity of the anodisation current is determined by the light-induced current of the solar cell. The magnitude of the bias voltage is selected such that the solar cell still operates in the first quadrant of its *I-V* curve. Aluminium can be also anodised by applying a high bias voltage without illumination, as was discussed in Chapter 5.

However, wafers anodised in this manner resulted in low iV_{oc} after anodisation, because the reverse bias breakdown may damage the cell junction at localised regions. Figure 6-4 shows the stabilised anodisation current as a function of bias voltage with and without illumination. At all bias voltage values, the current resulting from application of the bias voltage alone is significantly less than that contributed by the light-induced current. The difference in anodisation current becomes larger with increased bias voltage, because the operating point of the solar cell is moving from a point close to open-circuit to the short-circuit operating point.

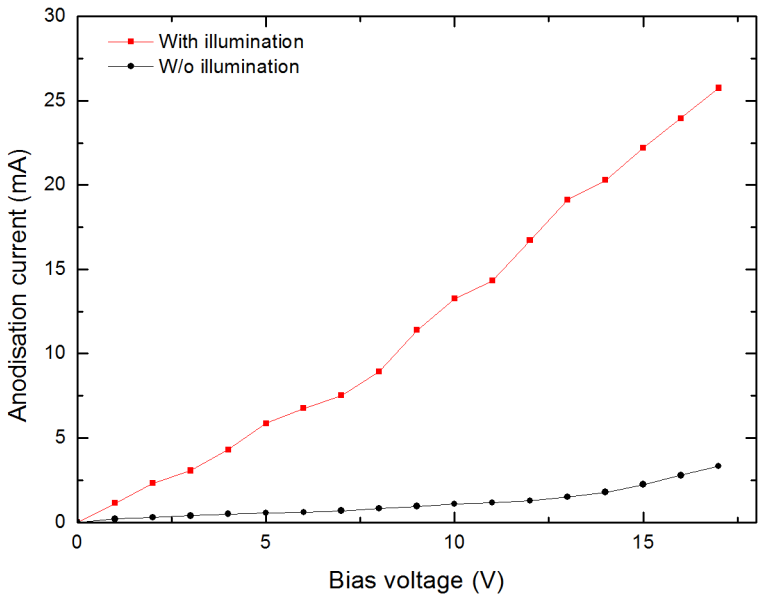

Figure 6-4 Measured stabilised anodisation current for an alkaline-textured 3 - 5 Ω cm boron-doped Cz silicon wafer with a phosphorus-diffused emitter as a function of bias voltage with illumination (red) and in the dark (black) during the anodisation. The intensity of the light provided at the *n*-type surface was estimated to be 150 W m^{-2}.

6.2.2 Comparison to Clip Anodisation

This section reports on experiments that were performed to compare the quality of the *p*-type surface passivation provided by AAO layers grown by LIA and clip anodisation. The measured τ_{eff} of wafers were represented as 1-sun iV_{oc} values and directly compared.

6.2.2.1 Experimental

Alkaline-textured boron-doped 3 - 5 Ω cm wafers were phosphorus-diffused to an emitter sheet resistance of 80 Ω/□. The wafers were then rear-side etched in 25%

(w/v) NaOH (J.T.Baker) at 80 °C for 7 min to remove the residual phosphorus and partially planarise the surface. Wafers were then cleaved into fragments of ~ 40 mm × 40 mm. A 17 ± 1 nm SiO_2 layer was thermally-grown on both surfaces of the wafer fragments at 980 °C for 18 min in a quartz tube furnace, and a 300 nm aluminium layer was evaporated onto the intervening SiO_2 covering the *p*-type surface. One group of five wafer fragments was anodised using clip anodisation and the remaining five wafer fragments were anodised by LIA using the arrangement described in Section 5.3.8. To enable the anode to make low-resistance electrical contact to the *n*-type surface of the wafers anodised using LIA, the SiO_2 layer on that surface was patterned into a series of linear openings spaced 1 mm apart using a 15 W, 532 nm CW laser. The aluminium was anodised using LIA in 0.5 M H_2SO_4, with a 15 V DC bias voltage and 150 W m^{-2} illumination. These anodisation conditions were found to be optimum in the experiments reported in Chapter 5. After anodisation, all wafer fragments were annealed at 400 °C in a quartz tube furnace in nitrogen ambient for 15 min. Figure 6-5 shows a schematic of the test structures.

The τ_{eff} was measured by PC using a lifetime tester WCT-120 (Sinton Instruments) under quasi-steady-state illumination and analysed in generalised mode [294]. In this study the iV_{oc} reported at 1-sun was used as an indicator of the passivation quality for all test structures (as described in Section 5.6.1.2).

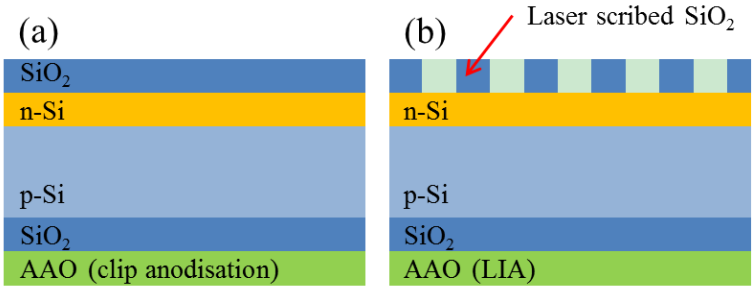

Figure 6-5 Schematic diagram showing wafers passivated by AAO formed by: (a) clip anodisation; and (b) LIA.

6.2.2.2 Results and Discussion

Wafers in both groups started with comparable iV_{oc} values of ~ 630 mV after formation of the thin thermal SiO_2 layers. The extra laser-patterning step reduced the iV_{oc} of LIA AAO passivated wafers by ~ 20 mV (~ 3%). After anodisation, the mean iV_{oc} of clip anodised wafers increased by ~ 10 mV, while only a marginal increase was

observed for wafers anodised using LIA. The marginal increase after LIA was attributed to an increase in the D_{it} at the silicon/SiO_2 interface caused by electrons tunnelling through the thermal SiO_2 layer as discussed in the previous section. In comparison, during clip anodisation, the current was constrained in the aluminium layer hence the electrical quality of the silicon/SiO_2 interface was not impacted.

However, after annealing in nitrogen, the mean iV_{oc} of the wafers anodised using LIA increased from 618 to 654 mV, whilst the change in clip anodised wafers was minimal. Furthermore the variation in iV_{oc} after annealing was smaller for the wafers anodised using LIA, suggesting that the LIA process was more consistent and reliable than clip anodisation.

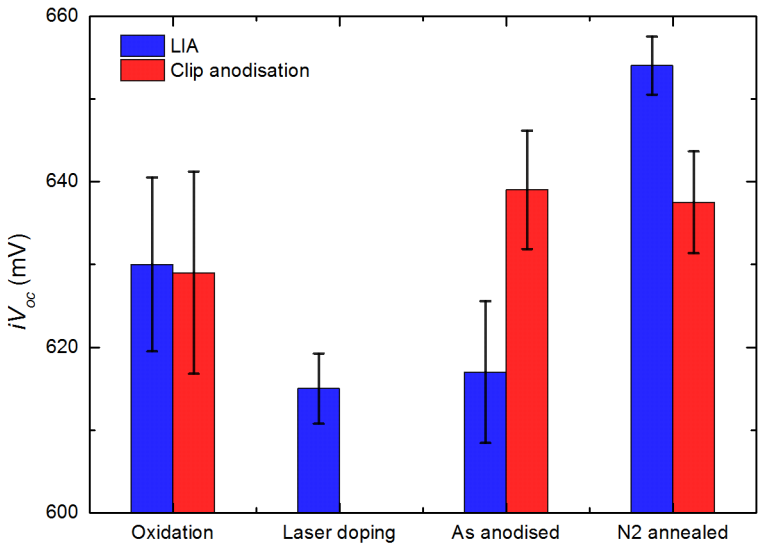

Figure 6-6 Implied V_{oc} of wafers anodised by LIA and clip anodisation at different steps of process. The error bars show the standard deviation of five wafers in each group.

6.2.3 Improved Surface Passivation by Process Optimisation

The experiment reported in the previous section demonstrated that anodisation using LIA can result in higher τ_{eff} values than when the anodisation is performed using the clip method. A solar cell's V_{oc} is limited to the maximum iV_{oc} before metallisation, as subsequent patterning and metallisation processes will typically result in some voltage losses, because for pn-junction silicon solar cells the metallisation is not decoupled from the absorber properties. Based on the lessons learned from LIA of silicon (reported in Chapter 5), the evaluation of surface passivation quality can be simplified by eliminating the laser patterning of the thermal SiO_2 on the *n*-type surface therefore eliminating the voltage losses that occur with that step. In Section 5.6.2.1 it

was shown that the current from the soft graphite electrode can tunnel through the thin SiO_2 layer. Furthermore, it was shown that oxygen and forming gas anneals performed after anodisation can result in significant improvements in the measured τ_{eff}. It was concluded in Section 5.6.2.2 that this improvement was due to the improved quality of the silicon/SiO_2 interface. This section reports on experiments that investigated the potential of similar optimisations in the LIA of aluminium process. The τ_{eff} values measured after anodisation and annealing (represented as 1-sun iV_{oc} values) were directly compared to those of comparative SiO_2/SiN_x dielectric stacks.

6.2.3.1 Experimental

Wafer fragments were prepared as described in Section 6.2.2.1 with the following differences: (i) the *n*-type surfaces were not laser-patterned; and (ii) after LIA, a subset of wafer fragments were annealed in oxygen and then forming gas at 400 °C for 30 min in each ambient. A baseline was established by annealing another subset of wafer fragments at 400 °C for 15 min in nitrogen. For a third subset of wafer fragments, a 75 nm SiN_x film was deposited by remote PECVD (Roth & Rau AK 400) on the intervening thermal SiO_2 on the *p*-type surface (i.e., replacing the AAO), simulating an industrial rear surface passivation process. Wafers with SiN_x were not annealed as mentioned above. The τ_{eff} was measured by PC at each step and represented as a 1-sun iV_{oc}. Figure 6-7 shows a schematic of the fabricated test structures.

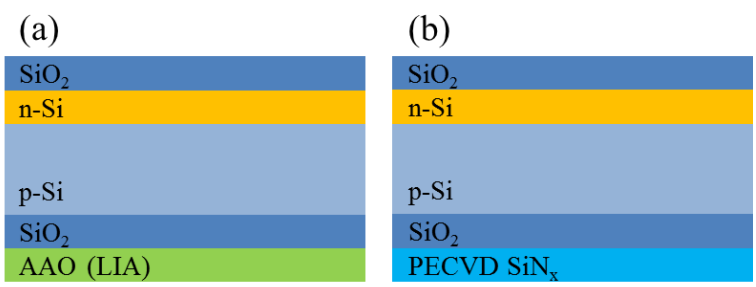

Figure 6-7 Schematic diagram showing wafers passivated by: (a) AAO formed by LIA of aluminium, without laser-patterning the n-type surface; and (b) PECVD SiN_x.

6.2.3.2 Results and Discussion

As illustrated in Figure 6-8, in the absence of laser-patterning of the *n*-type surface, the degradation in the mean iV_{oc} of the wafer fragments after LIA was more pronounced. There was also a much larger variation in iV_{oc} among the anodised wafer

fragments. Without laser patterning, the current tunnels through the intervening SiO_2 on both surfaces, therefore it is reasonable to assume that the D_{it} at both silicon/SiO_2 interfaces would have been increased. Despite these variable effective lifetimes, after annealing in nitrogen at 400 °C for 15 min, a mean iV_{oc} of 650 mV was achieved [see Figure 6-8 (C)], a value that was comparable to wafer fragments with a laser-patterned *n*-type surface (see Figure 6-6). The finding suggested that the degradation in effective lifetime due to current tunnelling through the thin SiO_2 layers was recovered by annealing in nitrogen and therefore the laser-patterning of the *n*-type surface was not essential for forming a high quality AAO layer. It is reported that hydrogen from overlying dielectric layers can effectively eliminate recombination-active defects at the silicon/SiO_2 interface [346]. It is interesting to note that an increase in mean iV_{oc} of ~ 35 mV was achieved by simply annealing in nitrogen. If the presumed reduced D_{it} was due to hydrogen then the implication of this result is that the hydrogen must have come from the AAO layer itself. It has been shown that AAO layers formed by clip anodisation contain hydrogen [347-350] and, if anodisation is performed in deuterated electrolytes, the deuterium can also be detected in the formed AAO layers [207]. The fact that an even higher mean iV_{oc} was measured when the wafer fragments were annealing in oxygen and forming gas may suggest that the introduction of even further hydrogen may be advantageous. However another explanation is that the oxygen anneal plays a critical role in the elimination of interfacial defects. This possibility is supported by the fact that annealing anodic SiO_2 layers just in forming gas resulted in lower iV_{oc} values than annealing the oxides in oxygen and forming gas as reported in Section 5.6.2.2. A similar observation for anodic SiO_2 was reported by Grant [127].

The ability to eliminate the laser-patterning step not only simplified the process but also eliminated the impact of laser-induced damage in the study of surface passivation. Consequently, the *n*-type surface was not patterned in the subsequent experiments.

An issue that emerged from these findings was that the iV_{oc} of the wafer fragments was now limited by the silicon/SiO_2 interfaces, rather than any extrinsic effects such as laser damage. Therefore alternative annealing processes, which could improve the quality of these interfaces, were investigated. Figure 6-8 (D) shows that the mean iV_{oc} could be increased to ~ 671 mV after annealing in oxygen followed by forming gas at 400 °C. This value was comparable to the value of 677 mV measured for wafer fragments passivated with an as-deposited SiO_2/SiN_x dielectric stack.

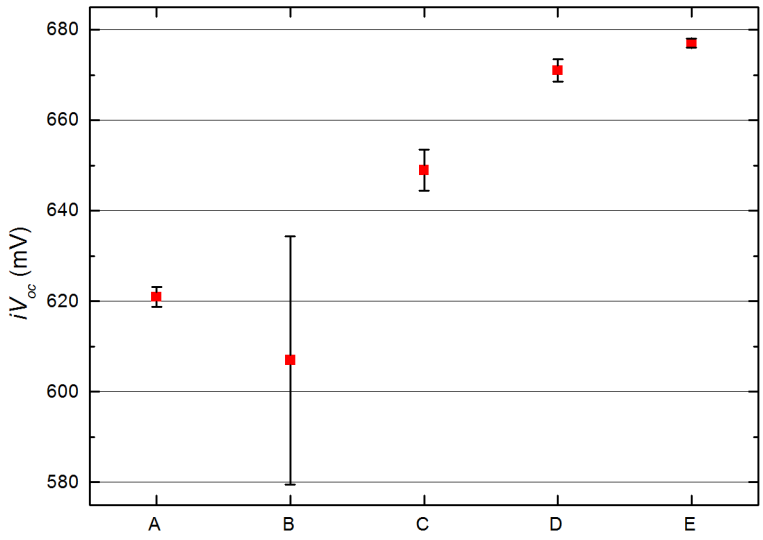

Figure 6-8 Mean implied V_{oc} of wafer fragments: (A) passivated by 18 nm thermal SiO_2 on both wafer surfaces; (B) after anodisation of aluminium using LIA (i.e., SiO_2/AAO); (C) after annealing in nitrogen at 400 °C for 15 min; (D) after oxygen and then forming gas anneal at 400 °C for 30 min in each ambient; and (E) after deposition of SiNx on the same thermal SiO_2 layer. The *n*-type surface was passivated by a thermally-grown 18 nm SiO_2 for all wafers. The error bars represent the standard deviation of five wafer fragments for each group.

6.2.3.3 Conclusions

The results presented in this section suggested the possibility that SiO_2/AAO dielectric stacks may be able to effectively replace SiO_2/SiN_x stacks for rear surface passivation in PERC solar cells. The significant improvement in iV_{oc} that was measured with annealing the SiO_2/AAO layers in both nitrogen and the oxygen and forming gas suggests that, during the annealing process, damage created by current tunnelling through the thin oxide layers can be effectively 'repaired'. The fact that a significant improvement in iV_{oc} is achieved by annealing in nitrogen suggests that AAO layers formed using LIA may also contain reservoirs of hydrogen which can be used to reduce the density of recombination active defects at the silicon/SiO_2 interface. The effects of annealing on the silicon interfacial properties in AAO stacks are discussed further in Section 6.3.

6.2.4 Thermal Stability

A major limitation of the AAO layers formed by clip anodisation is the poor thermal stability of the layers. Lu *et al.* [206] exploited the fact that not all the aluminium is anodised during clip anodisation to form self-patterned metal contact

regions. However, if the intention is to deliberately pattern a SiO_2/AAO dielectric stack, the presence of residual aluminium after anodisation results in metal penetration through the dielectric on belt furnace firing as demonstrated in Section 4.5.2.2. Due to this limitation, in a previous study by Lu *et al.* [265], AAO layers were formed over a thick SiO_2/SiN_x dielectric stack layer before being laser-patterned for aluminium-alloyed local contact regions. Although Lu *et al.* show that the AAO layer can contribute a source of dopants for laser doping [207], use of AAO will not reduce the manufacturing cost as a plasma process is still required to deposit the SiN_x. In other words, the need to use SiN_x in this rear dielectric stack limits the value of using the AAO layer as it is essentially simply a source of dopant.

Section 6.2.3 demonstrated that AAO layers formed by anodising aluminium directly on a thin intervening SiO_2 layer by LIA can result in similar levels of surface passivation to SiO_2/SiN_x layers. The SiO_2/AAO dielectric stacks in the reported experiments were shown to be stable at 400 °C (as the τ_{eff} increased with annealing), however stability is required at higher temperatures (i.e., above the aluminium-silicon eutectic temperature of 577 °C) if aluminium-alloyed LBSF regions are to be formed for cells. The experiments reported in this section aimed to establish whether AAO layers formed by anodisation of aluminium using LIA could withstand belt furnace firing at 750 °C, the latter temperature being indicative of a peak firing temperature that would be required to form an aluminium-alloyed LBSF.

6.2.4.1 Experimental

Double-side polished, boron-doped 1 - 10 Ω cm Cz silicon 40 mm × 40 mm wafer fragments were phosphorus-diffused to an emitter sheet resistance of 100 Ω/□. The wafer fragments were then rear-side etched to remove the residual phosphorus. An 17 ± 1 nm SiO_2 layer was thermally-grown on both surfaces in a quartz tube furnace, and a 300 nm thick aluminium layer was evaporated onto the intervening SiO_2 covering the *p*-type surface. Three wafer fragments were anodised by LIA. After anodisation, they were cleaved into two using a laser. One half-wafer was annealed in a quartz tube furnace at 400 °C in nitrogen for 15 min and the other half fired at 750 °C in a Centrotherm belt furnace with a belt speed of 5400 mm min^{-1}, which corresponded to the wafer fragments being exposed to the peak firing temperature for duration of ~ 4 s. Open circuit PL imaging was performed before and after heat treatment to examine the thermal stability of the AAO layers. A similar wafer fragment, for which the aluminium

was anodised by clip anodisation, was annealed at 400 °C and then fired at 750 °C with the same belt speed.

6.2.4.2 Results and Discussion

Figure 6-9 (a) and (b) shows PL images recorded of a wafer fragment on which the AAO layer was formed by clip anodisation of aluminium over a thin SiO_2 layer after annealing at 400 °C in nitrogen and after firing at 750 °C in the belt furnace, respectively. Although the average PL intensity increased after the low temperature anneal, it was severely degraded after firing at 750 °C. The temperature of 400 °C was presumably too low to result in any penetration of the 17 nm SiO_2 layer by aluminium residue due to incomplete anodisation. However, this was not the case when the wafer fragment was fired at the higher temperature in the belt furnace with the average PL intensity reducing from 3×10^4 to 5×10^2 counts. Any aluminium that penetrated the thin SiO_2 layer would have resulted in shallow aluminium-alloyed regions at the silicon surface as shown in [206]. The dashed lines in Figure 6-9 indicate the electrolyte/air interface due to the need to clip the wafer fragment, with the clip remaining dry to prevent anodisation. The wafer was clipped in two spots, right edge and top left corner; therefore aluminium residue remained in these areas. The aluminium residue may spike through the thin SiO_2 during heat treatment resulting in the dark spots shown in Figure 6-9(a), or stay on the SiO_2 and become a displaced reflector which results in a very high PL signal intensity as shown in Figure 6-9(b), however this high intensity does not necessarily correlate to improved surface passivation (i.e., optical effects must be the same for PL intensity to linearly correlate with τ_{eff}).

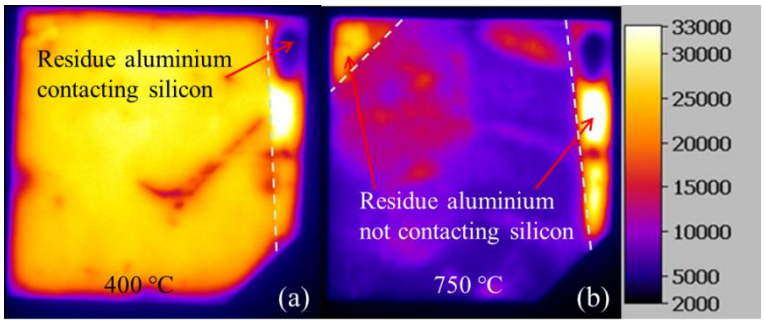

Figure 6-9 Open circuit PL images showing: (a) uniform surface passivation provided by an AAO layer formed by clip anodisation of aluminium over a thin SiO_2 layer after a 400 °C anneal in nitrogen; and (b) reduced PL intensity which was attributed to degradation in surface passivation after 750 °C firing. The exposure time for both PL images was 1 s.

Figure 6-10 shows that the thermal stability of the AAO layers formed by LIA is much improved over those formed using clip anodisation. Figure 6-10 (a) shows PL images of two halves of a wafer fragment after LIA. Because the anodisation current passes through the wafer in LIA the entire surface is uniformly anodised (i.e., no unanodised regions due to clips). After annealing at 400 °C in nitrogen for 15 mins, the τ_{eff} was significantly improved as evidenced by the more intense PL signal shown in Figure 6-10(b). After firing at 750 °C, similar surface passivation to that achieved with the 400 °C anneal was demonstrated. The increase in PL intensity at the top left hand corner was reduced compared to that in the centre. It was hypothesised that this may have been due to non-uniform heating in the belt furnace (i.e., where the wafer was placed with respect to the belt metal).

This result suggested that LIA results in more complete anodisation than occurs with clip anodisation. This is perhaps to be expected, as the anodisation current is passing through the wafer perpendicular to the aluminium layer and so it is unlikely that aluminium regions become isolated in the formed dielectric. However, it should be noted that the experiments reported here used polished wafer surfaces and, for cells, LIA would need to be performed on partially-planarised surfaces.

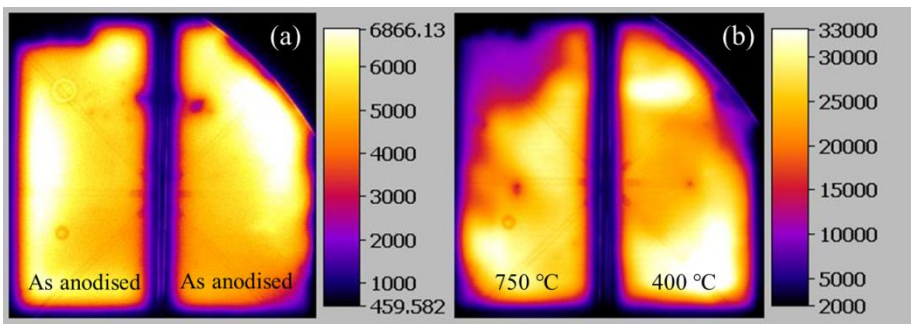

Figure 6-10 Open circuit PL images showing: (a) as-anodised AAO by LIA after laser cutting; and (b) after firing in a belt furnace at 750 °C (left) and annealing at 400 °C for 15 mins (right), respectively. The different scale is used to show the uniformity in detail. The exposure time for both PL images was 1 s.

6.2.4.3 Conclusions

Based on this result, it was concluded that AAO layers, formed by LIA of aluminium on thin SiO_2 layers, can withstand a high temperature belt furnace firing process which would be required to form LBSF regions. This suggested that less aluminium remains after the LIA process as compared with clip anodisation. However,

the surface passivation may be sensitive to the uniformity of heating. Consequently, it was concluded that it may be preferable to sinter cells with rear AAO layers at lower temperatures, rather than employ a high temperature firing step used for aluminium alloying.

6.2.5 Anodic SiO_2/AAO Dielectric Stack Passivation

The use of thermal oxides is undesirable in manufacturing because it necessitates the maintenance of high temperature furnaces in very clean states for high quality oxide growth. Given the results of Chapter 5, where LIA was used to form anodic SiO_2 layers, it was perhaps obvious to try and replace the thermal SiO_2 layer with an anodic SiO_2 in order to further reduce the potential cost of this SiO_2/AAO rear passivation layer. In other words, first grow an anodic SiO_2 layer by LIA on the *p*-type surface, then deposit aluminium over that oxide and anodise it by LIA to form AAO. The experiments reported below explored this possibility.

6.2.5.1 Experimental

Wafers were prepared until after thermal oxidation as described in Section 6.2.2.1. The thermal SiO_2 on the *p*-type surface was then removed by single-side etch exposing the wafer to 1% (w/v) HF for 2 min. A ~ 10 nm LIA anodic SiO_2 was grown on the *p*-type silicon surface by anodising in 0.5 M H_2SO_4, at 15 V and 150 W m^{-2} illumination. As shown in Figure 6-11, a subset of the wafers went through the first anneal at 400 °C in oxygen and then forming gas for 30 min each, which improved the silicon/SiO_2 interface quality as discussed in Section 6.2.3. Another subset of wafers was not annealed after the growth of anodic SiO_2. Then a 300 nm thick aluminium layer was evaporated on the anodic SiO_2 layer and anodised using the conditions detailed above. After formation of AAO, all the wafers were annealed in oxygen and then forming gas. The process flow is summarised in Figure 6-11.

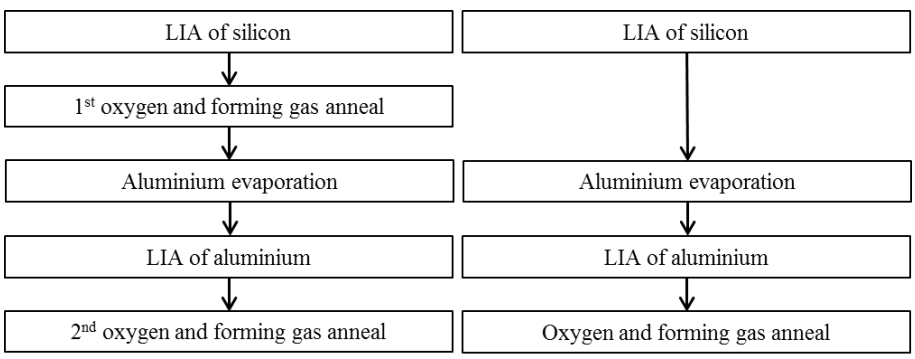

Figure 6-11 Process flow for preparing anodic SiO_2/AAO stack layers.

6.2.5.2 Results and Discussion

Figure 6-12 shows the iV_{oc} of wafers passivated by anodic SiO_2/AAO dielectric stack. After the first anneal of anodic SiO_2, an iV_{oc} of ~ 640 mV was achieved, similar to the value reported in Section 5.6.2.5. As expected, the subsequent anodisation of aluminium degraded the surface passivation again due to the current tunnelling through two intervening oxide layers. Surprisingly, the second anneal process recovered the iV_{oc} to an average of 650 mV, however there was considerable variation in the measured lifetimes. Attention was then turned to simplify the process by eliminating the first anneal (i.e., after anodising silicon) and relying on the second anneal to anneal the current tunnelling damage. However, with this simplified process the mean iV_{oc} after the single final anneal was only 577 mV, a value that was very close to the starting iV_{oc}.

These findings showed that anodic SiO_2 can potentially replace a thermal SiO_2 layer as an intervening layer for AAO growth, however only if the anodic SiO_2 is annealed before aluminium anodisation. This suggests that the quality of the silicon/anodic SiO_2 interface is critical for effective passivation by AAO formed by LIA. If the starting interface quality was low, then annealing after formation of AAO was unable to recover the lifetime. Another noticeable finding was that the silicon/anodic SiO_2 interface was more vulnerable than the silicon/thermal SiO_2 interface in the subsequent aluminium anodisation process. Therefore the improvement in iV_{oc} after the second anneal was marginal and the variation from wafer to wafer was large. One possibility that could be investigated is that the damage at the silicon/SiO_2 interface needs to be maintained below some critical value if it is to be recovered in a subsequent annealing step. If this is the case then it may be possible to address the issue of interface damage by anodising using reduced illumination intensity (i.e., anodisation current).

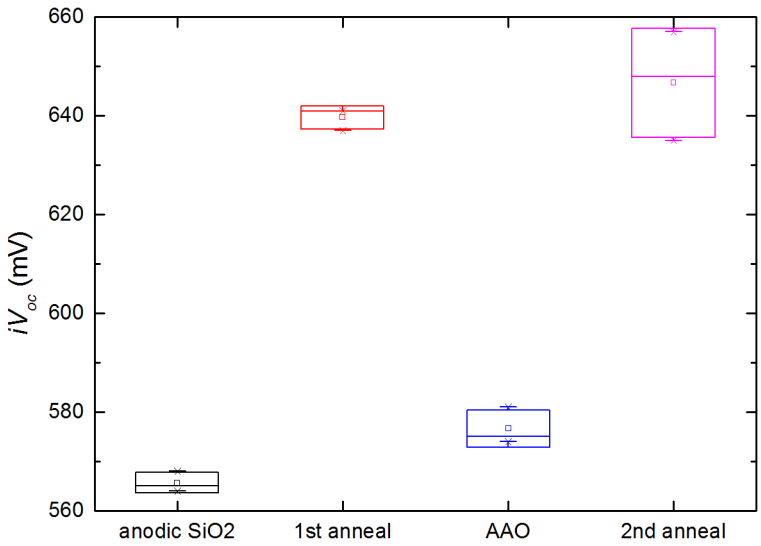

Figure 6-12 Implied V_{oc} of wafers passivated by anodic SiO_2/AAO dielectric stack at different stages of processing. The box shows the standard derivation of five wafers.

6.2.5.3 Conclusions

It was shown that anodic SiO_2 could replace a thermal SiO_2 layer as the intervening layer in SiO_2/AAO dielectric stacks provided that an anneal in oxygen and forming gas are performed before deposition of aluminium and LIA to form the AAO layer. Further investigation is required to understand why this is so, however it is hypothesised that, if the silicon/SiO_2 interface is damaged too much by a tunnelling current, then it cannot be 'repaired' by a final anneal after the AAO has been formed. Use of reduced illumination should be explored in future experiments.

For the remaining experiments reported in this Chapter, a thermal SiO_2 intervening layer was used in the SiO_2/AAO dielectric stack to ensure repeatable results. However, the use of a fully anodic SiO_2/AAO dielectric stack is considered worth investigating in future work, due to its potentially significant reduced cost and simplification of the process.

6.2.6 Conclusions

This section discussed the mechanism of LIA of aluminium and compared it to the mechanism of LIA of silicon and clip anodisation of aluminium. It was demonstrated that the AAO layers formed using LIA resulted in higher iV_{oc} values than equivalent layers formed using clip anodisation. This was primarily attributed to the improved uniformity of the AAO layer and completeness of the anodisation process (i.e., reduced residual aluminium). Although in initial experiments the *n*-type surface was

patterned by a laser to ensure low resistance electrode contacts, it was shown that this patterning was not necessary as current could tunnel through the thin SiO_2 layer on the *n*-type surface.

It was shown that the surface passivation was further improved by annealing anodised wafers at 400 °C in oxygen and then forming gas for 30 min in each ambient. This annealing process was derived from the work of Grant *et al.* [127] and successfully used in Chapter 5 to anneal SiO_2 layers formed by LIA of silicon. After annealing, one-sun iV_{oc} values that were comparable to SiO_2/SiN_x dielectric stacks were demonstrated. It was also shown that the thermal stability of AAO was improved by using LIA, although the surface passivation after high temperatures firing was sensitive to the uniformity of heating profile.

The potential of replacing the thermal SiO_2 intervening layer by an anodic SiO_2 formed by LIA was also investigated. It was found that equivalent effective surface passivation was achievable with the anodic oxide as long as the silicon/anodic SiO_2 interface was annealed before the anodisation of aluminium. However, this interface was more sensitive to a subsequent anodising process, therefore further investigation (e.g., by lowering anodisation current density) may be required to enable a subsequent anodisation process to be performed without an interim annealing step.

6.3 Interface Quality

Section 6.2.5 showed how critical the silicon/SiO_2 interface is for effective surface passivation. The quality of the silicon/SiO_2 interface can be characterised using measurements of D_{it} and Q_f as described in Section 5.6.2.3. The variation in iV_{oc} observed in the previous sections after performing different annealing processes may be due to the variations in D_{it} and Q_f. To further investigate the mechanism by which post anodisation annealing improves the surface passivation, the Q_f within the SiO_2/AAO dielectric stack layer and the D_{it} at the silicon/SiO_2 interface were measured by contactless *C-V* [351, 352] before and after annealing in both nitrogen in a tube furnace or air ambient with an industrial belt furnace.

6.3.1 Experimental

Experiments were performed on alkaline-textured 3 - 5 Ω cm boron-doped Cz silicon wafer fragments (40 mm × 40 mm) of thickness of 180 µm. Wafers were

$POCl_3$-diffused to form emitters having a sheet resistance of 80 Ω/□. The *p*-type surfaces were then planarised by etching in 25% (w/v) NaOH (J.T. Baker) at 80 °C for 7 min with the front surface protected by a sacrificial PECVD SiN_x layer. After removal of the SiN_x, a thermal SiO_2 layer of 17 ± 1 nm thickness was formed by dry oxidation at 980 °C for 18 min in a quartz tube furnace followed by thermal evaporation of a 300 nm layer of 5N purity aluminium on to the *p*-type silicon surface. The LIA was performed at 25 °C in 0.5 M H_2SO_4 under 150 W m^{-2} illumination and constant bias voltage until the aluminium was fully anodised. A subset of wafers was annealed at 400 °C in a quartz tube furnace in nitrogen. The purpose of the anneal was to reduce recombination at the silicon/SiO_2 interface caused by current tunnelling though the intervening oxide during the LIA process as described in the previous sections of this chapter and in [127]. Another subset of the anodised wafers was annealed at either 400 °C or 700 °C in air using a Centrotherm belt furnace. The 400 °C anneal was performed at a belt speed of 4000 mm min^{-1} with six heating zones all set to 400 °C, which corresponded to the wafers being exposed to the peak temperature for ~ 45 s. The 700 °C anneal was performed at 5400 mm min^{-1} belt speed with gradually increased temperature and only the last two heating zones set at 700 °C. This corresponded to wafers being exposed to the peak temperature for ~ 4 s to simulate the metallisation firing process. The use of the belt furnace anneal was to investigate an alternative in-line process that simplified the batch process of the tube furnace anneal. The *n*-type emitter surface remained passivated with the thermal SiO_2 for all experiments with current tunnelling from the semi-transparent anode through this oxide.

The bulk lifetime of wafers was measured as described in Section 5.6.1. One-sun iV_{oc} acquired by PC measurement was used as an indicator of the passivation quality for all test structures [294]. The Q_f and D_{it} of the SiO_2/AAO dielectric stack were determined by contactless *C*-*V* measurements using a Semilab PV-2000 [351, 352].

6.3.2 Results and Discussion

As shown in Figure 6-13(a), the D_{it} of the SiO_2/AAO dielectric stacks was relatively high (4×10^{12} cm^{-2} eV^{-1}) immediately after LIA, presumably due to current tunnelling through the intervening SiO_2 on both surfaces. However it was reduced significantly by the subsequent annealing processes. The lower annealing temperature of 400 °C, regardless of the ambient used, was found to be more effective than the 700 °C anneal. Surprisingly, the 400 °C anneal using a belt furnace was found to be

more effective than the nitrogen anneal in the tube furnace at the same temperature, with a very low D_{it} in the range of 1×10^{10} cm^{-2} eV^{-1} being measured. This D_{it} was even lower than that obtained from the SiO_2/SiN_x dielectric stack deposited by PECVD after firing in an industrial belt furnace [304].

Interestingly, Figure 6-13(b) shows that the Q_f follows the same trend as the D_{it} for most cases. The Q_f immediately after LIA was the highest of all measurements. This may be due to the accumulation of cations in the dielectric layer in the vicinity of the SiO_2/AAO interface. Subsequent annealing steps may act to redistribute these charges and therefore reduce the interface charge density. After annealing, a higher Q_f ($+1\times10^{12}$ cm^{-2}) was detected at the higher temperature annealing of 700 °C. This result was consistent with the trend observed by Grant *et al.* [291]. The higher D_{it} was believed to be caused by the high Q_f, since increased Q_f can result in an increase of the neutrally-charged dangling bonds at interface, and therefore increase of D_{it} [353]. However this explanation could not completely explain the behaviour observed for wafers annealed in nitrogen, were the lowest Q_f was measured but that measurement did not correspond to the lowest D_{it} as the D_{it} value that was measured was higher than the belt furnace annealed wafers at the same temperature. The iV_{oc} of corresponding wafers is shown in Figure 6-13(c). They follow an inverse trend with D_{it}, the most effective surface passivation was demonstrated by wafers annealed at 400 °C. This suggested that the high iV_{oc} values were primarily due to the low D_{it} rather than a high Q_f. This is an instructive result as it demonstrates the importance of a low D_{it} for high quality surface passivation.

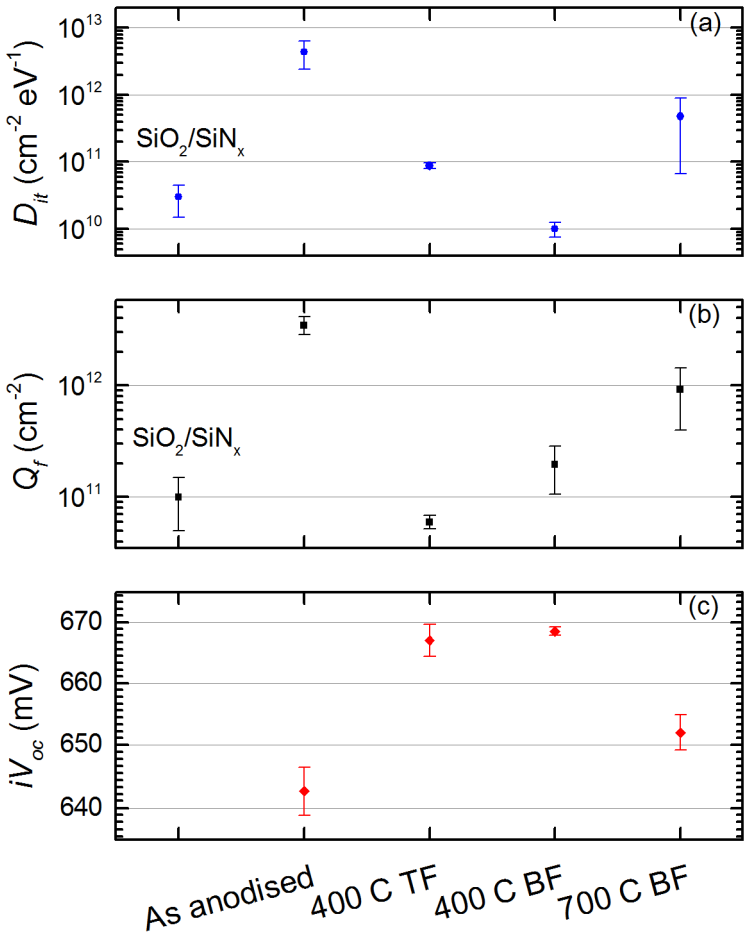

Figure 6-13 (a) Measured D_{it}, (b) Q_f, and (c) iV_{oc} of wafers passivated by a SiO_2/AAO dielectric stack after LIA and after annealing in nitrogen with a tube furnace (TF) at 400 °C and in air using a belt furnace (BF) at 400 °C or 700 °C. The error bars represent the maximum range of measurements on 3 wafers. The D_{it} and Q_f of a 75 nm SiO_2/SiN_x dielectric stack after industrial firing process are presented as a reference.

Table 6-1 compares the D_{it} and Q_f measured from passivated *p*-type silicon surfaces with a variety of passivation dielectrics. Although dielectrics with negative charges (e.g., Al_2O_3 [111]) are reported as a preferred material for *p*-type silicon surface passivation due to accumulation of majority carriers at the interface, it has been shown that a positively-charged dielectric can also effectively passivate boron emitters provided that the Q_f is less than + 1 × 10^{12} cm^{-2} and the D_{it} remains low [304]. Compared to SiO_2 and Al_2O_3 deposited by PECVD and ALD, AAO-passivated *p*-type surfaces demonstrate the lowest D_{it}, and a moderate Q_f of + 2 × 10^{11} cm^{-2}, indicating its potential to be effective passivation dielectrics for *p*-type silicon.

Table 6-1 Comparison between D_{it} and Q_f measured for *p*-type silicon surfaces with various dielectric layers.

Passivation Dielectrics	D_{it} (cm^{-2} eV^{-1})	Q_f (cm^{-2})	Reference
17 nm thermal SiO_2/300 nm AAO	1×10^{10}	$+2\times10^{11}$	This work
15 nm PECVD SiO_2/70 nm PECVD SiN_x	3×10^{10}	$+6\times10^{10}$	[304]
30 nm H_2O-ALD Al_2O_3	4×10^{10}	-1.3×10^{12}	[354]
30 nm Plasma-ALD Al_2O_3	8×10^{10}	-5.6×10^{12}	[354]
30 nm O_3-ALD Al_2O_3	1×10^{11}	-3.4×10^{12}	[354]
10 nm PECVD SiO_2	7×10^{12}	$+2\times10^{12}$	[355]
10 nm PECVD SiO_2/30 nm ALD Al_2O_3	$<1\times10^{11}$	$+1\times10^{11}$	[355]
50 nm PECVD AlO_x	1.7×10^{11}	-2.1×10^{12}	[356]
105 nm thermal SiO_2	4×10^{9}	$+7\times10^{10}$	[357]

6.3.3 Conclusions

It is demonstrated that when AAO layers are formed over a thin SiO_2 layer by LIA of aluminium, they effectively passivate the *p*-type surfaces of silicon wafers with the D_{it} measured to be as low as 1×10^{10} cm^{-2} eV^{-1}. This value is even lower than the latest reported values of PECVD SiO_2/SiN_x dielectric stacks [304], SiO_2/AlO_x dielectric stacks [356] and ALD AlO_x [354, 355]. Effective surface passivation using SiO_2/AAO dielectric layers requires a post anodisation anneal process, which was found to be most effective at 400 °C. Annealing after LIA significantly reduced both the D_{it} and Q_f at the silicon/SiO_2 interface, with low D_{it} values corresponding to high iV_{oc} values. The effective surface passivation provided by AAO layers, formed using LIA, may find applications in the electronic passivation of silicon surfaces. With an ultra-low D_{it}, AAO layers formed by LIA of aluminium can potentially be used in the passivation of boron-doped emitters of silicon solar cells and *p*-type silicon surfaces in general.

6.4 Anodic Aluminium Oxide Composition

If AAO layers formed by LIA of aluminium are to be used as rear passivation layers they need to able to be formed with uniform thickness and physical properties over the entire surface of 156 mm × 156 mm wafers. It has been shown in earlier sections of this chapter that one of the advantages of AAO layers formed by LIA is that the entire wafer surface can be immersed in electrolyte and anodised. Consequently,

unanodised regions which can result in clip anodisation (e.g., see Figure 6-9) are avoided.

This section reports on investigations into the physical properties of AAO layers, formed by LIA of aluminium. Characterisations show that AAO layers formed by LIA of aluminium are stoichiometric and of high uniformity in both thickness and n_r over the area of a 40 mm × 40 mm wafer fragment.

6.4.1 Experimental

Double-side polished boron-doped 1 - 10 Ω cm Cz silicon wafers of thickness of 190 µm were phosphorus-diffused to form 100 Ω/□ emitters. The phosphosilicate glass was removed by immersion in 1% (w/v) HF, and then the rear parasitic emitter was removed by immersing the wafers in 'Trilogy Etch' [221] for 5 min while the emitter surface was protected by photoresist. After the removal of photoresist in 'piranha etch' (H_2SO_4: H_2O_2 = 3: 1), a SiO_2 layer of 17 ± 1 nm thickness was formed by dry oxidation at 980 °C for 18 min in a quartz tube furnace followed by thermal evaporation of a 300 nm layer of 5N purity aluminium on to the *p*-type silicon surface. Light-induced anodisation of the aluminium was performed at 25 °C in 0.5 M H_2SO_4 under 150 W m^{-2} illumination and constant bias voltage between anode and cathode until the aluminium was fully anodised. The final AAO layer was ~ 313 nm thick due to volume expansion that occurs during anodisation [278].

After LIA, the wafers were rinsed in DI water to remove traces of electrolyte and dried by a nitrogen purge. The thickness of the AAO was measured by ellipsometry using an Ellipsometer and the software package WVASE [358] was used to develop an effective medium model of the SiO_2/AAO stack layer. X-ray photoelectron spectroscopy was performed using XPS ESCALAB250Xi (Thermo Scientific) after annealing to investigate the elemental profile of the layers. The cross-sectional microstructure was imaged by Phillip CM200 TEM.

6.4.2 Results and Discussion

The schematic representation of an experimental wafer is illustrated in Figure 6-14. Figure 6-15 shows an XPS depth profile of the formed AAO layer. It is compositionally uniform through the entire layer with the aluminium to oxygen stoichiometry slightly less than 2:3. In Figure 6-3, the cross-sectional microstructure of the layer is shown in a TEM image. During anodisation a non-porous barrier layer

formed under the porous layer [278], suggesting that the LIA process is mechanistically similar to the clip-based anodisation process. In the AAO layer shown in Figure 6-3, the barrier layer was estimated to be 11.5 nm thick and was uniform in thickness across the imaged region.

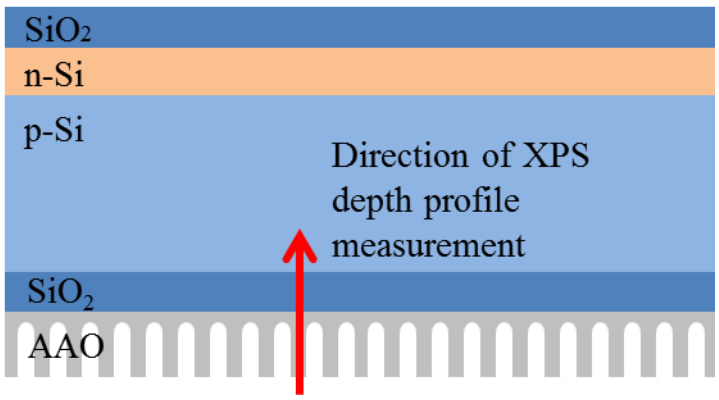

Figure 6-14 Schematic diagram of AAO passivated wafers on which the characterisations were performed. X-ray photoelectron spectroscopy depth profile.

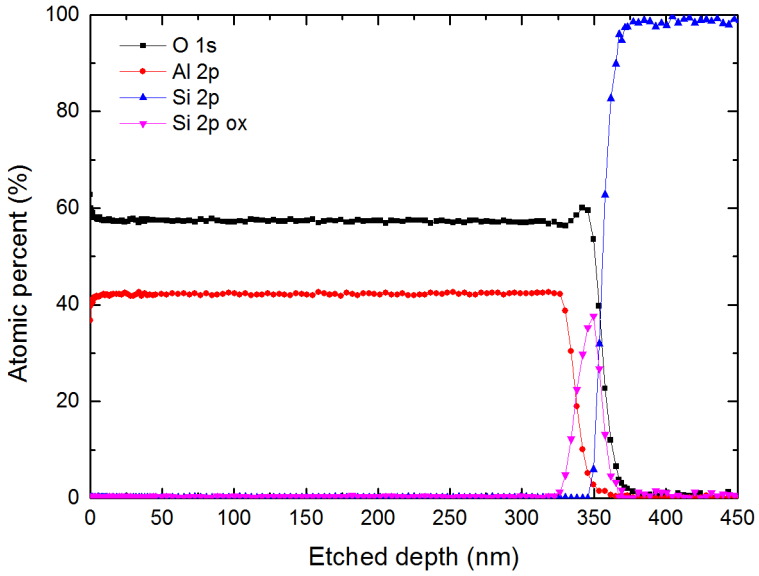

Figure 6-15 XPS depth profile of an AAO layer formed by LIA of a 300 nm aluminium layer. The “Si 2p” refers to the non-oxidised silicon and “Si 2p ox” represents the silicon in the + 4 oxidation state. The “Al 2p” refers to the oxidation state of aluminium.

Table 6-2 summarises the physical properties of an AAO layer, anodised from a 300 nm layer of aluminium, obtained from ellipsometry measurements. The standard deviation is obtained from five points measured across the wafer surface. The variation range, calculated by Equation 6.1, determines the maximum variation of each physical

parameter. Variation range less than 3% is demonstrated in film thickness, n_r and porosity, highlighting the high uniformity of the formed AAO layer.

$$\text{Variation range}\,\% = \frac{Max - Min}{Average} \times 100\% \tag{6.1}$$

A multi-layer WVASE model [358] was developed from ellipsometry measurements of the AAO layer. The structural model for ellipsometry in WVASE was established based on the TEM cross-section of the samples. The layered structure assumed was silicon/SiO_2/barrier AAO/porous AAO, as shown in Figure 6-3. The barrier AAO was treated as an EMA layer consisting of Al_2O_3 and aluminium, anticipating the possible existence of residual aluminium which was not fully anodised. The porous AAO was treated as an EMA layer consisting of Al_2O_3 and voids. Although the pore walls of the porous AAO layer may contain a gradient in density [359], the assumption of homogeneity for the AAO layer did not affect the ability of the model to generate the ellipsometry measurement data, with the simulated n_r being within the expected range and layer thickness matching well with the TEM image.

Diffusion lengths exceeding 400 μm can be routinely-achieved for Cz boron-doped silicon wafers which are electronically-passivated on both surfaces [360]. This means for the 180-200 μm thick wafers that are commonly-used in solar cell fabrication, electrons generated by light absorption anywhere in the wafer can diffuse to the junction to be collected leaving holes to drift to the *p*-type surface and contribute to the anodisation current. The uniformity of the formed oxide is ensured by uniform generation of carriers across the entire area of the wafer.

Table 6-2 Physical properties of an AAO, formed by LIA of 300 nm of aluminium, measured by ellipsometry. The standard deviation and maximum percentage error represent the error of five points measured across the wafer.

Parameters	Values	Variation Range
Barrier Layer Thickness (nm)	11.5 ± 0.1 nm	2.60%
Porous Layer Thickness (nm)	301.6 ± 3.5 nm	2.82%
n_r @ 600 nm	1.53 ± 0.00	0.26%
Porosity	19.8% ± 0.2%	2.53%

6.4.3 Conclusions

This section reported on investigations into the composition and uniformity of AAO layers formed by LIA of aluminium. It is shown that the AAO layer is stoichiometric, with aluminium to oxygen ratio slightly lower than 2:3. The variation ranges of thickness and n_r of the AAO layer over the area of a 40 mm × 40 mm wafer are 2.6% and 0.26%, respectively. The high uniformity of AAO layers formed by LIA, coupled with the electrical properties reported in Section 6.3, make these AAO layers a suitable candidate for rear surface passivation.

6.5 Fabrication of PERC Solar Cells

In recent years, PERC cells have demonstrated significant success in improving cell efficiency, due to reduced rear surface recombination and enhanced light absorption resulting from the presence of a dielectric layer on the rear surface [361, 362]. Having successfully developed the LIA of aluminium process, attention was turned to exploring the possibility of replacing the PECVD AlO_x/SiN_x rear passivation dielectric stack of PERC cells with a SiO_2/AAO dielectric stack, as the latter dielectric stacks have been demonstrated to effectively passivate *p*-type silicon surfaces. This section presents a PERC cell design featuring boron laser-doped linear openings through a SiO_2/AAO dielectric stack with sintered aluminium being used to make electrical contact. Open circuit voltages as high as 660 mV were achieved, which is comparable to voltages achieved from cells with PECVD AlO_x/SiN_x dielectric stack [22, 24]. This section presents initial cell results, identifies problems in the cell fabrication process and suggests possible solutions that could be examined in future work.

6.5.1 Experimental

Cells were fabricated using ~ 180 µm thick, boron-doped 3 - 5 Ω cm Cz silicon wafers. The wafers were phosphorus-diffused by an industrial partner using an industrial $POCl_3$ furnace to an emitter sheet resistance of 80 Ω/□. The rear surface of the wafers was planarised by immersion in 25% (w/v) NaOH (J.T. Baker) at 80 °C for 6 min (reducing the wafer thickness to ~ 170 µm), followed by dry oxidation at 950 °C to form a ~ 10 nm SiO_2 layer on both surfaces. A SiN_x layer was then deposited on the *n*-type emitter by remote plasma PECVD (Roth & Rau AK 400), and a layer of 300 nm aluminium of 5N purity was evaporated on the p-type surface.

The front ARC was laser-doped using 85% (w/w) H_3PO_4 (J.T. Baker) and then the 300 nm thick aluminium layer was anodised using LIA [243] to form an AAO layer. Lines spaced 1 mm apart were laser-doped using a boron spin-on source (PBF-1, Filmtronics) through the rear SiO_2/AAO dielectric stack. Laser doping was performed using a 532 nm CW laser with a power of 15 W and speed of 0.5 m s^{-1}, and then 2 µm of aluminium was deposited by thermal evaporation on the rear surface as the rear electrode. Cells were annealed in a quartz tube furnace in nitrogen at 450 °C for 20 min to reduce the barrier height associated with current flow to the aluminium [363] and form an ohmic contact. The front surface was then metallised by LIP of nickel and copper as described in [229].

This cell fabrication process is summarised in Figure 6-16. Compared to the PECVD AlO_x/SiN_x passivated solar cells, the SiO_2/AAO passivated cell eliminated the PECVD deposition process by introducing the aluminium evaporation and anodisation processes.

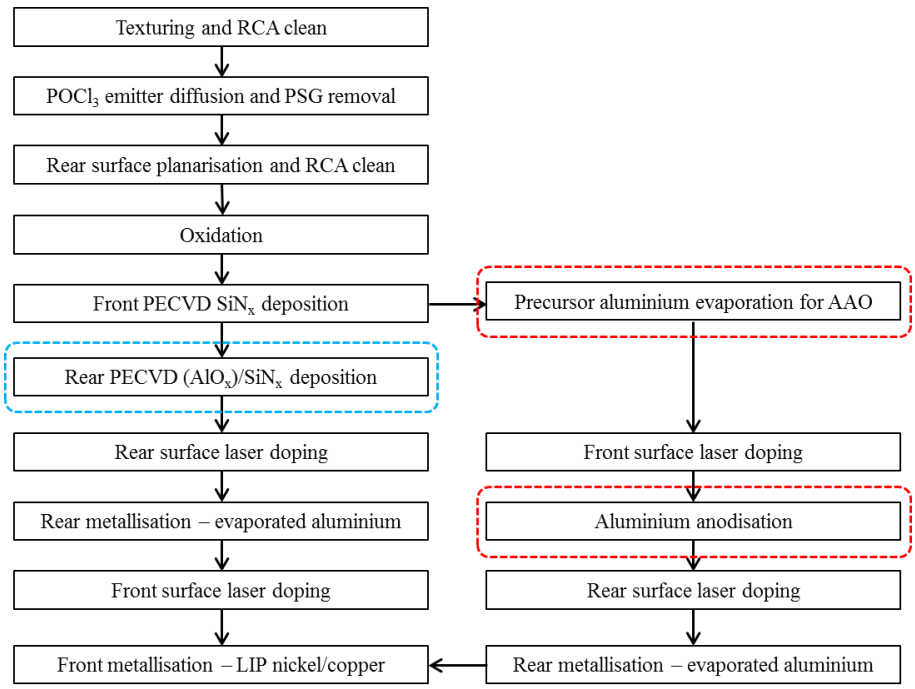

Figure 6-16 Process flow used for the AlO_x/SiN_x passivated PERC cells (left) and SiO_2/AAO rear passivated PERC cells (right) fabrication. The two steps in red circles are extra steps replacing the step in blue circle.

A cross-section schematic of the final cell structure is shown in Figure 6-17. After edge isolation, the cells had an effective area of 6.25 cm^2 and were characterised by light and dark *I-V*, spectral response, reflectance and Suns-V_{oc}. The cells were placed

on a copper block during *I-V* measurement, which was expected to remove any R_s component from the rear aluminium layer being thin.

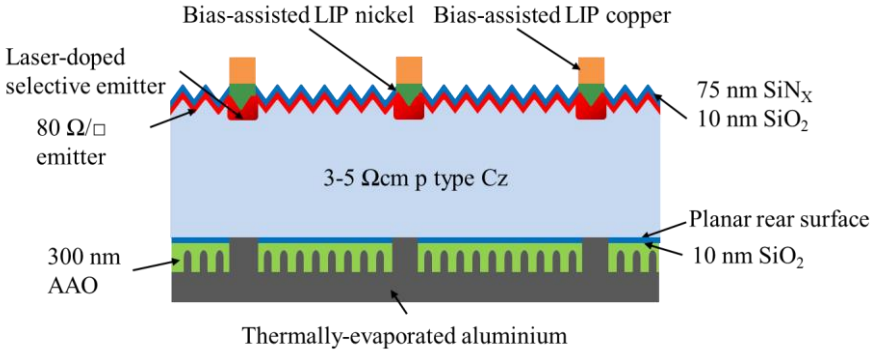

Figure 6-17 Cross-section schematic of the SiO_2/AAO rear passivated cell. Metal finger spacing on the front emitter was 0.8 mm and the local line contacts on the rear surface were spaced 1 mm apart.

6.5.2 Results and Discussion

6.5.2.1 Electrical Characterisation

The *I-V* data, *pFF* as measured by Suns-V_{oc}, *m* at the V_{mp} and R_s and for the most efficient AAO-passivated cell and the mean of four cells are summarised in Table 6-3. The effective R_s was estimated from luminescence based R_s imaging [364]. These results are compared to two reference cells. 'Ref A' was also a PERC cell with the LIP nickel/copper front metallisation, identical to the AAO-passivated cells but having a PECVD AlO_x/SiN_x rear surface passivation layer. The rear metallisation was realised by screen-printing aluminium paste and firing at high temperatures. 'Ref B' was a standard screen-printed cell with full-area aluminium BSF and silver grids on the front.

Table 6-3 Electrical characterization of the AAO rear passivated cells in comparison to two reference cells.

	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF* (%)	η (%)	*pFF* (%)	m^a @ V_{mp}	R_s (Ωcm^2)
Best η	655	38.5	71.0	17.8	82.0	2.0	1.7
Best V_{oc}	660	39.5	67.0	17.4	81.6	1.8	1.8
Mean	656	38.6	70.2	17.6	81.8	2.1	1.6
Ref A[b]	655	40.2	76.1	20.0	N/A	1.71	0.68
Ref B[c]	626	37.3	78.8	18.4	N/A	1.36	0.50

[a] *m* is the local ideality factor.

[b]Ref A: A PERC cell using PECVD AlO_x/SiN_x rear surface passivation, laser doping and LIP nickel/copper front contacts. Rear metallisation was realised by screen printing aluminium and firing at 800 °C [365].

[c]Ref B: A standard screen-printed cell with full-area aluminium BSF and silver grids on the front surface [365].

Rear Surface

As shown in Table 6-3, an average cell V_{oc} of 656 mV was achieved for cells with rear surface SiO_2/AAO layers. This represents a ~ 30 mV increase from the screen-printed reference cell, Ref B, and was attributed to a reduced rear *SRV*. The improvement from the front surface was limited because of the reasonably heavily doped emitter. Since a similar V_{oc} improvement was also observed for Ref A, it was concluded that the SiO_2/AAO dielectric stack can provide similar levels of rear surface passivation to a PECVD Al_2O_3/SiN_x dielectric stack. The improved rear surface passivation was also evidenced in the *QE* measurement (see Figure 6-18). The measured long wavelength *IQE* of the most efficient SiO_2/AAO passivated cell at long wavelength was marginally better than Ref A, with an *IQE* of 98% for 1000 nm and 60% for 1100 nm wavelength light being achieved.

The reflectance measured at 1200 nm was 57%, higher than the reflectance of 43% measured for Ref A. This may be due to three causes. First, the alkaline-planarised rear surface may have resulted in higher internal reflectance than a surface prepared by the industrial acidic rear etching (as used by Ref A) [21, 23]. With the industrial acidic rear etch only the peaks of textured pyramids were rounded, whereas a more polished surface can result with the alkaline planarisation. Second, the low temperature sintering prevented contact region expansion that occurs when aluminium is alloyed at high temperatures [171]. Finally, evaporated aluminium may have acted as a better rear reflector than fired screen-printed aluminium.

Front Surface

The width of the front metal fingers was ~ 35 µm, reduced from ~ 100 µm for the screen-printed fingers. The narrower finger width allowed fingers to be spaced 0.8 mm apart across the 80 Ω/□ emitter, reducing the front surface broadband reflection and improving the short wavelength light response. The front surface reflection was reduced to 3.6% resulting in 1.3 mA cm^{-2} higher J_{sc} than the screen-printed cell.

Although the AAO passivated cells had improved long wavelength response, the mean J_{sc} of cells was 1.6 mA cm^{-2} lower than that of Ref A. The cell J_{sc} was limited by the poor short wavelength response, which is evidenced in Figure 6-18 where the *IQE* of the AAO-passivated cell was degraded significantly in the sub 580 nm wavelengths. At 300 nm, the *IQE* of Ref A was 73%, compared to only 27% for the AAO-passivated cell.

Another notable difference was in the reflectance at short wavelength. This was attributed to strong absorption in the front SiN_x deposited with the laboratory PECVD system. The SiN_x of the AAO-passivated wafers showed higher reflection in the range of 400 - 600 nm. Although the reflectance appeared low in the sub 400 nm ranges, it was attributed to higher absorption, which was also demonstrated by an optical loss analysis (see Figure 6-19) for the most efficient AAO-passivated cell. Furthermore, the poor short wavelength response can also be caused by an increased emitter recombination in the more heavily-diffused emitter (80 Ω/□) of the AAO cell, which would have reduced slightlythe carrier collection from within the emitter. However, this contribution was considered to be small compared to the absorption in the ARC. This is because the emitter with such high recombination would have to be several micrometres deep to achieve a V_{oc} of 660 mV, rather than the 0.5 µm measured by electrochemical capacitance-voltage (ECV) profiling.

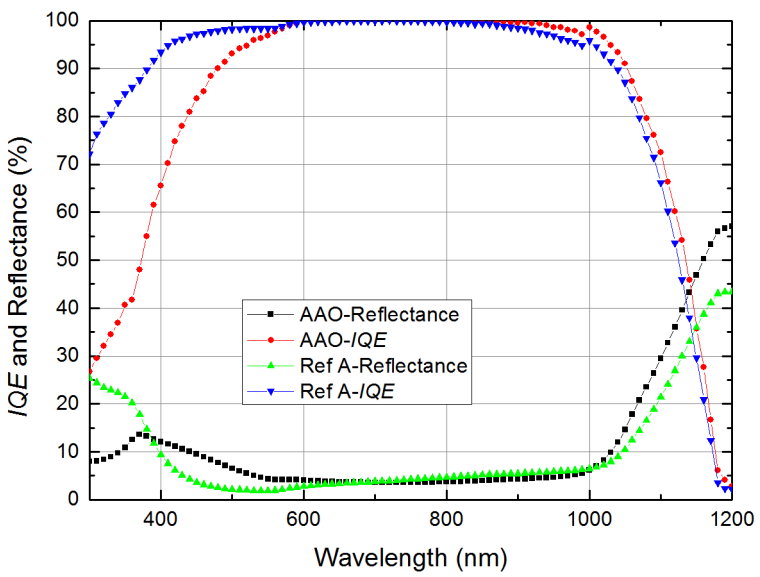

Figure 6-18 *IQE* and reflectance of the most efficient AAO-passivated cell from Table 6-3 and Ref A. Improved *IQE* and reflectance at long wavelength indicates effective rear surface passivation and displaced rear reflector, respectively.

6.5.2.2 Optical Loss Analysis

In order to gain an insight into the losses associated with the J_{sc}, a detailed optical loss analysis [366] was performed for the most efficient AAO-passivated cell. In Figure 6-19, the optical losses of the cell are decoupled into different loss mechanisms. The boundaries of the coloured areas from the bottom to the top are external quantum efficiency (*EQE*) and 1-Reflectance. The black dashed line at 1107 nm in Figure 6-19 is showing the upper limit of light determined by the silicon band gap. Light of longer wavelengths was not considered in the photon counting. Therefore the maximum possible J_{sc} was calculated by integrating the AM 1.5G spectrum from 300 to 1107 nm assuming 100% *EQE*. The fraction of incident light converted to current and lost was calculated by integrating the product of *EQE* and the AM 1.5G spectrum with respect to the wavelength. The percentage loss of each section was calculated with respect to the maximum possible J_{sc}. A summary of the J_{sc} losses is presented in Table 6-4. The green area under the *EQE* curve represents the effective absorption of light, which corresponds to 88.7% of the spectrum from 300 to 1107 nm being converted into current by the cell. The resulting calculated J_{sc} is 38.8 mA cm^{-2}, which is slightly higher than that measured by light *I-V*

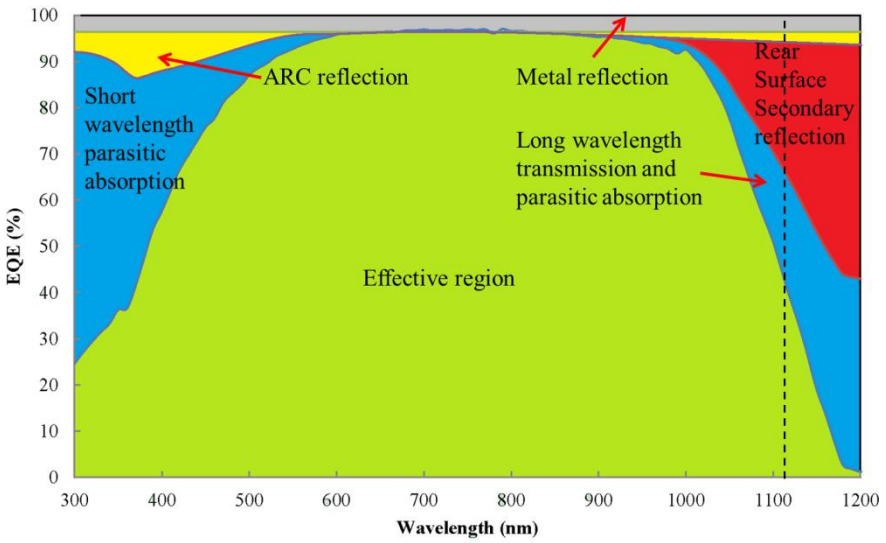

Figure 6-19 *EQE* and 1-Reflection of the most efficient AAO-passivated cell. The faction of incident light lost to various mechanisms is shown as coloured regions.

The green area under the *EQE* curve represents the effective absorption of light, which corresponds to 88.7% of the spectrum from 300 to 1107 nm being converted into

current by the cell. The resulting calculated J_{sc} is 38.8 mA cm^{-2}, which is slightly higher than that measured by light *I-V*.

Table 6-4 Decoupled J_{sc} losses due to various mechanisms for the most efficient AAO-passivated cell.

Loss Mechanism	J_{sc} Loss (mA cm^{-2})	Percentage Loss (%)
Short wavelength absorption	1.72	3.9
Long wavelength absorption	0.62	1.4
ARC reflection	0.70	1.6
Metal reflection	0.16	0.4
Rear surface secondary reflection	0.66	1.5

The largest source of optical loss is the parasitic absorption in the cell shown as the blue region in Figure 6-19. At short wavelength, a significant fraction of the J_{sc} (~ 1.72 mA cm^{-2}) is lost due to absorption at the front surface. As discussed in Section 6.5.2.1, this is attributed to the absorption in the ARC and, to a lesser degree the recombination in the relatively heavily-doped emitter. This loss is the main difference in the optical loss of the AAO-passivated cells in comparison with Ref A. At long wavelength, the blue region represents both absorption and transmission loss. Due to improved rear surface passivation by SiO_2/AAO and the presence of a dielectric displaced rear reflector, this fraction of loss was limited to 0.62 mA cm^{-2}.

The second largest loss is attributed to reflection, either due to front metal grids or ARC. The metal reflection only contributes 0.4% of the total loss due to narrow metal fingers by laser-doping and LIP nickel/copper. Narrow metal fingers of 30 μm reduced the metal contact fraction to 3.6% on the front surface.

The rear surface secondary reflection loss is unavoidable in silicon solar cells. It increases with the increased long wavelength reflection. The improved secondary reflection also increases the possibility of long wavelength light absorption and hence improved the *EQE*.

Compared to Ref A, which was fabricated on similar silicon wafers and achieved a J_{sc} of 40.2 mA cm^{-2}, it was concluded that the main difference in the J_{sc} of the AAO-passivated cell was due to the optical loss in the absorbing ARC and the more heavily-diffused emitter.

6.5.2.3 Fill Factor Losses

The electrical characterisation of the AAO-passivated cell shows that another limiting factor of the cell efficiency is the low *FF*. A low *FF* can result from a high R_s, low R_{sh}, and/or a high *m* values at the maximum power point (i.e., V_{mp}). The different potential causes of the low *FF* are examined below.

Series Resistance Losses

One contribution to the low *FF*s of the AAO-passivated cells was clearly the high R_s. The mean R_s was 1.6 Ω cm^2 compared to 0.68 and 0.6 Ω cm^2 for Ref A and Ref B, respectively (see Table 6-3). The total R_s of a silicon solar cell includes: (i) front grid resistance; (ii) front R_c; (iii) emitter lateral resistance; (iv) bulk resistance (including spreading resistance [367]); (v) rear R_c; and (vi) rear metal resistance. In PERC cells, the R_s is usually higher due to the presence of local contacts and lateral current flow in the bulk. The spreading resistance caused by current crowding at the rear local contacts increases the bulk resistance [367]. Therefore the R_s of PERC cells is primarily determined by the rear local contact configuration (e.g., line spacing) and the rear R_c.

The line spacing of the rear local contacts was not found to be a significant contributor to the high R_s for the AAO-passivated cells, because the R_s of Ref A cell was 0.68 Ω cm^2 with identical line spacing. Therefore, the higher R_s was assumed to be due to a high rear R_c. It was hypothesised that a resistive boron glass may have formed in the rear laser-doped line openings during the laser doping. Laser-doping using a boron spin-on-source has been shown to result in a high concentration of boron at the surface, see Figure 6-20(a) and [207]. This boron layer would most likely coincide with a high oxygen content region, with oxygen being incorporated into the laser-doped layer from both the AAO and the polyboron dopant source.

For the Ref A cell, screen-printed aluminium was fired at 800 °C to form an LBSF and in doing so any resistive boron-rich layer would have been disrupted and removed by the alloying reaction. For the AAO-passivated cell, however, the rear metallisation was performed by annealing evaporated aluminium at 400 °C, a temperature which was lower than the aluminium-silicon alloying temperature. The presence of a boron-rich layer may have prevented the formation of the ohmic contacts, with a MIS structure forming at the surface which may have significantly increased the R_c.

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Figure 6-20 (a) Secondary ion mass spectroscopy (SIMS) profile of 4 cm^2 regions that were formed by scribing laser through a spin-coated polyboron dopant source (applied over a rear SiN_x layer) with lines 20 µm apart using a 532 nm, 15 W laser with speed of 0.5 m s^{-1}. (b) ECV profiles showing the electrically-active *p*-type dopant concentration similar 4 cm^2 regions formed by laser-scribing through spin-coated poly boron dopant source applied over a rear SiN_x layer (red circles) and through an AAO layer without dopant source (black squares). (reproduced from [207])

To reduce R_s, any possible boron rich layer must be removed before metallisation. Lu *et al.* have demonstrated that the AAO layers can act as an effective dopant source during laser scribing with the electrically-active *p*-type dopant concentration exceeding 10^{20} cm^{-3} for the first 6-7 µm of the formed *p*+ region [see Figure 6-20(b)]. Therefore, rather than performing boron laser doping, the local *p*+ region can be formed by laser scribing through the AAO layer, with that layer being the dopant source. This process has been shown to be more effective if aluminium is anodised in an electrolyte containing boron [207]. Eliminating the need to use the polyboron dopant source is beneficial because it simplifies the process as the dopant source coating, laser doping and rinsing is combined into a single process of laser scribing through the AAO. Additionally, laser-doping through polyboron source can result in vapours which are harmful to humans [208]. If boron can be incorporated into an AAO layer during anodisation and introduced, with aluminium, into the underlying silicon, heavily-doped *p*+ regions can be formed by simply laser melting the AAO layer [207].

Even without the use of boron source, the laser scribing process is believed to form a thin oxide layer during silicon recrystallization in the laser-patterned grooves [170]. Although this thin SiO_2 layer is not as resistive as the boron rich layer, it still increases the R_c if not dissolved during metallisation or removed before metallisation. In future work, the laser-doped surfaces should be treated before metallisation to remove this layer.

Local Ideality Factor Losses

Another cause of the low *FF* is the high value of *m* at V_{mp}. It can be attributed to three major causes: (i) increased dark saturation current density of $n = 2$ (J_{02}) due to

damage created by laser edge isolation; (ii) injection level dependent rear *SRV* results due to positive charge in the rear passivation dielectric; and (iii) defects introduced by the boron laser doping process.

As shown in Figure 6-21 (also see Table 6-3), the mean *m* value at V_{mp} was 2.1 for AAO-passivated cells and 1.5 for Ref A, both were high when compared to the value of one expected under ideal diode conditions. Although laser-induced damage during laser edge isolation of cells was reported to increase the cell edge recombination and hence J_{02} [368], a low *m* value of 1.36 was observed in Ref B which was also laser edge isolated identically to the AAO-passivated cell and Ref A. Therefore, it was concluded that the edge recombination caused by laser edge isolation may have increased the *m* value at V_{mp}, however there must have been other contributions as well. The edge recombination problem can be resolved by *p*-type laser-doping around the cell perimeter of the cell before depositing the SiN_x as described in [369]. Future work could use this technique to establish the contribution of edge recombination to the high *m* value at V_{mp}.

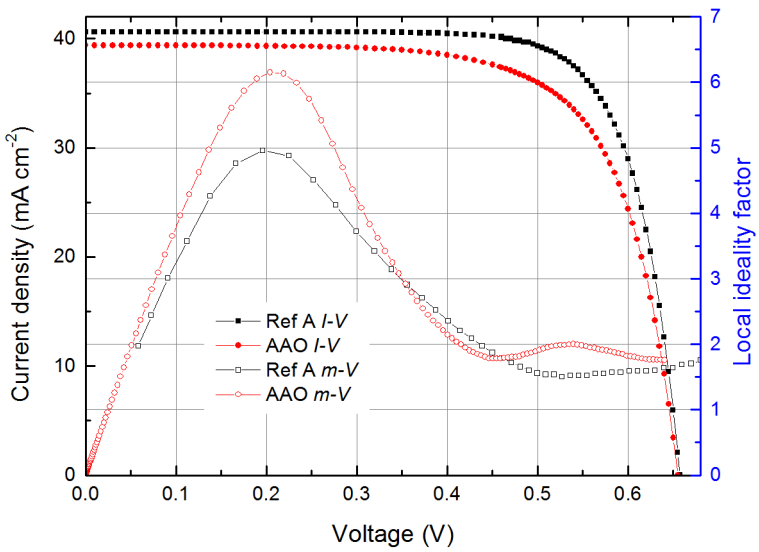

Figure 6-21 *I-V* and *m-V* curves of the most efficient AAO passivated cell and Ref A.

Many studies have shown that the positive electrostatic charge in the *p*-type surface passivation dielectrics results in a floating-junction effect [44] and an injection level dependent rear *SRV* [110, 288, 370]. As illustrated in Figure 6-22(a), Wang *et al.* showed that a SiO_2/SiN_x dielectric stack, which has stored positive charges, resulted in a dramatic increase in *m* value from 1.5 to 2.3 at V_{mp}. This injection-level dependent rear

SRV was also evident in the degradation of the long wavelength *EQE* without a bias light (i.e., at low injection) [371] (see also Figure 6-22).

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Figure 6-22 (a) *m*-*V* curve; and (b) *EQE* measured from a cell with SiO_2/SiN_x rear passivation and a cell with AlO_x/SiN_x rear passivation. The blue and red curves in (b) are showing the *EQE* measured with and without bias light of a SiO_2/SiN_x passivated cell (reproduced from [371]).

Figure 6-23 shows the *EQE* curves of the most efficient AAO-passivated cell with and without a bias light. Degradation in *EQE* without bias light was observed from 700 nm onwards, however the difference between the *EQE* under the two light conditions was much smaller compared to the difference shown in Figure 6-22. The lesser effect was partly attributed to the relatively low Q_f of the SiO_2/AAO stack of $+ 2 \times 10^{11}$ cm^{-2} comparing to $+ 4 \times 10^{11}$ cm^{-2} of SiO_2/SiN_x dielectric stack [44]. The direct comparison to the work of Wang *et al.* draws the conclusion that the positive electrostatic charge in the AAO layer results in an injection level dependent rear *SRV*, but this is not a significant contributor to the high *m* at V_{mp} due to the moderate Q_f of the SiO_2/AAO stack. Recent work of Lu *et al.* demonstrated that the magnitude and polarity of charges accumulated during the anodisation process can be manipulated by controlling the anodisation conditions [372]. Therefore, the impact of positive electrostatic charge can potentially be eliminated if the magnitude, and possibly also the polarity, of the stored charges in AAO layers can be manipulated by careful selection of anodisation conditions.

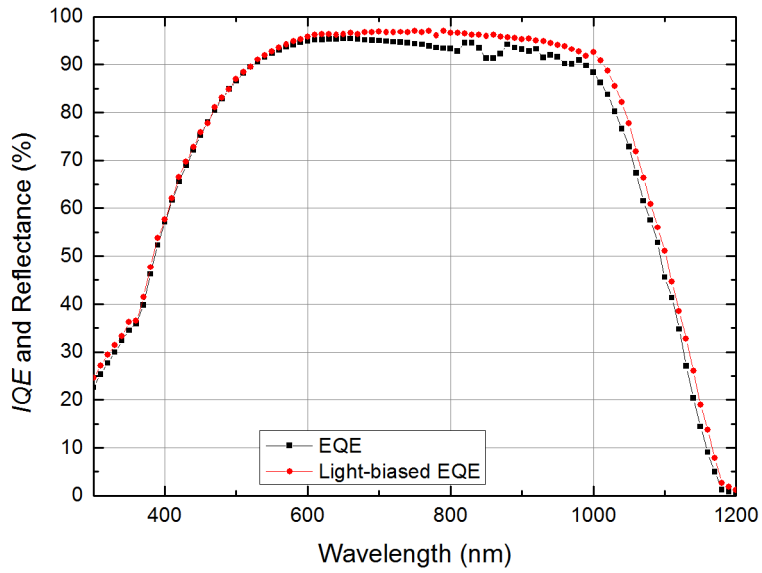

Figure 6-23 *EQE* measured from the most efficient AAO passivated PERC cell with and without the bias light.

A further contributor to the high m at V_{mp} may be the boron laser doping process itself. Wang *et al.* showed that defects induced by boron laser doping introduced additional recombination in cells [373]. Figure 6-24 shows that defects introduced during boron laser doping significantly decreased the τ_{eff} at 1-sun and increased the m at V_{mp} to 1.5. Moreover, the m value cannot be recovered to the initial recombination state even after a subsequent 700 °C anneal. Interestingly, the cells used in Wang *et al.*'s study were passivated by a PECVD AlO_x/SiN_x dielectric stack with the junction edge isolated by boron laser doping around the perimeter of the wafer fragment. In doing so, the two above mentioned m losses were eliminated and hence the increase of m at V_{mp} to 1.5 can be largely attributed to the boron laser doping of the p-type surface. Therefore, for the AAO-passivated cells, one of the obvious ways to reduce this ideality factor loss is to eliminate the boron laser doping process and instead laser scribe through the AAO layer as discussed previously. The AAO layer can provide a source of aluminium dopants and, if anodisation is performed in a boron-containing electrolyte, even higher concentrations of electrically-active dopants can be introduced into the silicon [207]. The elimination of the boron laser doping step would not only directly reduce the value of m at V_{mp} but would also act to reduce the rear R_c and consequently the cell R_s.

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Figure 6-24 (a) Injection level dependent τ_{eff}; and (b) m-iV_{oc} curves for a wafer fragment after different processes [373].

6.5.3 Conclusions

In this section, the fabrication of PERC cells featuring a SiO_2/AAO passivated rear surface and a laser-doped selective-emitter with LIP nickel/copper contacts was presented. The SiO_2/AAO dielectric stack layer was shown to provide excellent *p*-type silicon surface passivation that was comparable to a PECVD AlO_x/SiN_x dielectric stacks, with a maximum cell V_{oc} of 660 mV being demonstrated.

The highest J_{sc} of the initial cells fabricated was 39.5 mA cm^{-2}. It was found to be primarily limited by the short wavelength parasitic absorption in the ARC and, to a lesser extent, increased recombination in the reasonably heavily-doped emitter. The low *FF* was attributed to both high cell R_s and high m at V_{mp}. The high cell R_s was presumably due to the formation of a resistive boron rich layer which may be a consequence of the boron laser-doping process. It can potentially be reduced in three ways. First, the local *p*+ regions could be formed by laser scribing through AAO, with the AAO being the p-type dopant source [207]. Second, the native oxide in the laser-patterned lines could be removed by performing an oxide etch (e.g., a HF dip), however this would need to be performed with care as the AAO layer would also be etched. Furthermore, the R_s can be reduced by patterning the AAO layer by laser or inkjet patterning (as described in Chapter 4) and then firing at temperatures over 700 °C to form aluminium-silicon alloyed LBSF regions. However, with the third option, the firing profile would need to be controlled in a way that could guarantee uniform alloying while preserving the quality of the surface passivation provided by the AAO layer.

The high m at V_{mp} was attributed to three causes: (i) increased J_{02} due to laser-cleaved edge isolation; (ii) injection level dependent rear *SRV* due to positive electrostatic charge in AAO; and (iii) additional recombination introduced by the boron laser doping process. Analysis suggested that the first two causes were of lesser significance than the third cause. This source of loss could be addressed by: (i) fabricating cells on rear-etched 156 mm × 156 mm commercial wafers (i.e., eliminate the need for laser edge isolation); (ii) manipulating the polarity and magnitude of the electrostatic charge in the AAO layer by controlling the anodisation processes; and (iii) replacing the boron laser doping process by laser scribing/doping through the AAO layer. If these sources of losses can be addressed and a J_{sc} of 40.2 mA cm^{-2} and *FF* of 78% can be achieved, then cell efficiencies of ~ 20.7% should be possible.

6.6 Chapter Conclusions

The formation of AAO layers by LIA of aluminium on silicon wafers was investigated for surface passivation applications. It was demonstrated that the LIA technique improved the surface passivation of wafer after annealing in nitrogen at 400 °C compared to clip anodisation. The quality of surface passivation was further improved by eliminating the laser patterning of the *n*-type surface and annealing wafers in oxygen and forming gas at 400 °C. The latter process improved the interface quality of the silicon/SiO_2, resulting in comparable surface passivation to the thermal SiO_2/ PECVD SiN_x dielectric stacks.

The annealing process can be simplified to a process which involves annealing at 400 °C using an industrial belt furnace. Capacitance-voltage measurements showed a very high quality silicon/SiO_2 interface after belt furnace annealing, with a D_{it} of 1×10^{10} cm^{-2} eV^{-1} and the Q_f of $+2 \times 10^{11}$ cm^{-2} being measured. Anodic aluminium oxide layers were found to be thermally-stable at 750 °C, however the quality of surface passivation was found to be sensitive to the uniformity of heating. Therefore it was concluded that AAO-passivated solar cells are preferably metallised at low temperatures (e.g., 400 °C).

Preliminary fabrication results for anodic SiO_2/AAO dielectric stack were presented. The replacement of the thermal oxide with an anodic oxide allows for further cost reductions. One-sun iV_{oc} values exceeding 650 mV were achieved using commercial grade Cz *p*-type wafers and anodic SiO_2 and AAO layers. The final wafer iV_{oc} was found to be sensitive to the quality of silicon/anodic SiO_2 interface. If the AAO layer was grown on an anodic SiO_2 with a silicon/anodic SiO_2 interface of high D_{it} (i.e., low quality), an oxygen and forming gas anneal at the end of the process does not significantly improve the surface passivation.

Finally, the fabrication of AAO-passivated PERC solar cells was described. A mean cell V_{oc} of 656 mV was demonstrated, suggesting that SiO_2/AAO dielectric stacks can provide high quality rear surface passivation. The most efficient cell had an efficiency of 17.8% and was found to be limited by losses in J_{sc} and, to a greater extent, *FF*. Using an optical loss analysis, parasitic absorption in the ARC and a higher recombination due to the reasonably heavily-doped emitter were identified as causes for the low J_{sc}. Two major loss mechanisms which attributed to the low *FF* were identified:

high R_s and high m at V_{mp}. Potential solutions to improve the FF, such as eliminating boron laser doping process, removing native oxide in the local contact area before rear metallisation and manipulating the electrostatic charge were proposed. However, more research is required if the contributions of each of these factors is to be understood more completely.

High-quality passivation, rapid processing and large-area uniformity of AAO layers formed by LIA of aluminium may make these layers a promising alternative passivation material that can further improve the efficiency and reduce the cost of photovoltaic silicon solar cells. Moreover, the ability to achieve rapid and uniform large-area anodisation may find applications beyond silicon photovoltaics in fields such as in passivation of black silicon [337, 338, 374] and other pn-junction devices such as light-emitting diodes [339] or integrated circuits required for large-area display devices [375].

Chapter 7 Conclusions and Future Work

The primary aim of this thesis was to examine possible cost-effective improvements in rear local contact formation for silicon solar cells that could be used in manufacturing, with a special focus on the formation of anodic oxide dielectric layers and patterning of these layers. The study included local contact formation, dielectric patterning and surface passivation. The investigation resulted in the development of a new anodisation technique, LIA, which can be used to form low-cost anodic oxides for silicon solar cell fabrication.

In Chapter 3, the formation of LBSF regions via several dielectric patterning techniques was investigated. The main findings from this chapter were:

1. Aerosol jet etching can effectively pattern 200 nm SiO_2/SiN_x dielectric stacks and can reproducibly achieve etched line widths of 60 - 70 µm. The best patterning resolution was achieved using the 100 µm deposition tip of the AJP with a 2 mm tip-to-substrate distance and a platen temperature of 60 °C.
2. Although laser patterning can cause crystal damage, the damage is mitigated by the high temperature alloying process during which the damaged silicon is dissolved in the aluminium melt. Boron laser doping results in a large S_{limit} that causes thinner LBSF regions and more extensive Kirkendall void formation than laser scribing when fired at 850 ºC. This is attributed to the weaker Si-Si bonds due to the introduced boron dopant atoms.
3. Aerosol jet etching does not damage the silicon and results in 2 – 3 µm thicker LBSF regions than laser patterning with reduced line widening and a reduced percentage of Kirkendall void formation. However, this patterning method has yet to demonstrate reliability, stability and capability to process wafers at industrial throughput.
4. Small area cells (16 cm^2) patterned using AJE achieved a maximum efficiency of 18.5% on commercial grade *p*-type Cz wafer fragments. Two main problems were identified that limited the cell efficiency. First, the redistribution of a thin aluminium layer at high temperatures caused non-uniform LBSF formation, which limited both the cell *FF* and V_{oc}. The V_{oc} was also reduced by aluminium spiking

through the dielectric layer in the non-contact areas. Second, the large contact fraction of the AJE-patterned cells exacerbated the V_{oc} and J_{sc} losses at the rear surface.

Chemical etching (e.g., AJE) was demonstrated as a promising technique for rear dielectric patterning, because it does not result in damage to the crystalline structure. In Chapter 4, a new inkjet patterning technique and process for forming LBSF regions in an AAO layer were reported. The key findings of this chapter were:

1. Piezoelectric DOD inkjet printers can be used to pattern an array of point openings of diameter of 20 - 30 µm in an AAO layer. The opening diameter is determined by the volume of etchant and surface roughness. The etching rate increases with increased temperature, however temperatures exceeding 60 °C can result in excessive evaporation of water in the etchant and hence a reduced etching rate. Successful patterning of 600 nm AAO layers can be achieved on silicon substrates with polished, planar and textured surface morphologies.
2. Local BSF regions with a thickness up to 7 µm can be formed though inkjet-patterned holes in AAO layers. High peak firing temperatures result in thicker LBSF regions, as well as an increased probability of Kirkendall void formation and larger opening diameters. The increase in opening diameter can be minimised by using larger point spacing.
3. The reliability of the patterning was limited by the way the AAO layers were formed (i.e., using clip anodisation). Limitations of the clip anodisation method used to form AAO layers were outlined. First, uniformity of anodisation was strongly dependent on substrate surface roughness. Second, aluminium residue left at the intersection of textured pyramids can result in "spiking" during the firing process. Although the latter phenomenon has been used to achieved self-patterned metal contact regions in [206], in this application it limited the effectiveness of the proposed rear contact scheme.

These limitations of the clip anodisation were resolved by the development of the novel LIA technique. Chapter 4 describes the development of this technique and its application to anodise *p*-type silicon surfaces to grow anodic SiO_2. Key findings of this chapter include:

1. The light-induced current of a solar cell can make the *p*-type surface anodic and initiate the oxide growth. In LIA, the electric field is perpendicular to the substrate

surface, therefore enabling uniform oxide growth. Illumination and bias voltage are two key factors to realise LIA. Bias voltage offsets the resistive losses in the electrochemical circuit and can be used to ensure that the solar cell's operating point is close to short circuit. The illumination determines the anodisation current density.

2. The thickness of the anodic SiO_2 formed by LIA has a parabolic relationship with anodisation time, which is similar to that observed for thermal SiO_2 growth. Thin anodic SiO_2 (e.g., $\leq$ 10 nm) layers are close to stoichiometric, however the layers become silicon rich and less dense with increased thickness.
3. Anodic SiO_2 has excellent physical and electrical properties. Physically, it is highly uniform in thickness and n_r over areas of 16 cm^2. Electrically, it demonstrates a low D_{it} of 6×10^{11} eV^{-1} cm^{-2} and a very low Q_{eff} of $+ 3.4 \times 10^{11}$ cm^{-2}. Furthermore, low leakage current densities of 3.5×10^{-10} and 1.6×10^{-9} A cm^{-2} were measured at 1 and -1 V, respectively. These values are six orders of magnitude lower than for a thermal SiO_2 layer of equivalent thickness.
4. Comparable τ_{eff} values to thermal SiO_2 layer can be achieved and the τ_{eff} was shown to be stable when moisture ingress was eliminated by application of a capping dielectric layer. The excellent surface passivation and low leakage current density enables the application of LIA in growing anodic SiO_2 for MIS metal contact passivation, epitaxial thin silicon passivation, and barriers for metal plating and PID.

Based on the successful development of LIA of silicon in Chapter 5, the LIA of aluminium was investigated in Chapter 6. It was shown that uniform AAO layers could be formed on large area wafers with most of the limitations of clip anodisation, that were identified in Chapter 4, addressed. The main findings in this chapter were:

1. Higher τ_{eff} values, than achieved using clip anodisation, are possible. It was shown that a high quality silicon/SiO_2 interface is critical to achieving high τ_{eff} for structures with a SiO_2/AAO dielectric stack. Annealing in oxygen and then forming gas at 400 °C for 30 min each results in the highest τ_{eff} values.
2. The SiO_2/AAO dielectric stacks have an D_{it} as low as 1×10^{10} cm^{-2} eV^{-1} and a Q_f of $+2 \times 10^{11}$ cm^{-2}. The surface passivation of AAO formed by LIA is stable after 750 °C firing, although it is sensitive to the uniformity of heating. Moreover, the AAO layer is near stoichiometric with slightly higher oxygen composition. The thickness and n_r are uniform over a wafer area of 16 cm^2.
3. Open circuit voltages of 660 mV can be realised on AAO-passivated PERC cells, fabricated on commercial grade *p*-type Cz wafer fragments. This value is

comparable to the widely-used PECVD AlO_x/SiN_x stack and therefore demonstrates the potential for AAO to be used as rear passivation dielectric.

4. The efficiency of cells fabricated with a SiO_2/AAO rear dielectric stack was limited to 17.8% due to a low J_{sc} (attributed largely to the parasitic absorption in the ARC) and low *FF* (attributed to both the high R_s and high *m* at V_{mp}). Possible solutions to these problems were identified.

7.1 Original Contributions

The original contributions of this thesis are summarised below.

1. The potential of AJE to pattern 200 nm thick SiN_x rear passivation layers for PERC cells was demonstrated resulting in the fabrication of 18.5% efficient AJE-patterned PERC solar cells.
2. A new inkjet patterning technique was developed which can result in the formation of 20 - 30 μm diameter point openings in 600 nm thick AAO layers. The technique was simpler than existing inkjet patterning techniques and induced neither crystal damage nor degraded surface passivation.
3. Limitations of existing anodisation techniques were addressed by the development of a novel LIA technique which significantly improved the anodic oxide uniformity and electrical properties. A patent application was filed to protect this innovation.
4. It was demonstrated that anodic SiO_2 layers (formed using LIA) provided excellent surface passivation and leakage current densities as low as 3.5×10^{-10} and 1.6×10^{-9} A cm^{-2} measured at 1 and -1 V, respectively. This achievement may enable anodic SiO_2 to be used for MIS metal contact passivation, epitaxial thin silicon passivation and barriers for metal plating and PID.
5. It was shown that the formation of AAO layers using LIA addressed most of the identified limitations of the clip anodisation. Cells passivated on the rear surface with SiO_2/AAO layers were demonstrated with a V_{oc} of 660 mV being achieved using commercial grade Cz *p*-type wafers. This result suggests that low-cost AAO layers may be able to effectively replace the more expensive Al_2O_3/SiN_x dielectric layer which is currently deposited by PECVD in PERC cell manufacturing. A detailed loss analysis of the AAO-passivated cells showed the potential of this structure to achieve efficiencies achieving 20.7%.

7.2 Future Work

The investigations performed as part of this thesis also highlighted a number of areas of future research. The promising inkjet-patterning method, reported in Chapter 4, was limited by the properties of AAO layers formed by clip anodisation. The new LIA technique, reported in Chapters 5 and 6, was shown to practically address these limitations. However there was insufficient time to demonstrate this patterning method using AAO layers formed by LIA. Future work could investigate the use of this patterning method in the formation of inkjet-patterned PERC cells, with investigations into the effect of larger point spacing (i.e., greater than the 250 µm spacing demonstrated in Chapter 4) and the impact of point spacing on cell V_{oc} and efficiency.

As mentioned above there are a number of applications for thin SiO_2 layers which have low leakage currents. There is currently significant interest in passivated contact cell structures where doped polysilicon layers are formed over tunnel oxides [320, 376, 377]. The tunnel oxides in these cases need to be thin (< 3 nm) and very uniform across a wafer surface. These properties are difficult to achieve with both chemical and thermal oxides. The LIA technique has the potential to achieve the required uniformity. In addition, the low leakage currents of SiO_2 layers formed by LIA may enable them to be excellent barrier layers for metal plating and PID.

It would be advantageous to be able to manipulate the charge magnitude and polarity of AAO rear surface passivation layers. Negative or low positive stored charge is preferable for rear passivation layers of *p*-type PERC cells as it can result in a reduced injection-level dependent rear *SRV*. It has been shown [372] that the stored charge magnitude can be tuned with different anodisation conditions. However, further study is required to establish whether similar control of stored charge can be achieved using LIA of aluminium.

Finally, future studies could seek to address the low J_{sc} and *FF* of the fabricated AAO-passivated PERC cells. First, the use of a more lightly-doped emitter and less absorbing ARC is required to increase the J_{sc}. Second, the boron laser doping process could be replaced by laser scribing through the AAO (which has been shown to create local *p*+ regions in [207] or by inkjet patterning (as discussed above) to reduce the R_s which presumably resulted from the resistive boron glass layer. By eliminating edge

losses due to laser cleaving (e.g., by fabricating cells on 156 mm wafers), cell efficiencies of 20.6% should be achievable.

Appendix A. List of Publications

Journal Publications

Cui, J., Ouyang, Z., Hameiri, Z., Wang, X., Lennon, A. *Ultra-low interface state density achieved by light-induced anodisation of aluminium on silicon solar cell surfaces.* IEEE Journal of Photovotlaics, 2015. Accepted for publication.

Cui, J., Grant, N., and Lennon, A., *Effective surface passivation of p-type crystalline silicon with silicon oxides formed by light-induced anodisation.* Applied Surface Science, 2014. **323**(0): p. 40-44. Invited paper.

Cui, J., Wang, X., Opila, R., and Lennon, A. "*Light-induced anodisation of silicon for solar cell passivation.*" Journal of Applied Physics, 2013. 114(18): 184101.

Cui, J., To, A., Rodriguez, J., and Lennon, A. "*Inkjet patterned anodic aluminium oxide for rear metal contacts of silicon solar cells.*" 2013. Energy Procedia, 38, p.691-700.

Yao, Y., Rodriguez, J., Cui, J., Lennon, A., and Wenham, S. "*Uniform plating of thin nickel layers for silicon solar cells.*" 2013. Energy Procedia, 38, p.807-815.

Lu, Z., Lu, P.H., Cui, J., Wang, K., and Lennon, A., *Self-patterned localized metal contacts for silicon solar cells.* Journal of Materials Research, 2013. 28(15): p. 1984-1994. Invited paper.

Full Refereed Conference Proceedings

Cui, J. Wang, X., Opila, R., and Lennon, A. "*Characterization of silicon oxide formed by light-induced anodisation.*" 2013. 2013 MRS Fall Meeting, Boston, United States (oral presentation).

Cui, J., Colwell, J., Li, Z., and Lennon, A. "*Localised back surface field formation via different dielectric patterning approaches.*" 2012. SOLAR 2012 Conference, Melbourne, Australia (oral presentation).

Rodriguez, J., Wang, X., Subbiah, J., Cui, J., and Lennon, A. "*Polymer spraying for aerosol jet etching of dielectrics for 156-cm silicon wafers.*" 2013. 2013 MRS Fall Meeting, Boston, United States (oral presentation).

Conference Proceedings

Cui, J., Wang, X., Lin, D., Lu, P., and Lennon, A. "*Anodic aluminium oxide rear passivated laser-doped selective-emitter solar cells.*" 2014. 40th IEEE PVSC, Denver, United States (poster presentation)

Cui, J., Wang, X., and Lennon, A. "*Light-induced anodisation of aluminium for rear surface passivation.*" 2013. 28th EU PVSEC, Paris, France (poster presentation).

Cui, J., Wang, X., Lu, P.H., Lu, Z., Li, Y., Li, Z., Tong, J., and Lennon, A. "*Anodic oxide passivation using wet chemical through-wafer processes.*" 2013. 2013 Australian Center for Advanced Photovoltaics (ACAP) Research Conference, Sydney, Australia (poster presentation)

Ouyang, Z., Lau, D., Lu, P. H., Cui, J., Lennon, A. "*Formation of Metal-Metal Oxide Patterns using Masked Light-Induced Anodization*" 2015. Submitted to 42nd IEEE PVSC.

Ouyang, Z., Cui, J., Li, Y., Li, Z., and Lennon, A. "*Structural studies of light-induced anodic aluminium oxide.*" 2014. 40th IEEE PVSC, Denver, United States (poster presentation)

Lu, Z., Lu, P., Hameiri, Z., Wang, K., Cui, J., and Lennon, A. "*Stored charge properties of anodic aluminium oxide on silicon substrate.*" 2014. 40th IEEE PVSC, Denver, United States (poster presentation)

Li, Y., Li, Z., Lu, Z., Cui, J., Ouyang, Z., and Lennon, A. "*Optical modelling for multilayer and geometric light-trapping structures for crystalline silicon solar cells.*" 2014. 40th IEEE PVSC, Denver, United States (poster presentation)

Colwell, J., Cui, J., and Lennon, A. "*Method for evaluating the effectiveness of passivation layers on grains of different orientation in casted silicon wafers.*" 2013. 28th EU PVSEC, Paris, France (poster presentation).

Patent Applications

Cui, J. and Wang, X. 'A method of anodising a surface of a semiconductor device', 24 March 2014, Application No. PCT/AU2014/000307.

Yao, Y., Lennon, A., Cui, J., Luo, X., and Wenham, S. 'Formation of Metal Contacts', 9 November 2012, Application No. PCT/AU2013/001293.

Appendix B. List of Abbreviations

Abbreviation	Explanation
3D	Three Dimensional
AAO	Anodic Aluminium Oxide
AC	Alternating Current
AFM	Atomic Force Microscopy
AFR	Atomizer Flow Rate
AJE	Aerosol Jet Etching
APCVD	Atmospheric Pressure Chemical Vapour Deposition
ARC	Anti-Reflection Coating
a.u.	Arbitrary Unit
BSF	Back Surface Field
CIJ	Continuous Ink Jet
CV	Capacitance-Voltage
CVD	Chemical Vapour Deposition
CW	Continuous Wave
Cz	Czochralski
DC	Direct Current
DI	Deionised
DOD	Drop-On-Demand
ECV	Electrochemical Capacitance-Voltage
EQE	External Quantum Efficiency
EWT	Emitter Wrap Through
FF	Fill Factor
FIB	Focused Ion Beam
FIA	Field-Induced Anodisation
FTIR	Fourier Transform Infrared Spectroscopy
FZ	Float Zone
HF	Hydrofluoric Acid
IBC	Interdigitated Back Contact Cells
IQE	Internal Quantum Efficiency
Laser	Light Amplification by Stimulated Emission of Radiation
LBSF	Local Back Surface Field
LED	Light Emitting Diode
LFC	Laser Fired Contact
LIA	Light-Induced Anodisation
LIP	Light-Induced Plating
LPCVD	Low-Pressure Chemical Vapour Deposition
MIS	Metal Insulator Silicon

MIS/IL	Metal Insulator Silicon/Inversion Layer
MWT	Metal Wrap Through
PAA	Polyacrylic Acid
PC	Photoconductance
PECVD	Plasma Enhanced Chemical Vapour Deposition
PERC	Passivated-Emitter and Rear Contact
PERL	Passivated-Emitter and Rear Locally-Diffused
PID	Potential-Induced Degradation
PL	Photoluminescence
PSG	Phosphorus Silicon Glass
PV	Photovoltaics
QE	Quantum Efficiency
QSS	Quasi-Steady-State
QSS-PC	Quasi-Steady-State Photoconductance
QSS-PL	Quasi-Steady-State Photoluminescence
RT	Room Temperature
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectroscopy
SFR	Sheath Gas Flow Rate
SRV	Surface Recombination Velocity
STC	Standard Test Condition
Suntech	Suntech Power Inc.
TEM	Transmission Electron Microscopy
UMG	Upgraded Metallurgical Grade
UNSW	University of New South Wales
UV	Ultra-Violet

Appendix C. List of Symbols

Symbol	Description	Unit
A	Pre-exponential constant in Arrhenius equation	---
C	Capacitance	F
C_{ox}	Oxide capacitance	F
D_{it}	Interface state	$cm^{-2}\ eV^{-1}$
E_g	Band gap	eV
FF	Fill factor	%
I	Current	A
iV_{oc}	Implied open circuit voltage	mV
J_0	Dark saturation current density	$A\ cm^{-2}$
J_{0e}	Emitter saturation current density	$A\ cm^{-2}$
J_{mp}	Current density at maximum power point	$A\ cm^{-2}$
J_{sc}	Short circuit current density	$A\ cm^{-2}$
k	Boltzmann constant	$J\ K^{-1}$
k	Extinction coefficient	---
K	Reaction rate in Arrhenius equation	$mol\ L^{-1}\ s^{-1}$
m	Local ideality factor	---
M	Molar mass	$g\ mol^{-1}$
M	Molar concentration	$mol\ L^{-1}$
n_i	Intrinsic carrier concentration	cm^{-3}
n_r	Refractive index	---
pFF	Pseudo fill factor	%
P_{mp}	Power at maximum power point	W
q	Elementary charge of electron	C
Q_f	Density of fixed charge	$C\ cm^{-2}$
Q_{eff}	Density of effective charge	$C\ cm^{-2}$
Q_{total}	Total charge	C
R	Universal gas constant in Arrhenius equation	$V\ K^{-1}\ mol^{-1}$
R	Reflectance	%
R_c	Contact resistance	$\Omega\ cm^2$
$R_{cooling}$	Cooling rate	$K\ s^{-1}$
R_{CT}	Charge transfer resistance	$\Omega\ cm^2$
R_O	Anodic oxide resistance	$\Omega\ cm^2$
R_s	Series resistance	$\Omega\ cm^2$
R_{sp}	Spreading resistance	$\Omega\ cm^2$
R_{sh}	Shunt resistance	$\Omega\ cm^2$
R_Ω	Electrolyte resistance	$\Omega\ cm^2$
S_{eff}	Effective surface recombination velocity	$cm\ s^{-1}$

t	Time	s
t_{epi}	Time for silicon epitaxial growth	s
t_{ideal}	Ideal thickness of anodic oxide	nm
T	Absolute temperature	K
$T_{eutectic}$	Eutectic temperature of aluminium silicon binary system	°C
T_{peak_m}	Measured peak firing temperature	°C
T_{peak_s}	Set peak firing temperature	°C
V	Voltage	V
V_{bias}	Bias voltage	V
V_{cell}	Cell voltage	V
V_{mp}	Voltage at maximum power point	mV
V_{oc}	Open circuit voltage	mV
$V_{p\text{-}p}$	Peak to peak voltage	V
V_{rms}	Root mean square voltage	V
W	Wafer thickness	µm
Δn	Minority carrier concentration	cm^{-3}
η	Solar cell efficiency	%
ρ	Density	g cm^{-3}
ρ_c	Specific contact resistance	Ω cm^2
τ_{bulk}	Bulk lifetime	s
τ_{eff}	Effective minority carrier lifetime	s
$\tau_{emitter}$	Emitter lifetime	s
$\tau_{surface}$	Surface lifetime	s
φ	Interfacial potential	V
AlO_x	Aluminium oxide	
DEG	Diethylene glycol	
H_3PO_4	Phosphoric acid	
H_2SO_4	Sulphuric acid	
HF	Hydrofluoric acid	
NaOH	Sodium hydroxide	
NH_3	Ammonia	
NH_4F	Ammonium fluoride	
NH_4HF_2	Ammonium bifluoride	
NH_4OH	Ammonium hydroxide	
$POCl_3$	Phosphoryl chloride	
SiH_4	Silane	
SiH_2Cl_2	Dichlorosilane	
$Si(OH)_4$	Silicic acid	
SiO_2	Silicon dioxide	
SiN_x	Silicon nitride	
TiO_2	Titanium dioxide	

Appendix D. System of Units

Quantity	Unit	Symbol
Conductance	Siemens	S
Current[1]	Ampere	A
Electric charge	Coulomb	C
	Elementary charge	q
Energy	Joule	J
	Electron-volt	eV
Flow rate	Standard cubic centimetres per minute	sccm
Frequency	Hertz	Hz
	Revolutions per minute	rpm
Length[2]	Meter	m
Mass	Gram	g
Power[3]	Watt	W
Pressure	Bar (milli)	mbar
	Pascal	Pa
	Torr (milli)	mTorr
Resistivity	Ohm	Ω
Temperature	Kelvin	K
	Degree Celsius	°C
Time[4]	Second	s
Voltage[5]	Volt	V
Volume	Litre	L

[1]Milliampere (10^{-3} A) is often used in this thesis for current.

[2] In semiconductors it is more common to use centimetre (10^{-2} m), micrometer (10^{-6} m) and nanometre (10^{-9} m) for length.

[3] Milliwatt (10^{-3} W) is often used in this thesis for power.

[4] Microsecond (10^{-6} s) is often used in this thesis for time.

[5] Millivolt (10^{-3} V) is often used in this thesis for voltage.

Appendix E. Surface Passivation on Grains of Different Orientation in Lower Quality Silicon Wafers

The aim of this thesis was to examine low-cost rear contact schemes that were applicable to commercial grade or lower-quality silicon wafers. Therefore the effectiveness of passivation on these wafers especially cast-mono and high performance (HP) multi wafers was studied as part of this work. This study found that a high density of twin (Σ3) boundaries corresponded to the areas of improved lifetime, whereas randomly-oriented boundaries acted as high recombination regions and limited τ_{eff}.

Introduction

The photovoltaic industry is currently dominated by crystalline silicon based technologies, which have approximately 90% of the market share in 2013. Within silicon-based PV, the market is largely split between single crystal Cz silicon (mono-Si) and the lower-cost, multi-crystalline silicon (mc-Si) [8, 378]. The main difference between these is a result of the casting process, with the higher quality Cz silicon being the product of an energy-intensive, costly crystallisation technique to produce a highly pure single crystal ingot, whilst the lower cost, lower quality mc-Si is a result of directional solidification of molten silicon in a crucible, known as block casting. The solidification process for mc-Si introduces a number of defects and impurities into the silicon block, such as dislocations and grain boundaries. These defects and impurities act as recombination centres, thus reducing the overall τ_{eff} of the wafer [379].

One way of solving this issue is to combine these two crystallisation processes, resulting in cast-mono silicon. Cast-mono silicon combines the cost-effectiveness of the block casting method used in mc-Si ingot production, with the benefit of producing a large area of mono-crystalline material of (100) orientation with the aid of a seed crystal [380]. However, the edge and corner regions of this ingot are still largely mc-Si in nature and experience the same defect issues as standard mc-Si wafers, and are thus not ideal for higher efficiency cell production. Next-phase mc-Si materials, such as high performance (HP) multi-Si, attempt to overcome these issues by introducing multiple

seed casting in order to produce higher quality mc-Si for higher efficiency cells, however grain boundaries still exist.

Passivation offers a solution to this problem, and is an important step in improving the effective lifetime of low quality silicon wafers by eliminating dangling bonds at the surface to reduce surface recombination, whilst introducing hydrogen into the bulk material to passivate the deeper grain boundaries and defects [341, 381].

A number of studies have been conducted to investigate the defects present in mc-Si wafers and to determine how such defects can best be passivated such that they are not detrimental to the performance of completed devices. Sopori *et al.* performed a study on the dislocations and properties of cast-mono and mc-Si, showing that effective passivation of defects can result in efficiencies of 18 - 20% with such materials [382]. Tsuchiya *et al.* studied the impact of certain impurities on different grain boundaries, showing that particular grain boundaries ($\Sigma 3$, for example) were able to getter impurities better and that randomly-oriented boundaries decorated with impurities (iron in particular) severely deteriorate cell performance [383]. Guthrey *et al.* investigated the use of PL and electron backscatter diffraction (EBSD), to study performance limitations in mc-Si. They were able to identify grain boundaries of various misorientation angles present in regions exhibiting high recombination rate [384].

Few reports exist on the effect of crystal orientation on passivation effectiveness. Some studies have examined crystal dependence of electrical properties in (100), (111) and (110) mono-crystalline wafers [385, 386]. However, little of this knowledge has been applied to cast-mono and mc-Si wafers. A recent study by Sio *et al.* investigated the influence of crystal orientation on surface passivation in mc-Si. In this study, a contrast in lifetime among different grains was observed in PL images taken of mc-Si wafers passivated with aluminium oxide [387]. However, the effectiveness of various passivation materials on different grain orientations has not been detailed extensively in a quantitative form.

The purpose of this study was to investigate the effective lifetime improvements of cast-mono and HP multi-Si wafers using different passivation layers applied using PECVD. Using a combination of PL imaging, lifetime testing and grain identification via EBSD, the lifetime variation between grains and the possible correlations between grain orientation, distribution and passivation effectiveness were evaluated.

Experimental

This study was performed using cast mono and HP multi silicon wafers. The cast-mono wafers used in this study were 156 mm × 156 mm acidic-textured wafers selected from the edge region of the ingot, such that each wafer consisted of both mc-Si and mono-Si regions. The HP multi wafers selected were 156 mm × 156 mm as-cut wafers selected from various positions along the edge of the ingot and the centre of the block for comparison. The initial thickness of each wafer type was 180 μm and 190 μm, respectively, with a bulk resistivity of 1 - 3 Ω cm for both types of wafer. Neighbouring wafers were chosen such that the crystal orientation and distribution were identical between wafers for the purposes of experimental comparison.

Acidic-textured wafers were used to eliminate optical effects during PL imaging for the cast-mono experiments. However, since the HP multi wafers had a significant layer of surface damage, this had to be removed before passivation. Furthermore, in order for the grain distribution to be analysed all the wafer surfaces (including the acidic-textured surfaces of the cast-mono wafers) needed to be polished. To achieve this, an acidic HNA solution was used. The volume ratio of HNO_3:CH_3COOH:HF was 75:17:8 assuming stock solutions of concentrations 70% (w/w) HNO3, 49% (w/w) HF and 100% (glacial) CH_3COOH. The isotropic etching step was performed for 4 min to produce a semi-polished, planar surface for passivation experiments on the HP multi wafers. The etching was extended to 5 min to produce the more mirror-polished surface necessary for the grain identification via EBSD. Each wafer was then rinsed in DI water followed by a 10% HF dip to remove any native oxide that formed during the process. This 4 min etching step reduced the wafer thickness to approximately 140 - 150 μm.

One wafer from each block was left as a control for comparison. Every wafer processed was laser cleaved into 16 samples for each experiment. Each batch undergoing passivation was RCA cleaned and underwent a 1 min 5% HF dip before the application of a 75 nm SiN_x or SiON layer via a remote PECVD (Roth & Rou AK400) on both sides of each wafer. Afterwards, a post-deposition annealing step was performed at 400 °C for 15 min in ambient nitrogen.

Effective minority carrier lifetime was measured using a WCT-100 Lifetime Tester (Sinton Instrument) and PL images were taken using a BT Imaging tool. These measurements were performed before and after dielectric layer deposition and after annealing in order to study the passivation effectiveness at different stages of processing.

PL images were also analysed using Matlab to produce delta-PL maps that highlighted each wafer's response to the passivation process. From this data, areas of interest were scanned and mapped using EBSD with a Zeiss AURIGA FIB-SEM system.

Results and Discussions

Figure 1 shows a PL image taken of one cast-mono wafer before the application of the passivation layer with an arbitrary PL count scale provided. The dark lines on the image correspond to grain boundaries or dislocations in the silicon wafer and represent areas of high carrier recombination and thus lower lifetime.

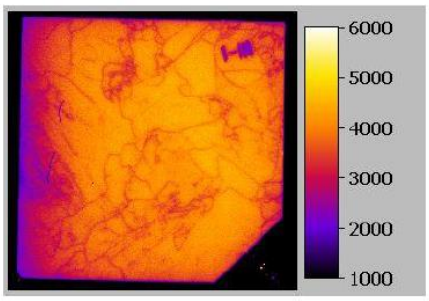

Figure 1 PL image of a cast-mono silicon wafer before the application of a passivation layer.

After the application of a dielectric layer comprising either SiN_x or SiON and subsequent annealing, the PL image shows a significant increase in lifetime. However, there is a clear variation in the lifetime improvement across the wafer surface. This is in agreement with previous studies conducted [387, 388]. An aim of this work was to compare the lifetime improvements of cast-mono silicon with the application of different passivation layers. A set of PL images from neighbouring wafers with identical grain distributions after the application of SiN_x or SiON via PECVD is shown in Figure 2 below.

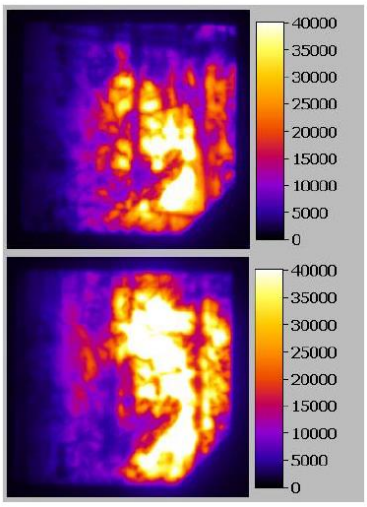

Figure 2 PL images of cast-mono silicon wafers passivated by 75 nm SiN_x (top) and 75 nm SiON (bottom).

Figure 2 shows that there is not only a variation in passivation quality across a wafer, but that the average magnitude of the lifetime improvement varies for different passivation layers. The SiON layer appears to passivate the same regions of the wafer more effectively than a standard SiN_x layer. This was a noticeable trend that occurred with other neighbouring wafers. Since both wafers underwent the same processing before passivation, it is clear that some regions were less effectively passivated by the SiN_x layer. This trend is also reflected in the lifetime measured for each wafer after passivation. The average effective minority carrier lifetime of the cast-mono wafers after annealing was 50 μs for those wafers passivated by SiON, whilst the

SiN_x samples only achieved an average effective lifetime of approximately 40 μs. This difference could be due to the passivation mechanism of SiON, or due to differing deposition conditions for the two passivation layers.

For both passivation layers, annealing at 400 °C for 15 min improved the effective lifetime of all the cast-mono wafers, with the average effective lifetime increasing from 33 to 50 μs after annealing. However, as seen in Figure 3, the improvement is still localised to regions that already had higher effective lifetimes before annealing, with lower lifetime regions showing little improvement on annealing.

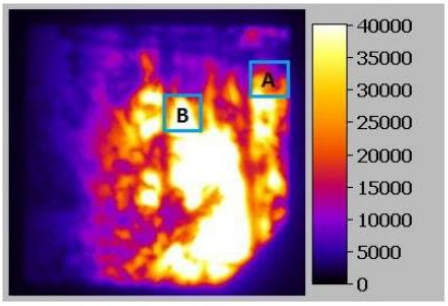

Figure 3 PL image of a cast-mono silicon wafer passivated by 75 nm SiN_x followed by annealing at 400 °C. The regions A and B refer to areas of interest scanned by EBSD to identify grain/grain boundary distribution.

Extending this to the HP-multi silicon wafers, a similar variability in passivation quality was observed in the open-circuit PL images. One key difference between these two types of wafer was the effective lifetime. The effective lifetimes measured for the HP multi wafers were significantly greater than those of the cast-mono wafers. The highest lifetime achieved for the HP multi wafers was ~ 360 μs, and this was achieved using a 75 nm double-sided SiON layer. To confirm the accuracy of this data, a transient photoconductance measurement was performed to eliminate any effects from the bulk doping of the wafer. The result of this transient measurement was in close agreement with the original QSS measurement. As is clear from the open-circuit PL image in Figure 4 below, there is a clear increase in bright PL regions for the HP multi wafers, and yet a variable lifetime between grains is still observable.

The significantly higher effective lifetimes measured for the HP multi wafers compared to the cast-mono wafers may be due to higher silicon purity utilised in the casting process and/or lower dislocation densities. Multiple seed casting produces many small grains, which tend to be less decorated with impurities and dislocations than the larger grains and mono-Si regions found in cast-mono materials [382]. Effective lifetime results obtained in this study for both cast-mono and HP multi silicon are summarised in Table 1.

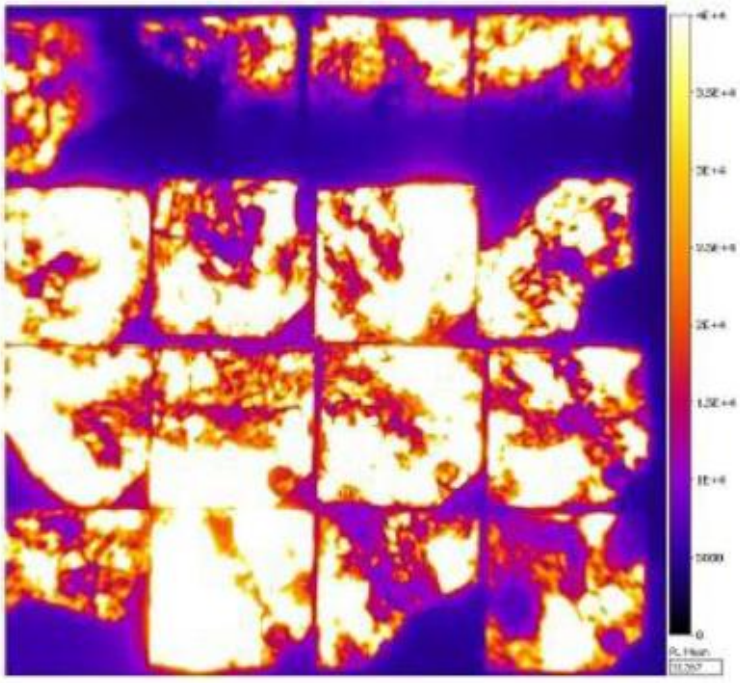

Figure 4 PL image taken of HP multi wafers after passivation with SiN_x (top eight wafers) and SiON (bottom eight wafers).

Table 1 Summary of effective lifetime results for cast-mono and HP multi wafers after passivation and annealing.

Wafer type	Sample	iV_{oc} (mV)	τ_{eff} (µs)	Passivation material
Cast-mono wafers	Best	642	71	SiON
	Worst	601	15	SiN_x
	Mean	628	46	---
HP multi wafers	Best	701	362	SiON
	Worst	617	25	SiN_x
	Mean	657	116	---

Photoluminescence images obtained for each wafer pre and post-passivation were utilised by Matlab to produce a delta-PL count map (see Figure 5). Each image was loaded into Matlab to produce a matrix, where each matrix element corresponds to a coordinate of the wafer surface and the value given reference to the PL count. Rotation and cropping tools provided in Matlab were utilised to match each wafer as accurately as possible.

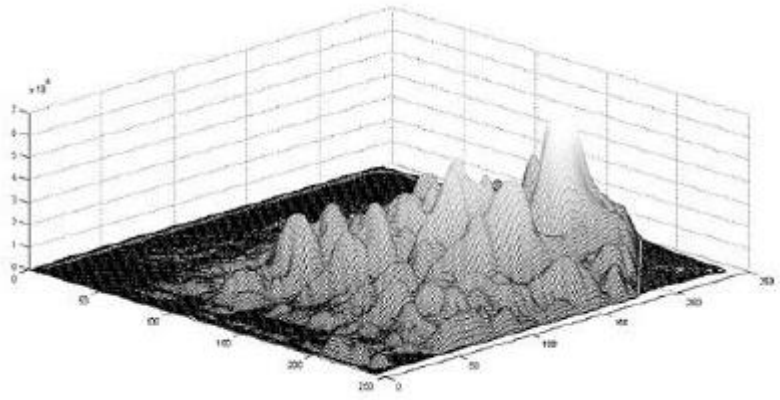

Figure 5 Terrain-style map showing delta PL count for a cast-mono sample. (0,0) on the plot indicates the top left corner, opposite the laser cut corner.

As is clear from the Matlab-produced graph, compared to the open-circuit PL image as seen in Figure 2, the regions with the highest delta-PL counts match those observed in the PL images. Thus, the delta-PL maps provided a useful means for studying variations in lifetime with surface passivation for the casted silicon wafers studied. With the use of Matlab, peaks and troughs were able to be identified in the matrix, and their exact location determined for use in selecting regions to be scanned by EBSD to study the grains and grain distribution in some of these areas of interest. Also, with the PL image loaded in as a matrix, several matrix operations could be performed to determine a number of relationships, such as the effective lifetime vs. percentage coverage of PL counts above a certain threshold.

The second objective of this work was to study the influence of crystal orientation on passivation effectiveness for cast-mono and HP multi wafers. Using EBSD scans, grain maps of selected regions were produced. Figure 6 presents grain maps taken from two different regions in a cast-mono sample.

Each scan covered an area of approximately 5 mm × 5 mm and used a step size of 100 μm for clearly resolved maps of grains and grain boundaries. To better understand the meaning of the results presented here, we have identified the areas scanned on the PL image in Figure 3 earlier in this paper.

In each image in Figure 6, the red outlines represent twin boundaries, classified as (111) 60° boundaries, also known as Sigma 3 boundaries (Σ3). The other boundaries,

which we refer to as randomly-oriented boundaries, were classified by their misorientation angle. The thick black lines represent boundaries with angles ≥ 10°. Thinner lines were observed in some wafers and they represent boundaries classified as small angle boundaries of < 10°. An analysis of these scans showed all boundaries were of angles < 60°. The boundaries present in each of these EBSD scans were identified and are summarised in Table 2.

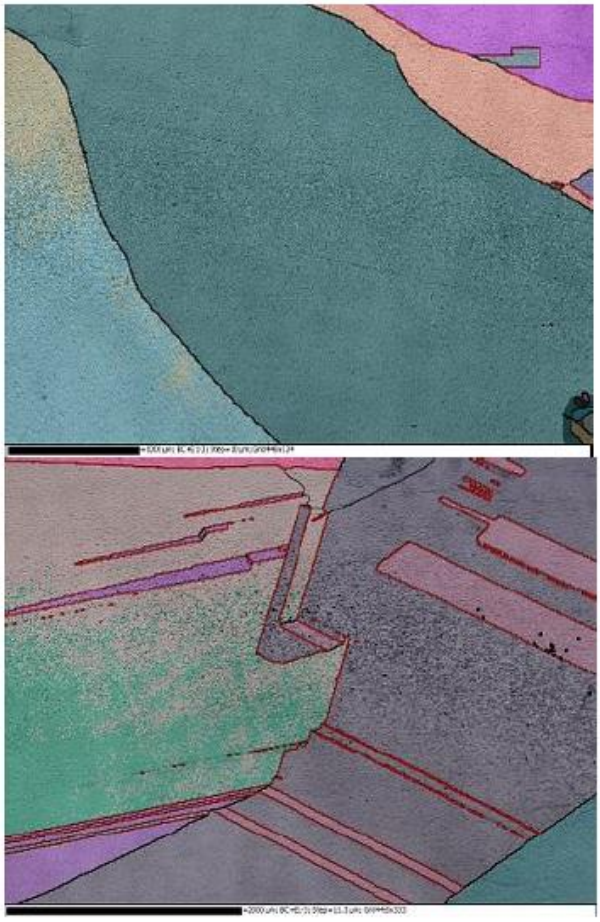

Figure 6 EBSD Maps for locations A (top) and B (bottom) as given in Figure 3.

Table 2 Ratio of Σ3 boundaries to randomly-oriented boundaries in cast-mono wafer locations.

Location	No. of Σ3 boundaries	No. of Randomly-oriented boundaries
A	2	4
B	> 10	4

If we compare the EBSD maps to the PL images presented earlier, it is seen that the EBSD map of location B corresponds to the region of higher lifetime. Also, location B shows a significantly greater number of Σ3 boundaries than that of location A. This result seems to suggest that regions dominated by these Σ3 boundaries are passivated more effectively than those with randomly-oriented grain boundaries. This trend was also observed in the scans taken of regions in the HP multi wafers.

The analysis software used in this study interprets the data from each scan to define grains based on three separate values known as Euler angles (φ1, Φ and φ2), which represent a set of rotations about the *z-axis*, rotated *x-axis* and rotated *z-axis* respectively in order to bring one orientation into coincidence with another [389]. The grain details for four separate areas of interest and their qualitative lifetime improvement as determined from the open-circuit PL image taken is presented in Table 3.

Table 3 Euler angles denoting crystal grain orientation for different positions in cast mono (1-2) and HP multi (3-4) wafers.

Wafer	Position	Lifetime	φ1	Φ	φ2
Cast-mono	1	Low	2.4	27.4	29.9
wafers	2	High	91.5	19.5	28.3
HP multi	3	Low	283.7	51.1	46.4
wafers	4	High	131	30.7	326

The results above are representative of some of the various grains measured via EBSD for particular regions of both cast-mono and HP multi silicon passivated by different dielectric layers. From the data collected and analysed, any obvious correlation between grain orientation and passivation quality was difficult to determine. Despite the clear variation in the effective lifetime of wafers between grains, no quantitative dependence on grain orientation was evident when relating the EBSD maps to the associated regions in the PL images.

Conclusions

In this study, cast-mono and HP multi silicon wafers were passivated with SiN_x and SiON dielectric layers to study the lifetime improvements of these materials when passivated. Although the average effective lifetime improves after deposition of both

SiN_x and SiON layers, annealing did little to improve the effective lifetime of regions which had a low effective lifetime after deposition of the dielectric layer. One key result from this study is that SiON layers can more effectively passivate both wafer types when compared to SiN_x layers. The average effective lifetime of HP multi wafers increased significantly after annealing, with a lifetime of ~ 360 μs resulting after deposition and annealing of a SiON layer. Photoluminescence imaging and EBSD measurements were used to investigate the relationship between grain orientation and passivation quality. It was found that twin boundaries tended to propagate in the higher lifetime regions of wafers, whereas randomly-oriented boundaries acted as high recombination regions and limited effective carrier lifetime. However, no clear relationship between grain orientation and effective lifetime was evident.

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