Improved Hybrid Techniques for Grid Fault Detection and Fault Ride-Through of Power Converters

Animesh Sahoo

A dissertation submitted in fulfillment
of the requirements for the degree of

Doctor of Philosophy

School of Electrical Engineering and Telecommunications
The University of New South Wales

January 2021

Thesis/Dissertation Sheet

Surname/Family Name	:	**SAHOO**
Given Name/s	:	**ANIMESH**
Abbreviation for degree as give in the University calendar	:	**PhD**
Faculty	:	**Engineering**
School	:	**Electrical Engineering and Telecommunications**
Thesis Title	:	**Improved hybrid techniques for grid fault detection and fault ride-through of power converters.**

Abstract 350 words maximum: (PLEASE TYPE)

Accurate and fast grid voltage parameter estimation is essential for grid-connected converters. To achieve this objective, the contributions of this thesis are classified into two parts.

The first part of the thesis deals with the fault detection for converters during a grid fault using digital signal processing (DSP) techniques. A hybrid fault detection technique is proposed to detect grid faults. The technique combines the features of two DSP techniques, namely, Hilbert-Huang Transform (HHT) and Teager Energy Operator (TEO). Hence it is called Teager-Huang in this thesis. With this proposed technique, several grid faults, balanced and unbalanced, in both the grid voltage magnitude and phase-angle jumps are detected. Further, comparisons of the fault energies are presented, which provide a benchmark for the severity of the grid faults.

In the second part of the thesis, the synchronization aspect of the converter is investigated. The synchronization using the classical synchronous frame phase-locked loop (SRFPLL) is taken for consideration and emphasises is provided on the occurrence of the phase-angle jump (PAJ) during a fault. The thesis indicates that the conventional SRFPLL design parameters result in synchronization delays and insufficient damping to ride-through such PAJs. To enhance the grid synchronization performance during a grid fault with PAJ, a hybrid grid synchronization concept is proposed. The proposed technique is designed to be compatible with both the three-phase and single-phase grid synchronization. To avoid voltage transients during the transition between the estimators, a transition scheme is presented. This is controlled based on the instantaneous phase-angle error measured by the estimators.

Both three-phase and single-phase grid-connected converters are modelled using the proposed hybrid grid synchronization technique. The current controller of the converter is designed both in the stationary and synchronous reference frame. Further, the fault ride-through (FRT) strategy is embedded in the converter controller. With the developed model, the FRT of the converter is tested during a fault. Both symmetrical and asymmetrical grid faults with PAJs are considered. The efficacy of the proposed technique is evaluated using both simulation and experimental validations.

ORIGINALITY STATEMENT

'I hereby declare that this submission is my own work and to the best of my knowledge it contains no materials previously published or written by another person, or substantial proportions of material which have been accepted for the award of any other degree or diploma at UNSW or any other educational institution, except where due acknowledgement is made in the thesis. Any contribution made to the research by others, with whom I have worked at UNSW or elsewhere, is explicitly acknowledged in the thesis. I also declare that the intellectual content of this thesis is the product of my own work, except to the extent that assistance from others in the project's design and conception or in style, presentation and linguistic expression is acknowledged.'

Signed ……..

Date ……..

INCLUSION OF PUBLICATIONS STATEMENT

UNSW is supportive of candidates publishing their research results during their candidature as detailed in the UNSW Thesis Examination Procedure.

Publications can be used in their thesis in lieu of a Chapter if:

- The candidate contributed greater than 50% of the content in the publication and is the "primary author", ie. the candidate was responsible primarily for the planning, execution and preparation of the work for publication
- The candidate has approval to include the publication in their thesis in lieu of a Chapter from their supervisor and Postgraduate Coordinator.
- The publication is not subject to any obligations or contractual agreements with a third party that would constrain its inclusion in the thesis

Please indicate whether this thesis contains published material or not:

☐ This thesis contains no publications, either published or submitted for publication

☒ Some of the work described in this thesis has been published and it has been documented in the relevant Chapters with acknowledgement

☐ This thesis has publications (either published or submitted for publication) incorporated into it in lieu of a chapter and the details are presented below

CANDIDATE'S DECLARATION

I declare that:

- I have complied with the UNSW Thesis Examination Procedure
- where I have used a publication in lieu of a Chapter, the listed publication(s) below meet(s) the requirements to be included in the thesis.

Candidate's Name	Signature	Date (dd/mm/yy)

Abstract

In recent years, electric power generation using renewable energy sources has experienced an exponential growth in the world energy market. Their unprecedented large scale penetration foresees a 100% renewable based power generation in near future. These sources require power electronic converters at various levels for power conversion and grid integration. The converters are fast acting devices and use advance control techniques in a hierarchical manner. With the retirement of the conventional synchronous generators, the modern power electronics based power system lacks the inertia property. Hence, they are more vulnerable to several grid transient events; for instance grid faults. Control functionalities classify these converters as grid-forming and grid-following. Both these types can act as grid supporting devices during grid fault. In contrast to grid-forming type, grid-following type converters are mostly used to support the grid. The act of supporting the grid with reactive power instead of tripping during a fault for a pre-defined duration is known as fault ride-through. These converters rely on a separate synchronization unit to inject grid current during both normal and fault condition. Recent grid fault events across the globe have revealed the inefficiency of such synchronization units. This is attributed to the delayed grid parameter estimation that eventually leads to the tripping of the converters rather ride-through. It indicates that the performance robustness of the synchronizing unit while considering the fault ride-through of converter needs to be further investigated thoroughly.

In lieu of the above, accurate and fast grid voltage parameter estimation is essential for grid-connected converters. To achieve this objective, the contributions of this thesis are classified into two parts.

The first part of the thesis deals with the fault detection for converters during a grid fault using digital signal processing (DSP) techniques. Faster fault detection is vital to safeguard the power converter as they have limited fault current carrying capacity. Hence a hybrid fault detection technique is proposed. The technique combines the features of two DSP techniques, Hilbert-Huang Transform (HHT) and Teager Energy Operator (TEO). This is called Teager-Huang in this thesis. With this proposed technique, several grid faults, balanced and unbalanced, in both the grid voltage magnitude and phase-angle jumps are detected. Further, comparisons of the fault energies are presented, which provides a benchmark for the severity of the grid faults.

In the second part of the thesis, the synchronization aspect of the converter is investigated. For the purpose of analysis, the synchronization using the classical synchronous reference frame phase-locked loop (SRFPLL) is considered. Initially, the synchronization inefficiency of SRFPLL during the grid fault is explained in regards to the loss of synchronization (LOS) instability. It is shown that the cause for LOS during a fault may be initiated as results of very low grid voltage magnitude, high grid impedance or high current injection. The analysis emphasises on the occurrence of phase-angle jump (PAJ) during a fault. The thesis indicates that the conventional SRFPLL design parameters result in synchronization delay and insufficient damping to ride-through such PAJs.

The decrease in the SRFPLL synchronization robustness highly affects the grid-connected converters. To enhance the grid synchronization performance during a grid fault with PAJ, a hybrid grid synchronization concept is proposed. It consists of both hybrid phase-angle estimators and hybrid frequency estimators. The hybrid frequency estimators contain several improved adaptive and PLL independent frequency estimation techniques. The proposed technique is designed to be compatible with both the three-phase and single-phase grid synchronization. To avoid voltage transients during the transition between the estimators, a transition scheme is presented. This is controlled based on the instantaneous phase-angle error measured by the estimators.

The three-phase grid-connected converter is modelled using the proposed hybrid grid synchronization technique. The current controller of the converter is designed both in stationary and synchronous reference frame. Further, the fault ride-through (FRT) strategy is embedded in the converter controller. With the developed model, the FRT of the converter is tested during a fault. Both symmetrical and asymmetrical grid faults with PAJs are considered. The efficacy of the proposed technique is evaluated using both simulation and experimental validations.

The last part of the thesis explores the FRT of single-phase power converters employing the proposed hybrid grid synchronization transition. The synchronization performance along with the current controller robustness during FRT is investigated.

Acknowledgement

The research work in this PhD thesis is carried out under the supervision of Assoc. Prof. Jayashri Ravishankar (as my main supervisor) from the University of New South Wales (UNSW) and Dr. Mihai Ciobotaru (as my co-supervisor) from the Macquarie University (MQU).

First of all, I would like to express my sincere gratitude to Prof. Jayashri for believing and allowing me to pursue my research carrier in the school of electrical engineering and telecommunication at UNSW as an international PhD student. I got a chance to learn several qualities from you during my PhD journey such as research motivation, dedication to work, time management and above all, the quality of a good human being. You will always be an inspiration in my life. Secondly, I would like to thank Dr. Mihai for all the useful discussions regarding technical challenges during my thesis work. I really appreciate your vision towards the practical aspects of any research problem. It was amazing spending qualitative time with you during my PhD journey. This thesis would not have been possible without both of your support and motivation.

I would also like to thank Prof. John Fletcher from UNSW, for providing me an opportunity to work on the TYREE Microgrid project as part of my PhD research.

I would like to thank further all my colleagues in the energy system research group at UNSW for your lovely friendship and timely motivations during my PhD. Khizir, Anusuya, Miao, Hua, Shibo, and Swapneel. You guys are really awesome.

I would like to provide my deepest gratitude to my parents. I am unable to express the love and affection you have bestowed on me. Most importantly, I will never forget the tremendous patience you have shown during these days and allowed me to achieve my goal.

Lastly, but not the least, I would like to send a note of thanks to my lovely wife Mrs. Shuchismita Sahu for giving me unconditional love, showing unbelievable patience, and providing me strong motivation to keep going to achieve the carrier goal even during our hard times.

Dedicated to my parents and my wife

for their unconditional love and continuous motivations

Contents

List of Figures

List of Tables

List of Acronyms

AC	Alternating Current
ADC	Analog to Digital Converter
BPF	Band Pass Filter
DC	Direct Current
DFT	Discrete Fourier Transform
DLG	Double Line to Ground
DSC	Delayed Signal Cancellation
DSO	Distribution System Operator
DSOGI	Dual Second-Order Generalized Integrator
DSP	Digital Signal Processing
FRT	Fault Ride-Through
FFT	Fast Fourier Transform
HHT	Hilbert-Huang Transform
IIR	Infinite Impulse Response
IRDFT	Inverse Recursive Discrete Fourier Transform
LCL	Inductor-Capacitor-Inductor
LL	Line to Line
LPF	Low Pass Filter
LVRT	Low Voltage Ride-Through
MAF	Moving Average Filter
PCC	Point of Common Coupling
PI	Proportional Integral
PIR	Proportional Integral Resonant
PLL	Phase-Locked Loop
PR	Proportional Resonant
PWM	Pulse Width Modulation
QSG	Quadrature Signal Generator
RDFT	Recursive Discrete Fourier Transform
SCR	Short Circuit Ratio
SLG	Single Line to Ground

SOGI	Second-Order Generalized Integrator
SRFPLL	Synchronous Reference Frame Phase-Locked Loop
TEO	Teager Energy Operator
TFLL	Transition Frequency-Locked Loop
THD	Total Harmonic Distortion
TPLL	Transition Phase-Locked Loop
TSO	Transmission System Operator
VSC	Voltage Source Converter

List of Symbols

V_{DC}	DC-Link Voltage
V_{PCC}	Grid Voltage Measured at the Point of Common Coupling
$V_{sag} = V_F$	Fault Voltage Magnitude Measured at the Grid Side Bus
I_g	Grid Current Measured at the Point of Common Coupling
$V_{\alpha\beta}$	$\alpha\beta$-components of V_{PCC}
V_{dq}	dq-components of V_{PCC}
u_{dq}	Reference Voltages for dq-components of V_{PCC}
I_{dqr}	Reference Currents for dq-components of I_g
I_{dq}	dq-components of I_g
P, Q	Active and Reactive Power
Z_f	Converter Side Filter Impedance
R_f	Converter Side Filter Resistance
L_f	Converter Side Filter Inductance
Z_{fg}	Grid Side Filter Impedance
R_{fg}	Grid Side Filter Resistance
L_{fg}	Grid Side Filter Inductance
C_f	Filter Capacitance
R_d	Passive Damping Resistance
V_g	Thevenin Equivalent of Grid Voltage
Z_g	Thevenin Equivalent of Grid Impedance
Z_l	Line Impedance between Point of Common Coupling and Fault
K_{pv}, K_{iv}	Proportional and Integral Gains of the DC Voltage Controller
K_{pi}, K_{ii}	Proportional and Integral Gains of the Current Controller
K_{pi}, K_{ir}	Proportional and Resonant Gains of the Current Controller
K_{PPLL}, K_{IPLL}	Proportional and Integral Gains of Phase-Locked Loop
ζ	Damping Factor
t_{set}	Settling Time of Phase-Locked Loop
θ_{PLL}	Phase-angle Estimated by Phase-Locked Loop
ω_{PLL}	Frequency Estimated by Phase-Locked Loop
θ_{Arctan}	Phase-angle Estimated by Arctangent

θ_{TPLL}	Phase-angle Estimated by Transition Phase-Locked Loop
t_{tr}	Transition Time
$\omega_{\alpha\beta}$	Frequency Estimated by Arctangent Derived
ω_{TFLL}	Frequency Estimated by Transition Frequency-Locked Loop
ω_{teo}	Frequency Estimated by Teager Energy Operator
ω_{FD}	Frequency Estimated by Fixed Delay Method
$f_{sam}=f_s$	Sampling Frequency
T_s	Sampling Time
f_{sw}	Switching Frequency
θ_I	Current Injection Angle

Chapter 1

Introduction

1.1 Background

1.1.1 Power Generation using Renewable Energy Sources

The need for environmentally friendly (free from greenhouse gas emission), cost effective, safe and clean energy has attracted the attention to deploy several renewable energy resources (RESs) [1], [2]. They include hydro, marine, geothermal, bio, solar, wind energy, etc. Large-scale penetrations of these renewables have accelerated the replacement of the conventional synchronous generator based power generation to achieve the new energy paradigm of 100% renewable grid [3]. Out of the above-mentioned RESs, solar and wind energy systems have experienced an exponential growth in the world energy market in recent years [4]. Based on the recent study, in the last decade the RESs have added 75% of the total energy generation in which the amount of energy added in 2019 is more than 200 gigawatts as shown in Figure 1.1 [5]. Out of this total power, the contribution by solar is around 118 gigawatts, by wind is 60 gigawatts, and 22 gigawatts by the rest of RESs.

Energy generation using solar is a Worldwide proven technology. In this case, the sun's energy is exploited to generate electricity using either solar photovoltaic (PV) or concentrating solar power systems [6]. The solar energy system can operate for both off-grid and on-grid (grid-connected) applications. Off-grid operation of solar energy is an efficient replacement of diesel generators in rural areas [7]. In contrast, on-grid solar energy application is more cost effective

as it does not depend highly on extra energy storage system. On the other hand, wind energy is considered as one of the most emerging and sustainable RES in the era of 20th century [8], [9]. In this technology, the wind energy is converted to useful form of electricity using wind turbines. Despite the advantages obtained by the use of RESs in place of conventional energy sources, integration of these RESs to the existing grid poses several techno-economic challenges to the classical power system [10].

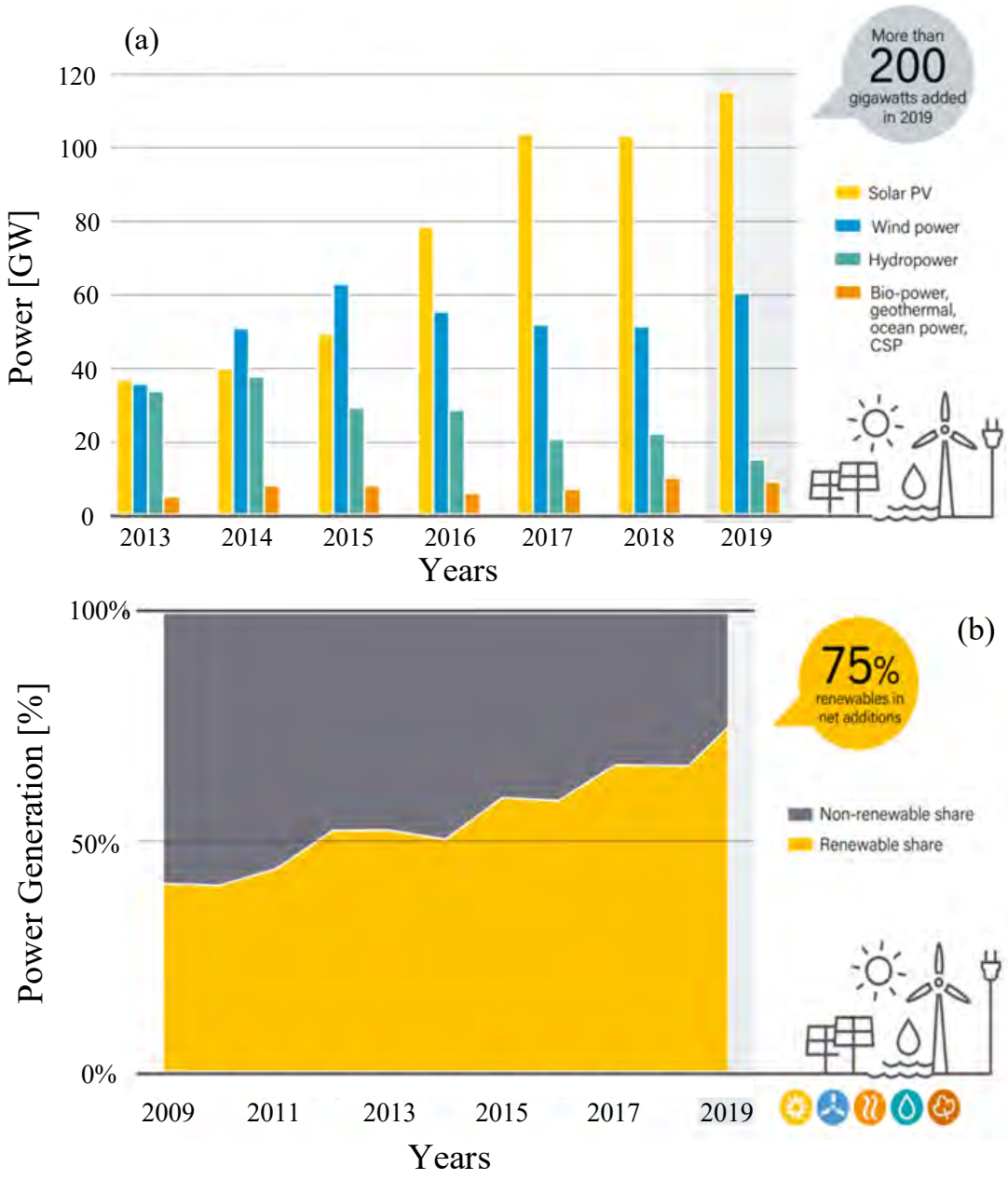


Figure 1.1 Power generation statistics using renewable energy resources (RESs) till 2019: (a) Amount of power generation in GWs and (b) Percentage contribution by the RESs [5].

1.1.2 Power Electronics Converters and Control

Power converters are the key power electronic components used for the grid integration of RESs especially solar and wind energy systems. The control architectures for these converters are hierarchical which consists of inner control, primary control, secondary control, and tertiary control [11]-[13]. On the basis of control functionalities at different control layers, these converters are called 'Grid-following (or Grid-feeding)' and 'Grid-forming' [14], [15] as shown in Figure 1.2.

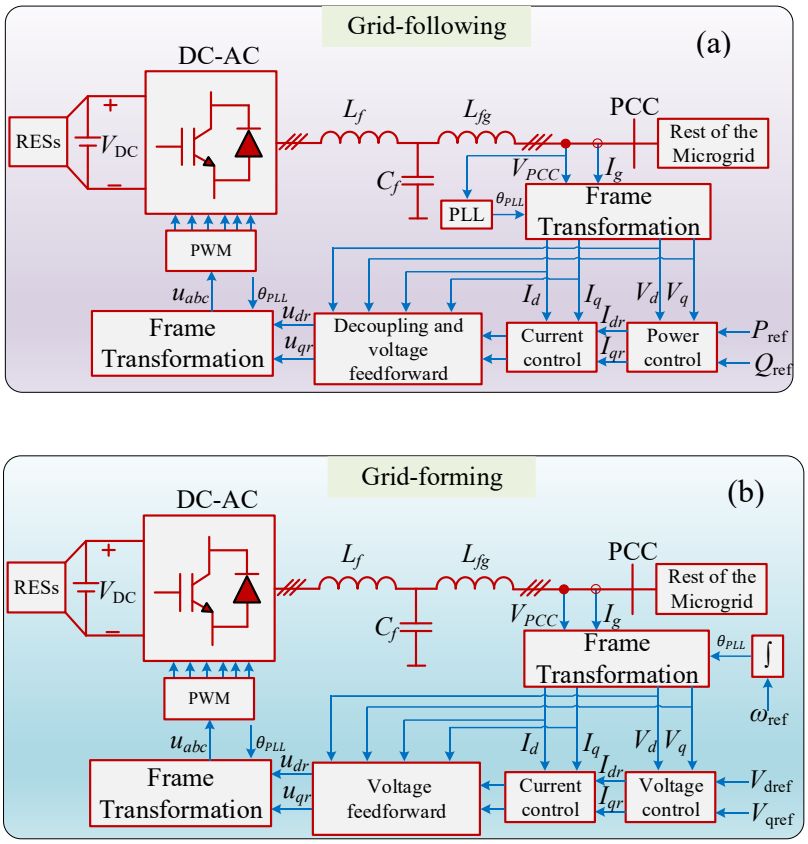


Figure 1.2 Basic converter control structure: (a) Grid-following mode and (b) Grid-forming mode [15].

The 'Grid-following' types of power converters require a dedicated grid synchronization unit to follow the grid voltage reference. Most RESs use these types of converters for grid integration. Based on the power references they supply the power to the grid (both active and reactive power) [16]. The controllers of these converters are designed either in the synchronous

reference frame or stationary reference frame [17]. These converters work efficiently provided the grid is stiff. With the growing penetration of RESs, the point at which these converters are connected to the grid becomes weak due to the increased amount of grid impedance. Hence the stability of the controllers used by these converters is highly affected due to such weak grid connection. On the contrary, 'Grid-forming' type of converters is resistive to the weak grid operation. They have the self-synchronization ability which is mainly derived from the droop concept [18], [19]. Such type of synchronization is often termed as power synchronization [20]. These converters are vulnerable to large grid disturbances such as grid faults [20].

1.1.3 Grid Synchronization and Challenges

Grid-connected power converters especially the 'Grid-following' types require grid synchronization unit to remain connected with the grid. Using the grid synchronization, the essential grid voltage parameters such as amplitude, frequency and phase-angle are estimated for several applications. These include control of converters, fault detection, and fault-ride through operation.

a) Grid synchronization techniques:

Based on the control architecture, synchronization is classified as: a) Open-loop grid synchronization and b) Closed-loop grid synchronization as shown in Figure 1.3 (a) and Figure 1.3 (b) respectively. Open-loop grid synchronization techniques do not use any kind of feedback signals during the estimation process. Hence they feature unconditional stability. The grid synchronization dynamics are also fast for open-loop control. They require some filtering techniques for synchronization purposes. Filtering techniques use discrete Fourier transform (DFT) [21], [22], least square estimation [23], [24], low-pass notch filter [25],[26], Kalman filter [27], delayed-signal cancellation [28], moving average filter [29], etc. These filters need to be frequency-adaptive to avoid any amplitude or phase-angle offset during off-nominal

frequency variations. This necessitates an additional frequency detector which either degrades the open-loop features or adds more computational complexity.

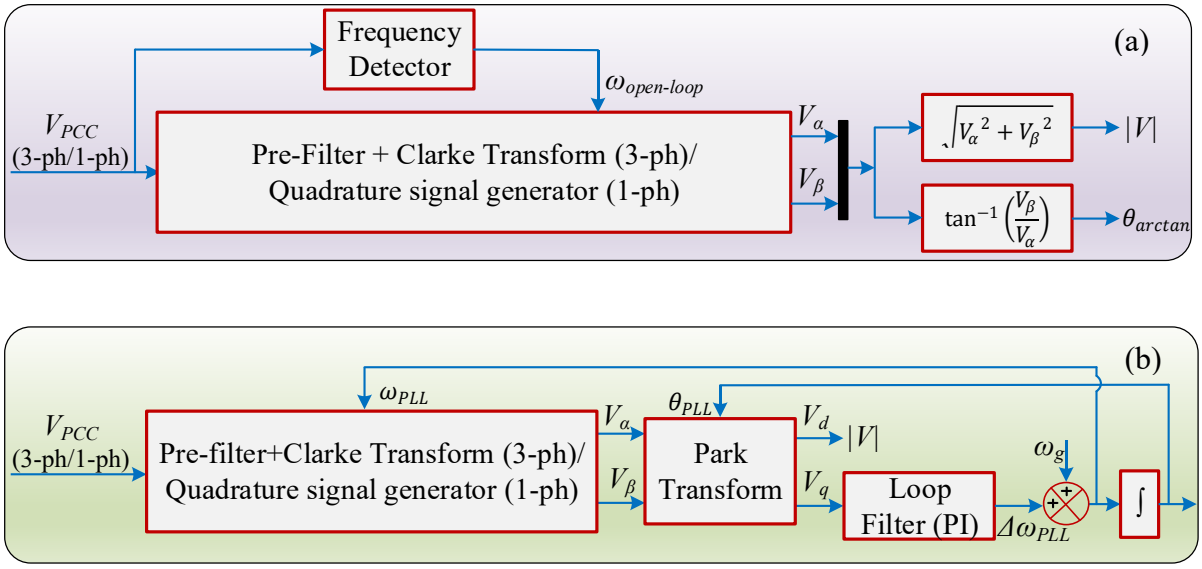


Figure 1.3 Grid Synchronization control architecture: (a) open-loop structure and (b) closed-loop structure.

In contrast, synchronous reference frame phase-locked loop (SRFPLL) is a widely used closed-loop grid synchronization technique. It consists of a phase detector, a loop-filter and a voltage controlled oscillator [30]. It offers a good trade-off between the accuracy and disturbance rejection capability during normal grid operating conditions. However, during grid unbalances and in the presence of lower order harmonics it requires extra filtering techniques. Moving-average filters (MAF) are used with SRFPLL in [31], [32]. This increases the filtering capability at the cost of slower dynamic response. The use of notch filter along with SRFPLL is proposed for selective harmonic elimination [33]. This increases the overall computational burden for the synchronization implementation. During grid voltage unbalances, to extract positive and negative sequence components use of two SRFPLL named as decoupled doubled SRFPLL (DDSRF-PLL) is proposed in [34]. This technique degrades the dynamic performance of the SRFPLL due to the inclusion of extra low-pass filters (LPFs). Additionally, during a fault having phase-angle jumps DDSRF-PLL highly suffers as the LPFs rely on the phase-

angle coupled frequency feedback from the SRFPLL. Similarly, at the cost of extra computational burden, use of complex band-pass filters (BPFs) as in-loop or pre-loop to SRFPLL is presented in [35]. The BPFs in this case require the frequency feedback from PLL as well. Hence, they are vulnerable to grid voltage phase-angle jumps like DDSRFPLL. The filtering capability of the classical SRFPLL can also be enhanced by using delayed-signal cancellation (DSC) as pre-filter. Their frequency-adaptive nature makes the implementation complex [36]. In contrast to DDSRF-PLL, dual second-order generalized integrator (DSOGI) based PLL has received attention due to its higher harmonic rejection capability and comparatively lower computation burden [37]. Its resonant frequency is dependent on the SRFPLL frequency estimation. Hence during any phase-angle jump based grid faults, the large oscillations observed in the PLL estimated frequency degrade the dynamics response of DSOGI. Apart from filtering requirements, attempts have been made to design adaptive synchronization techniques to improve the dynamics response during grid transients. These are adaptive SRFPLL [38] and enhanced PLL (EPLL) [39].

It is observed that though several advanced grid synchronization techniques have been proposed in the literatures, only few of them have considered the grid synchronization performance during the grid interaction of the power converters. This is the main objective of this thesis work. Industrial converters have not yet used these advanced grid synchronization techniques due to either of their computational complexity or cost. They still rely on the conventional SRFPLL technique as it provides accurate grid synchronization with simplicity in implementation. Due to the frequency and phase-angle coupling, SRFPLL suffers during grid faults having PAJs. Accordingly, the grid-connected converter's fault ride-through (FRT) performance is highly affected. An overview of synchronization challenges with the SRFPLL during grid faults is provided below.

b) Grid synchronization Challenges:

Grid synchronization challenges during a grid fault are studied as the 'loss of synchronization (LOS)' in the literatures. The LOS of the power converter during a grid fault may arise as a result of low voltage, high grid impedance or high current injection during FRT. The LOS phenomena can be explained referring to either large-signal instability (transient instability) or small-signal instability. As studied in [40], during grid faults having a low voltage level, the higher amount of active/reactive current injection by the converter leads to large-signal instability. The low frequency non-linear behaviour of SRFPLL is revealed as the cause for large-signal instability in [41]. In both [40] and [41], it is suggested that to avoid LOS the current injection during fault should be limited by the steady-state fault current limit. On the other hand, ref [42]-[45] claim that the LOS phenomenon is highly dependent on the existence of equilibrium points during fault and post-fault. The insight into the equilibrium point existence during grid fault is explained using phase portrait analysis [46]-[48]. This analysis provides high computational complexity and less physical insight [49]. The use of Lyapunov's direct method is proposed in [50], [51] to analyse the large-signal instability based LOS phenomenon which is considered an unresolved issue [49]. The concept based on classical power system fault analysis of conventional synchronous generators such as 'equal area criteria (EAC)' and 'swing equation' have been recently proposed for the understanding of LOS [52]. Apart from the stability analysis as mentioned in [40]-[52], several control enhancement methods have been proposed to improve the large-signal instability. For instance, the idea of 'freezing PLL' is proposed in [53], [54] which are less effective during the grid faults having PAJs. The ideas like zero current injection, line X/R dependent current injection, reduction of active current based on voltage drop are proposed in [55]-[57]. All these techniques either violate the grid code that delivers 1.0 pu/0.0 pu current injection or require precise measurement of grid impedance. The concept of modification to the SRFPLL by resetting its

integrator is proposed in [58], [59]. In this case, the proportional gain should be properly deigned to give a robust stability margin.

In contrast to large-signal, LOS can also happen due to small-signal instability. Small-signal instability is attributed to the weak grid interaction of the grid-connected converters. In this case, either high bandwidth of SRFPLL or high short circuit ratio (SCR) can cause instability. Small-signal instability is studied using state-space model or impedance-based analysis [60], [61]. Lower bandwidth of SRFPLL can enhance the small-signal stability by reducing the negative resistance offered by the SRFPLL in the low frequency region [62]. However, the low bandwidth of PLL highly degrades the dynamics of the converter controller during FRT. To improve small-signal stability, control techniques such as active damping on SRFPLL, virtual impedance, and feedforward are proposed in [63]-[66]. Insufficient damping and high settling time can lead to LOS during grid faults having PAJs.

The topic of loss of synchronization will be explained with the illustration of suitable examples of grid faults and FRT in Chapter-3 which is the main motivation and objective of this thesis.

1.1.4 Grid Faults and Fault Ride-through

As stated in 1.1.3, the main objective of the thesis relates to grid synchronization issue during a grid fault while the converter is operated in the FRT mode. In classical power systems, the faults are classified as: a) Symmetrical faults and b) Asymmetrical faults. The frequency of occurrence of symmetrical (balanced three-phase) faults is only 5% while for asymmetrical faults, the contributions from single-line to ground fault is 70%, line-line fault is 15% and double-line to ground is 10% [67]. The three-phase fault is considered as the most severe grid fault. During either symmetrical or asymmetrical grid faults, there are also chances of occurrence of phase-angle jumps (PAJs). The PAJ occurs due to the unequal X/R ratio between the fault and grid impedance values which further classify the faults into seven types [68].

These seven types of faults consider both magnitude sag and PAJs that can happen in a three-phase voltage during fault.

At the advent of any grid fault, the grid-connected converters are suggested to remain connected instead of suddenly tripping. Also they are expected to inject reactive power based on the grid code compliances (depends on the grid code of the country). Such phenomenon is called as the fault ride-through (FRT) or low voltage ride-through (LVRT). The reactive current is injected in accordance to the voltage level measured at the converter connection point (generally the PCC). This is considered as one of the stringent grid code requirements by the transmission system operator (TSO) or distribution system operator (DSO) of any country.

An ample amount of research work has been carried out in the literatures on the FRT of wind turbine energy system [69]-[78]. The rise of DC-link voltage during the occurrence of symmetrical fault is encountered and hence the implementation of chopper (in the form of extra resistance) is suggested to enhance the FRT in [69]-[71]. Similarly, the use of induction motor load near the PCC point is proposed to enhance the FRT and reactive current injection dynamics in [72]. The scheme for the reactive current injection by the wind turbine based on the improvement of the angle stability of nearby synchronous generator is proposed in [73]-[75]. The enhancement of FRT of wind turbine by advanced control methods that ensure the mitigation of overcurrent during fault is proposed in [76]. Other FRT studies based on the stability perspective are also proposed [77], [78]. All the aforementioned studies do not include the LOS phenomena during grid fault which can affect the FRT of the power converters due to synchronization instability as mentioned above. In contrast to wind energy, FRT of solar energy systems have recently received attraction due to their large-scale penetration and grid integration [79]-[82]. It is suggested that during grid faults, solar PV based power converters should inject reactive current in addition to riding through of the fault [83]-[86].

1.2 Motivation and Objectives

The motivation to carry out the research work is initiated from the occurrence of recent grid fault events across the world as shown in Figure 1.4 [87]-[90].

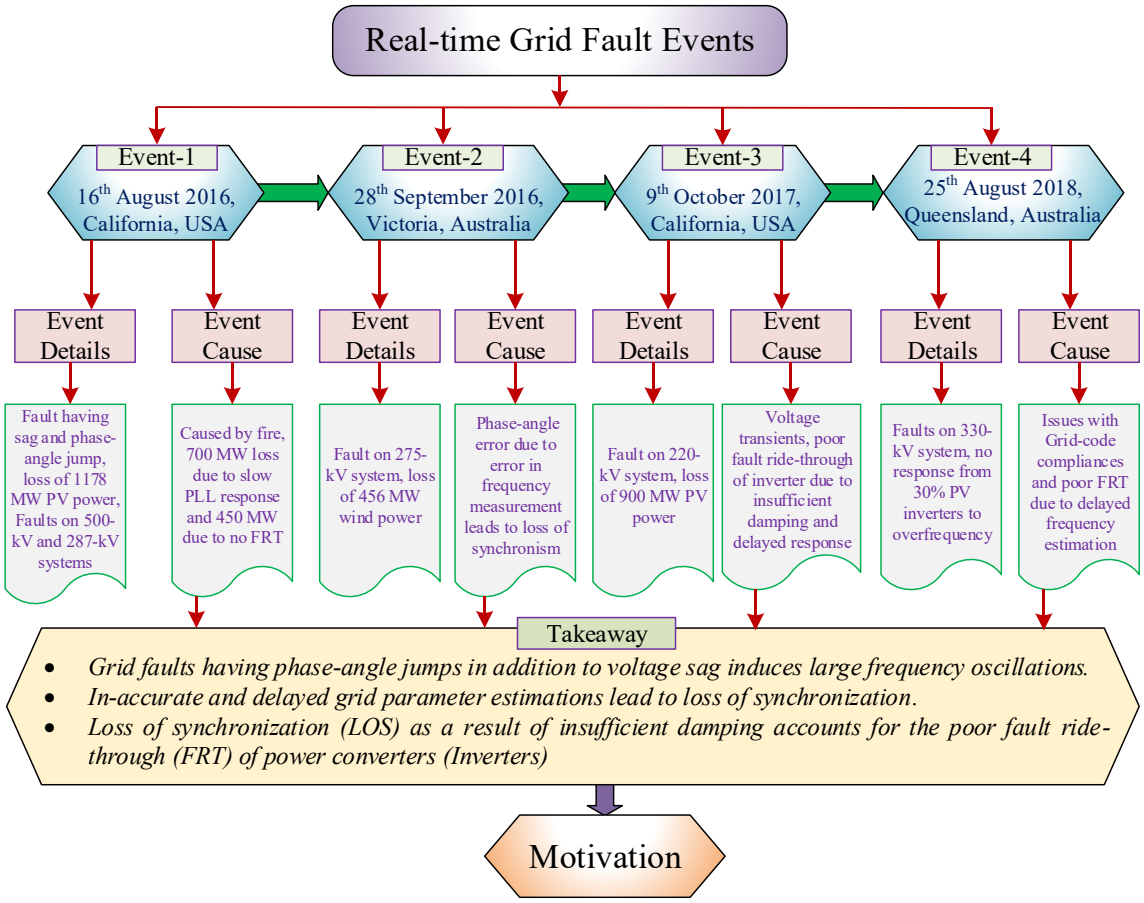


Figure 1.4 Real time grid fault event details.

From all these events, it is observed that the major cause of the failure of power converters is the inaccurate and delayed grid parameter estimations by the grid synchronization unit. Despite the extensive contributions in the field of grid synchronization in academia as mentioned in 1.1.3, the industrial converters are still relaying on the conventional synchronous reference frame phase-locked loop (SRFPLL). Most of the advanced grid synchronization techniques mentioned above have not been benchmarked with the consideration of the grid interaction of power converters (grid impedance is considered). As mentioned earlier, such interaction of the

grid-following converters lead to loss of synchronization during grid fault and degrade the FRT as a result of either large-signal [40]-[59] or small-signal instability [60]-[66]. Hence, the behaviour of the grid synchronization (especially SRFPLL) during grid faults having PAJ needs to be reinvestigated considering the converter interaction with the grid. To sum up, during a grid fault having PAJ, faster fault detection, accurate and smart grid synchronization along with the design of robust current controller is of utmost importance to enhance the FRT of power converters. To achieve these requirements, the objectives for the research work in this thesis are set as below:

1) Faster fault detection in grid-connected converter using advanced digital signal processing (DSP) techniques.
2) Reinvestigate the synchronization performance of SRFPLL and its adaptability to design parameters (proportional and integral gain) that account for the damping factor and settling time while considering several grid faults having PAJs. This is one of the tasks carried out in the thesis as in Chapter 3. This is done to understand and analyse the details of the loss of synchronization issue with SRFPLL as reported recently in real time during grid faults. The solution to this is presented in detail in the contribution section Part-II of Chapter 1.
3) Propose adaptive/hybrid grid synchronization techniques for both three-phase and single-phase power converters during PAJ associated grid faults.
4) Develop robust current controller with the proposed adaptive/hybrid grid synchronization to enhance the FRT of power converters (both three-phase and single-phase).
5) Investigate and compare the FRT of the power converters synchronized with the proposed technique with that of conventional SRFPLL and state-of-the-art adaptive PLL techniques considering both non-severe grid faults (voltage without PAJ) and

severe grid faults (voltage with PAJ) that illustrate the loss of synchronization (LOS) phenomena.

1.3 Methodology and Tools Used

The research work in this thesis is carried out using the switching model of a grid-connected voltage source converter (VSI). The model is built using software simulation tools such as MATLAB®/SIMULINK and PLECS® Blockset [91], [92]. The power circuit of the model is built using the PLECS toolbox. The version used is 4.1.8. The power circuit consists of the model for DC power supply, three-phase VSI (2-Level IGBT converter), single-phase VSI (Full-Bridge inverter), plant model (represented by *LCL* filter), the Thevenin equivalent of the grid model (represented by controlled AC voltage source with series impedance) and the Pulse-width Modulation (PWM). The control circuit for the grid-connected VSI is modelled using the SIMULINK toolbox (Version used is MATLAB® R2018b).

The outcomes deduced from the simulation analysis are validated using experimentation in real-time. For that purpose, a small laboratory-scale prototype of the grid-connected power converter is developed. In the prototype, the DC power supply is generated using the 'Magna-Power Electronics DC Power Supply Series' [93]. The VSI used for the experimental test set up is a commercial product from Danfoss A/S [94]. The actual grid is presented using a programmable AC power supply provided by the REGATRON 4-quadrant grid simulator [95]. Using this simulator, several grid fault voltage characteristics are programmed for testing purposes. The controller developed by the SIMULINK is interfaced with the experimental set up using the dSPACE-DS1103 controller board [96]. The details schematic of both the simulation model and experimental set up are provided in the appendix (refer Section B and Section C in the Appendix)

1.4 Major Contributions

The major contributions presented in the thesis consist of two parts. The first part (Part I) deals with the fault detection in grid-connected power converters. The second part (Part II) emphasises on the improved fault ride-through of power converters using hybrid grid synchronization transition. The details of these contributions are provided in the following.

Part I: **Fault detection in grid-connected power converters.**

Contribution: ***Hybrid Fault Detection for Grid-connected Power Converter***

A hybrid fault detection technique is proposed that consists of two digital signal processing techniques Hilbert-Huang Transform (HHT) and Teager Energy Operator (TEO). The three-phase grid voltage measured at the point of common coupling (PCC) is sampled and fed to the fault detection unit. Using the empirical mode decomposition (EMD), the first intrinsic mode function (IMF-1) of the fault voltage signal is extracted. Based on the HHT principle, the instantaneous amplitude and frequency information of the IMF-1 is acquired. These amplitude and frequency information of IMF-1 are used to calculate the Teager Energy which is equal to the square of the multiplication of the absolute values of amplitude and frequency. The energy calculated for IMF-1 is used to detect the fault conditions. With the proposed technique, grid faults having both voltage sags and phase-angle jumps (PAJs) are detected. The proposed fault detection technique is also used to classify the seven types of grid faults which include the unbalances in both grid voltage and PAJ. It is observed that the average teager energy calculated for three-phase symmetrical faults having PAJ (Type-A fault) is highest among other types of faults which illustrate the severity of three-phase faults.

Part II: **Improved fault ride-through (FRT) of power converters using hybrid grid synchronization transition.**

Contribution 1: ***Novel Three-phase Hybrid Grid Synchronization Transition***

In the second part of the thesis, the concept of three-phase hybrid grid synchronization for grid-connected power converter is introduced. It consists of hybrid phase-angle estimator for the current controller of the converter. The main objective behind the proposition is to improve the fault ride-through of converters during grid faults having phase-angle jumps (PAJs). The hybrid phase-angle estimator estimates the phase-angle of the grid voltage measured at the point of common coupling (PCC) using the conventional second order synchronous reference frame phase-locked loop (SRFPLL) during normal grid operating conditions. On the occurrence of the grid faults it switches to the arctangent based phase-angle estimation in the stationary reference frame ($\alpha\beta$-frame). On the recovery of the fault, it again switches back to the SRFPLL estimation. A novel transition scheme is proposed to control the hybrid phase-angle estimation. The scheme generates two pre-defined ramp functions as gain functions for the phase-angle transition by taking the phase-angle error as input signal. The phase-angle error is the difference between the arctangent and SRFPLL estimated phase-angle.

The proposed hybrid phase-angle estimator based hybrid grid synchronization works well considering three-phase balanced faults. In contrast, during the three-phase voltage unbalance as a result of asymmetrical faults, the hybrid grid synchronization concept is extended to enhance the frequency adaptability of the dual second-order generalized integrator (DSOGI) used as pre-filter (positive sequence extractor). The extension contains hybrid-frequency estimator which feeds the arctangent derived frequency to the DSOGI during PAJ associated grid faults instead of SRFPLL estimation.

The proposed hybrid frequency and phase-angle estimator under the concept of hybrid grid synchronization transition is tested during both symmetrical and asymmetrical grid faults having PAJ. Additionally, a benchmarking of its grid synchronization performance with the conventional second-order SRFPLL and other state-of-the-art techniques is presented. Accurate grid synchronization along with the minimization of the synchronization delay is achieved with the proposed technique. The contributions discussed above are included in Chapter-4.

Contribution 2: ***Novel Single-phase Adaptive and Hybrid Grid Synchronization Transition***

To improvise the frequency adaptability of the single-phase grid synchronization using second-order generalized integrator phase-locked loop (SOGIPLL) during grid faults having PAJs, two PLL independent frequency estimators are proposed. The estimators are: a) Teager Energy Operator (TEO) and b) Fixed Delay (FD) method. These two estimators provide the frequency estimations of the single-phase voltage signal using only a few samples, provided the voltage input to the estimators are normalized. Two types of normalization techniques are implemented: i) using the cascade structure recursive discrete Fourier transform and inverse recursive discrete Fourier transform based band pass filter (BPF) and ii) using the in-phase and in-quadrature output from SOGI based BPF. From the computational complexity point of view, the second option is selected by exploiting filtering capability of SOGI BPF. The normalized in-phase output signal of the SOGI is fed to the frequency estimators. The phase-angle is estimated using the arctangent function as done for three-phase systems. The frequency and phase-angle estimations are used for grid synchronization and current controller for grid faults having PAJs. The hybrid grid synchronization transition scheme proposed for three-phase systems is used for single-phase systems for the transition between hybrid frequency and phase-angle estimators.

It is revealed that during the normal grid operating conditions and faults having only voltage sag the SOGIPLL can serve as an efficient single-phase grid synchronization unit. On the other hand, for grid faults having PAJs, the SOGIPLL suffers due to the linearized phase-angle approximated frequency estimation feedback by SRFPLL. In such cases, the proposed adaptive and hybrid grid synchronization can be considered as an alternative to enhance the grid synchronization performance. All the above-mentioned contributions are addressed in Chapter-4.

Contribution 3: ***Fault Ride-Through of Power Converters using Hybrid Grid Synchronization Transition***.

This is focused on modelling of the current controller of the power converters that use the proposed hybrid grid synchronization transition during grid faults to deliver fault ride-through (FRT) capability. This discusses the control of both three-phase and single-phase power converters. For symmetrical faults, the converter's current controller is modelled in the synchronous reference frame (*dq*-frame) using the hybrid phase-angle estimator based hybrid grid synchronization. On the other hand, during asymmetrical grid faults, performances of the two types of current controllers are evaluated to inject positive sequence current during the FRT. The controllers implemented are: a) proportional plus integral plus second resonant (PIR_2) and b) proportional plus resonant (PR) along with both the hybrid frequency and phase-angle estimator based hybrid grid synchronization.

The FRT of three-phase power converter with the proposed hybrid grid synchronization is investigated during several grid faults having PAJs using both simulation and experiments. The test scenarios considered under study are, i) Non-severe symmetrical faults and PAJs, ii) severe symmetrical faults and PAJs and iii) Asymmetrical faults and PAJs. The comparison of current controller performance during FRT is made with the conventional SRFPLL and other modified

PLL structures. A comparison of the proposed technique with the addition of PCC voltage feedforward compensation is also carried out. The details of the FRT of three-phase converters are provided in Chapter-5.

In contrast to three-phase converters, the FRT of single-phase converters are modelled using the proportional plus resonant (PR) current controller. The frequency adaptability of the PR current controller is enhanced using the proposed adaptive and hybrid single-phase grid synchronization during the grid fault having PAJ. The performance comparisons of the FRT of the single-phase converters are made using simulation studies. The responses along with the converter control model are addressed in Chapter-6.

1.5 List of Publications

[1] **A. Sahoo**, K. Mahmud, J. Ravishankar, "An Enhanced Frequency-Adaptive Single-phase Grid Synchronization Technique," [accepted and in-press *in IEEE Transaction on Instrumentation and Measurement*]

[2] **A. Sahoo**, J. Ravishankar, M. Ciobotaru, F. Blaabjerg, "Enhanced Fault Ride-through of Power Converters Using Hybrid Grid Synchronization," [accepted and in-press in *IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE)*]. https://ieeexplore.ieee.org/abstract/document/9336683

[3] **A. Sahoo**, J. Ravishankar, M. Ciobotaru, P. Sajeevikumar, "Improved Low Voltage Ride-Through Performance of Single-phase Power Converters using Hybrid Grid Synchronization," in *(IECON) 2020-46th Annual Conference of the IEEE Industrial Electronics Society*, IEEE. https://ieeexplore.ieee.org/document/9254513

[4] **A. Sahoo**, A. Arunan, K. Mahmud, J. Ravishankar, M. S. H. Nizami and M. J. Hossain, "Teager-Huang based Fault Detection in Inverter-interfaced AC Microgrid," *2019-19th IEEE International Conference on Environment and Electrical Engineering and 2019 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, Genova, Italy, 2019, pp. 1-5. https://ieeexplore.ieee.org/document/8783453

[5] **A. Sahoo**, K. Mahmud, M. Ciobotaru, J. Ravishankar, "Adaptive Grid Synchronization Technique for Single-phase Inverters in AC Microgrid," In Proceedings of the *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 29 September–3 October 2019; pp. 4441–4446. https://ieeexplore.ieee.org/document/8911834

Research work carried out in this thesis have also been contributed to other co-authored publications related to inverter-interfaced Microgrid. The contents are not included in this thesis. However, the work below greatly enhanced the understanding of inverter control principles and helped come up with the thesis motivations. The details can be found as below.

[1] **A. K. Sahoo**, K. Mahmud, M. Crittenden, J. Ravishankar, S. Padmanaban and F. Blaabjerg, "Communication-less Primary and Secondary Control in Inverter-Interfaced AC Microgrid: An Overview," *IEEE J. Emerg. Sel. Top. Power Electron.* (accepted and in-press). https://ieeexplore.ieee.org/document/8999492

[2] K. Mahmud, **A. K. Sahoo**, J. Ravishankar, and Z. Y. Dong, "Coordinated multilayer control for energy management of grid-connected AC microgrids," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7071–7081, Nov./Dec. 2019. https://ieeexplore.ieee.org/document/8778673

[3] M. Ali, **A. Sahoo**, H. I. Nurdin, J. Ravishankar and J. E. Fletcher, "On the Power Sharing Dynamics of Parallel-Connected Virtual Oscillator-Controlled and Droop-Controlled Inverters in an AC Microgrid," IECON 2019 – *45th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Lisbon, Portugal, 2019, pp. 3931-3936. https://ieeexplore.ieee.org/document/8927510

[4] **A. Sahoo**, K. Thattai, J. Ravishankar and M. Ciobotaru, "Power-Sharing Based on Open-Loop Synchronization of Inverters in an Islanded AC Microgrid," *44th Annual Conference of the IEEE Industrial Electronics Society* (*IECON*), Washington, DC, 2018, pp. 237-242. https://ieeexplore.ieee.org/document/8591713

[5] **A. Sahoo**, M. Ciobotaru and J. Ravishankar, "A Novel Communication-less Frequency Restoration Technique in Droop Controlled Inverter-based Islanded AC Microgrid," *IEEE International Conference on Power Electronics, Drives and Energy Systems* (*PEDES*), Chennai, India, 2018, pp. 1-6. https://ieeexplore.ieee.org/document/8707686

[6] **A. Sahoo**, K. Thattai and J. Ravishankar, "Fault Detection in an Islanded Inverter Based Microgrid Using Recurrence Plot Analysis," *IEEE Innovative Smart Grid Technologies - Asia* (*ISGT Asia*), Singapore, 2018, pp. 658-663. https://ieeexplore.ieee.org/document/8467862

[7] K. Thattai, **A. Sahoo**, J. Ravishankar, "Teager energy operator based fault detection and classification technique for converter dominated autonomous AC microgrid," Proc. *IECON 2018 – 44th Annu. Conf. IEEE Ind. Electron. Soc.*, vol. 1, no. October, pp. 294–299, 2018. https://ieeexplore.ieee.org/document/8591762

1.6 Thesis Organization

The aforementioned research contributions and outcomes are addressed and incorporated by organizing the thesis into seven chapters as follows:

Chapter-2 begins with an overview of existing fault detection techniques in classical power systems and modern power electronic based power systems using digital signal-processing techniques. Further, the proposed 'Teager-Huang' based fault detection for grid-connected converter is detailed with detection principle, algorithm and test scenarios such as grid faults having different voltage sags and PAJs.

Chapter-3 explores the loss of grid synchronization (LOS) phenomena during grid faults. A clear picture of the difference between the chances of large-signal and small-signal instability based LOS with the SRFPLL are provided with mathematical analysis. To this end, with suitable grid fault events the occurrences of LOS are illustrated via simulation analysis.

Chapter-4 introduces the concept of adaptive/hybrid grid synchronization transition for both three-phase and single-phase grid voltages. The control implementation, and transition scheme along with the mathematical details are provided in this chapter. Finally, benchmarking of the grid synchronization performance of the proposed technique with the state-of-the-art techniques is carried out separately for three-phase and single-phase grid voltages.

Chapter-5 deals with the design of current controller for three-phase converters and the fault ride-through strategy synchronized with the proposed hybrid grid synchronization transition. Detailed model development with the consideration of grid synchronization (SRFPLL) and voltage feedforward compensation is presented. The FRT response of the developed current controller using both simulation and experiments are presented in this chapter along with comparisons with the other techniques by considering both symmetrical and asymmetrical grid faults having PAJs.

Chapter-6 investigates the FRT of single-phase converter during grid faults. The model development including reference current generation scheme and frequency adaptability of the current controller are discussed. The converter is synchronized with the proposed adaptive/hybrid grid synchronization principle. The simulation analyses are presented to validate the improved FRT with the proposed technique in comparison to the conventional technique.

Chapter-7 summarises the research outcome presented in the above chapters. Additionally, it provides an insight to the future research directions to the current research work discussed in the thesis.

Chapter 2

Fault Detection in Grid-Connected Power Converters

Power electronic converters are widely used for the grid integration of various renewable energy sources to deliver fossil fuel free power demand. The source side intermittency during such renewable based power generation along with the grid side disturbances affect the normal operating conditions of such power converters. One of the vital grid side disturbances is the occurrence of grid faults. In such scenarios, the limited fault current tolerance (2-3 times of rated current) of power converters during their grid-connected application demands the necessity of faster and accurate fault detections. Knowledge and application of several digital signal processing (DSP) techniques have been proposed in the growing body of literatures to achieve faster fault detection to safeguard the power electronic interface during grid side disturbances. This chapter initially provides an overview of such DSP techniques for fault detection. In addition to this, it proposes a hybrid technique that includes two well-known signal processing techniques, Teager Energy Operator (TEO) and Hilbert-Huang Transform (HHT). The combined principle is called a Teager-Huang technique, which can detect different line faults using the teager energy of the Hilbert-Huang based empirical mode decomposed signals. The fault detection technique is verified by creating various symmetrical and unsymmetrical faults at the inverter connection point to the grid, using MATLAB/SIMULINK and PLECS.

2.1 Introduction

The environmental concerns of greenhouse gas emission with the energy production using the conventional sources e.g., oil and natural gas, demand for the new regime of renewables and hence foresee the future growth of the energy sectors. The expeditiously evolving renewable energy sources (RESs) such as solar and wind energy systems under the new power generation paradigm are becoming successful to provide clean energy and thereby replacing the conventional energy sources. The favourable climatic condition in addition to the unprecedented large-scale penetration of such renewables has propelled the supply of efficient and uninterruptable energy to fulfil the customers' demand.

Grid integration of these renewable energy sources is an emerging topic in both academia and industry. The primary purpose of this is to feed in the energy generated (in the form of DC) to the existing utility grid (in the form of AC). Power electronic converters are key components which are used mainly for power conversion at different stages (DC/DC or DC/AC) and grid integration of RESs. These power converters feature advanced control systems, reduced size, low cost along with higher energy efficiency during the power conversion and grid integration [97].

On the other hand, unlike the conventional synchronous generator, these converters provide less inertia or inertia-less control performance. This makes them vulnerable to either source side or grid side disturbances. The disturbances from the grid side may occur due to various faults such as symmetrical or asymmetrical which result in voltage sags and phase-angle jumps (PAJs) [68]. Due to these disturbances, the power electronic converters are exposed to issues like over current stress, grid synchronization error, and distorted grid current injection, to name a few. These may eventually lead to the trip of the converters provided the fault current magnitude injected by them exceeds 2-3 times their rated value [98]. Further, the impose of

stringent modern grid code by the transmission system operator (TSO) and distribution system operator (DSO) of any country on these power converters requires them to stay connected with the faulty grid to inject reactive power for a specified amount of time (known as “Fault Ride-through”).

All the above-mentioned issues and requirements during the grid fault, urge to go for the fast and accurate fault detection to safeguard these power electronic components and hence their tripping to offer resilient grid-connected operation. There have been a large amount of literatures in the last couple of decades devoted to the fault detection either in the conventional power system or modern power electronic based power systems [99]. It is worth noting that many fault detection techniques that are applicable to the conventional power system having synchronous generator are not suitable for the power electronic based system due to their limited fault current carrying capacity [100]. Out of several fault detection methods, digital signal processing (DSP) technique based detection are well appreciated due to their faster and accurate detection in power electronic based power systems which is the main objective of this chapter.

2.1.1 Contribution and Organization of this Chapter

This chapter begins with an overview of digital signal processing (DSP) techniques used for fault detection in Section 2.2. The classification is presented based on three categories: a) Frequency Domain Techniques, b) Time-frequency Techniques, and c) Hybrid Techniques. Section 2.3 proposes a hybrid fault detection method that uses the combination of two signal processing techniques, Hilbert-Huang Transform (HHT) and Teager Energy Operator (TEO). Under this section, sub-section 2.3.1 provides the fault detection principle and sub-section 2.3.2 explains the system model under study for fault detection. Section 2.4 presents the simulation

analysis of fault detection considering the typical seven types of power system faults. The summary of this chapter in provided in Section 2.5.

2.2 Overview of Digital Signal Processing Techniques for Fault Detection

The flow-chart of the classification studied is shown in Figure 2.1.

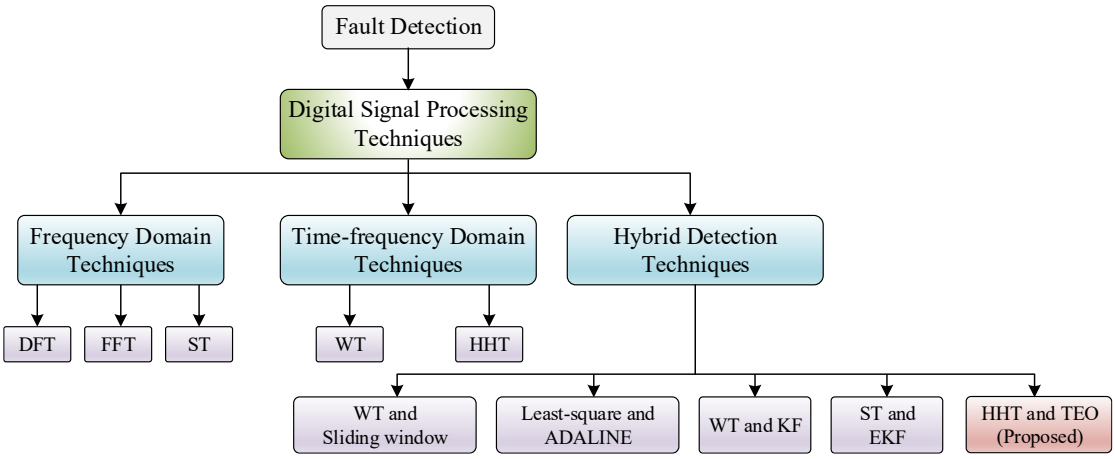


Figure 2.1 Overview of digital signal processing (DSP) techniques for fault detection.

*DFT: Discrete Fourier Transform, FFT: Fast Fourier Transform, ST: S-Transform, WT: Wavelet Transform, HHT: Hilbert-Huang Transform, KF: Kalman Filter, EKF: Extended Kalman Filter, ADALINE: Adaptive Linear Neuron or later Adaptive Linear Element

2.2.1 Frequency Domain Techniques

a) Discrete Fourier Transform (DFT)

It is used to transform finite sequence equally-spaced samples of a time domain signal to the same length sequence of equally spaced frequency domain signal [101]. The DFT of any sampled signal $x[n]$, can be given by

$$X[k] = \sum_{n=0}^{N-1} x[n] e^{\frac{j2\pi kn}{N}} \tag{2.1}$$

In (2.1), N represents the total number of samples present in the signal $x[n]$, k is the number of frequency bins: $k = 0, 1, 2, \ldots, N\text{-}1$. Both magnitude and phase-angle information of the signal can be obtained from $X[k]$. The frequency resolution (Δf) for a sampling frequency (f_s) can be calculated as $\Delta f = \frac{fs}{N}$. The frequency domain components of $X[k]$ are used to detect any fault instant happening in the time domain by extracting the magnitude and phase-angle information.

DFT has been used widely for fault detection in the field of conventional power system and for Microgrid (MG) applications. A fast recursive DFT is used for adaptive numerical relay settings in [102], and the application is further extended to both islanded and grid-connected MG in [103]. A DFT based fault feature extraction is proposed in [104] for the protection of MG. Here, the features like magnitude, phase-angle and frequency of the measured voltage and current signals are considered to provide fault information. DFT provides faster and intelligent fault detection performance in a stiff grid-connected system (low rate of change of frequency (ROCOF). However, in case of autonomous Microgrid, either interpolated-discrete Fourier transform with variable time window or Hilbert Transform (HT) can be used to arrest large ROCOF due to any transient disturbance. Further, with this technique scenarios like fault location, and high impedance fault (HIF) have not been researched thoroughly.

b) Fast Fourier Transform (FFT)

This is an optimized implementation of DFT discussed above. Performance wise it is much faster and efficient than DFT. It is the collection of various fast computing DFT techniques. It highly reduces the computational time as compared to DFT. For instance, FFT based DFT computation provides complexity of *NlogN* while it is N^2 times for direct DFT technique. Additionally, FFT reduces the round-off errors during the computation.

FFT has been used extensively in power systems to detect several transient phenomena along with faults [105]-[109]. The main drawback of FFT algorithm is the leakage effect. This method is also sensitive to frequency deviations.

c) S-Transform (ST)

This is an extension of wavelet transform (WT) and short-time Fourier transform. It is mainly used for PQ disturbance detection [110]. The mathematical expression for ST of a time domain signal $x(t)$ can be expressed by

$$S(\tau, j) = \int_{-\infty}^{\infty} x[t] w(t-\tau, j) dt \tag{2.2}$$

In (2.2), $w(t\text{-}\tau, j)$ is time-scaled replication of the mother wavelet which will be defined in the next sub-section. The width of mother wavelet and the resolution of transformation are determined by the dilation parameter '*t*'.

To extract features like mean, entropy of time-frequency contour, and standard deviation energy from the measured current of the distribution feeder, S-transform is used in [104] for pre-processing. Moreover, a differential protection scheme based on S-transform is presented

in [111]. The protection scheme is used to detect various faults in a varying network configuration of MG. The fault location and classification is not included in the scope of [111].

2.2.2 Time-frequency Domain Techniques

a) Wavelet Transform (WT)

It is an efficient digital signal processing tool which analyses different frequency components of the time domain signal individually with a unique resolution for each frequency component. In contrast to Fourier Transform, WT represents the time domain signal by the summation of different mother wavelet functions [112]. Mother wavelets are implemented as bandpass impulse response filters with an adjustable time width that corresponds to the frequency component of the signal, i.e., it provides a narrow time width for higher frequency components and a wider time width for lower frequency components. The necessary condition to be satisfied by any mother wavelet ($\psi(t)$) is given by

$$\int_{-\infty}^{\infty} (\psi(t))^2 \, dt \; < \infty \tag{2.3}$$

Various mother wavelets are available such as morlet, daubechies (db), symlets, Mexican hat, haar, biorthogonal, coiflets, etc. All these mother wavelets can follow a common mathematical operation for scaling/dilation and translation/shifting as given by

$$\psi_{a,b}(t) = \frac{1}{\sqrt{a}} \psi\left(\frac{t-b}{a}\right) \tag{2.4}$$

Where the dilation/scaling is done by factor 'a' and translation/shifting is done by factor 'b'. The scaling factor for the wavelet function is decided by the length of the filter corresponding to a particular mother wavelet. WT is used either in the form of Continuous Wavelet Transform (CWT) or Discrete Wavelet Transform (DWT).

WT is used for transient disturbance detection in [113]. Fault feature extraction based on WT function for MG protection is proposed in [114]. Similarly extracting useful features such as energy change, entropy and standard deviation of the measured fault current using WT is presented in [115]. The calculation of WT coefficients by the positive sequence current components measured at the point of common coupling for fault identification is proposed in [116]. A wavelet packet transform (WPT) based digital protection scheme is proposed in [117] where the high frequency components present in the synchronous reference frame (*dq*-frame) are extracted by the WPT coefficients which are further used for fault identification in both islanded and grid-connected applications [118].

The challenging part of the fault detection using WT is the selection of mother wavelet function and the number of signal decomposition levels. Higher number of signal decomposition levels provides higher accuracy at a higher cost and computational complexity. Mother wavelet selection should be done based on the sampling of the input signal data.

b) Hilbert-Huang Transform (HHT)

Any non-linearity and transient events contained in a sinusoidal signal can be decomposed in to various layers of signals containing varying frequencies. The process of such decomposition of signals from the highest frequency content to the lowest is called empirical mode decomposition (EMD). Each decomposed layer is called the intrinsic mode function (IMF). The extractions of IMFs are done following certain conditions as:

1. Maximum and minimum of the signal $x(t)$ is identified and spline interpolation is used to construct the upper and lower envelop as $e_m(t)$ and $e_M(t)$. Using these two parameters the mean value m(t) is calculated as

$$m(t) = \frac{e_m(t) + e_M(t)}{2} \tag{2.5}$$

2. New signal $h(t)$ is constructed as (2.6)

$$h(t) = x(t) - m(t) \tag{2.6}$$

It follows two conditions: (a) its average value is zero and (b) the local extrema are equal to the number of zero crossings or differ at most by one.

3. Steps (1) and (2) can be repeated until $h(t)$ satisfies the conditions to be an IMF.

4. The residual $r(t)$ can be calculated as

$$r(t) = x(t) - \sum_{i=1}^{M} IMF_M \tag{2.7}$$

The magnitude and frequency of each IMF (analytical signal) can be estimated using Hilbert-Huang technique. Any analytical signal (IMF) can be represented as

$$z(t) = x(t) + jy(t) \tag{2.8}$$

Instantaneous amplitude and instantaneous frequency of $z(t)$ can be estimated as

$$A(t) = \sqrt{x^2(t) + jy^2(t)} \tag{2.9}$$

$$f(t) = \frac{1}{2\pi t} \tan^{-1} \frac{y(t)}{x(t)} \tag{2.10}$$

2.2.3 Hybrid Techniques

Apart from the DSP techniques in frequency and time-frequency domains described above, recently the combination of multiple DSP techniques are used for fault detection purposes. They are called hybrid techniques. The combination of WT and sliding-window is proposed for the detection of voltage sag during a fault in [119]. Further, fault detection using the combination of Least Square (LS) and ADALINE is presented in [120]. With lower computational complexity, both the WT and Kalman Filter (KF) are used for voltage disturbance detection in [121] along with Fuzzy-expert system for classification. Detection of short duration disturbances using the combination of Extended KF (EKF) and ST is proposed in [122].

Motivated with the performance improvement using the hybrid fault detection unit during several faults, in this thesis, the combination of two DSP techniques is proposed to detect various types of fault occurrences at the PCC of a grid-connected converter system. The techniques are HHT and Teager Energy Operator (TEO) [123]. The hybrid technique is called ‘Teager-Huang’.

2.3 Teager-Huang based Fault Detection

Authors in [124] suggested that the use of the Teager Energy Operator (TEO) technique provides faster fault detection. As reported by [124], its speciality is that it can identify disturbances in a signal using only 3-5 samples of the frequency and amplitude. The TEO method is used in various studies such as induction motor fault diagnosis [125], negative sequence current energy [126] estimation during both symmetrical and unsymmetrical faults, and low frequency oscillation detection [127], [128]. However, researchers paid a little attention [129], [130] to use this technique to detect the faults in an inverter-interfaced grid faults. It appears that the TEO technique in combination with the HHT can be used to detect several types of grid faults that are measured at the PCC where the inverter is connected. This fault detection principle, the system model which is used for the study and simulation results are presented below.

2.3.1 Hybrid Detection Principle

Any of the single-phase signal ($x_a(t)$) of the measured three-phase voltage signal can be represented as a sinusoid (sine/cosine) as

$$x_a(t) = X_a \cos(\omega t + \theta_a) \tag{2.11}$$

The discrete equivalent of the time domain signal sampled at T_s= 10 kHz can be represented as

$$x_a(n) = X_a \cos(\Omega n + \theta_a) \tag{2.12}$$

where $\Omega = (2 \times \Pi \times f \times T_s)$, f = analog frequency and θ_a is any arbitrary phase angle associated with signal $x_a(n)$ .It requires three samples as $x_a(n), x_a(n-1), and\ x_a(n+1)$ to find out the energy as given by

$$E[x_a(n)] = \frac{1}{{T_s}^2}[x_a(n)^2 - (x_a(n)(n-1) \times x_a(n)(n+1))] \quad (2.13)$$

With these three samples the energy of the signal $x_a(n)$ can be found with the help of teager energy operator using (2.13)

From (2.13) the previous and future samples of $x_a(n)$ can be written as

$$x_a(n-1) = X_a \cos(\Omega(\mathrm{n}-1)) + \theta_a \quad (2.14)$$

$$x_a(n+1) = X_a \cos(\Omega(\mathrm{n}+1)) + \theta_a \quad (2.15)$$

Equations (2.14) and (2.15) can be solved using trigonometric identities given by equations as

$$\cos(\alpha+\beta)\cos(\alpha-\beta) = 0.5 \times [\cos(2\alpha) + \cos(2\beta)] \quad (2.16)$$

$$\cos(2\alpha) = 2[\cos(\alpha)]^2 - 1 = 1 - 2[\sin(\alpha)]^2 \quad (2.17)$$

On solving equations (2.16) and (2.17), equation (2.13) can be written as

$$E[x_a(n)] = \frac{1}{{T_s}^2}[x_a(n)^2 - (x_a(n-1) \times x_a(n+1))] = \frac{1}{{T_s}^2}[{X_a}^2 \sin^2(\Omega)] \quad (2.18)$$

For small values of Ω, $\sin(\Omega) = \Omega$

So, the teager energy of the signal can be calculated instantaneously from the squared multiplication of the amplitude (X_a) and frequency (ω) as given by

$$E[x_a(n)] = \frac{1}{{T_s}^2}\left[{X_a}^2\Omega^2\right] = {X_a}^2\omega^2 \quad (2.19)$$

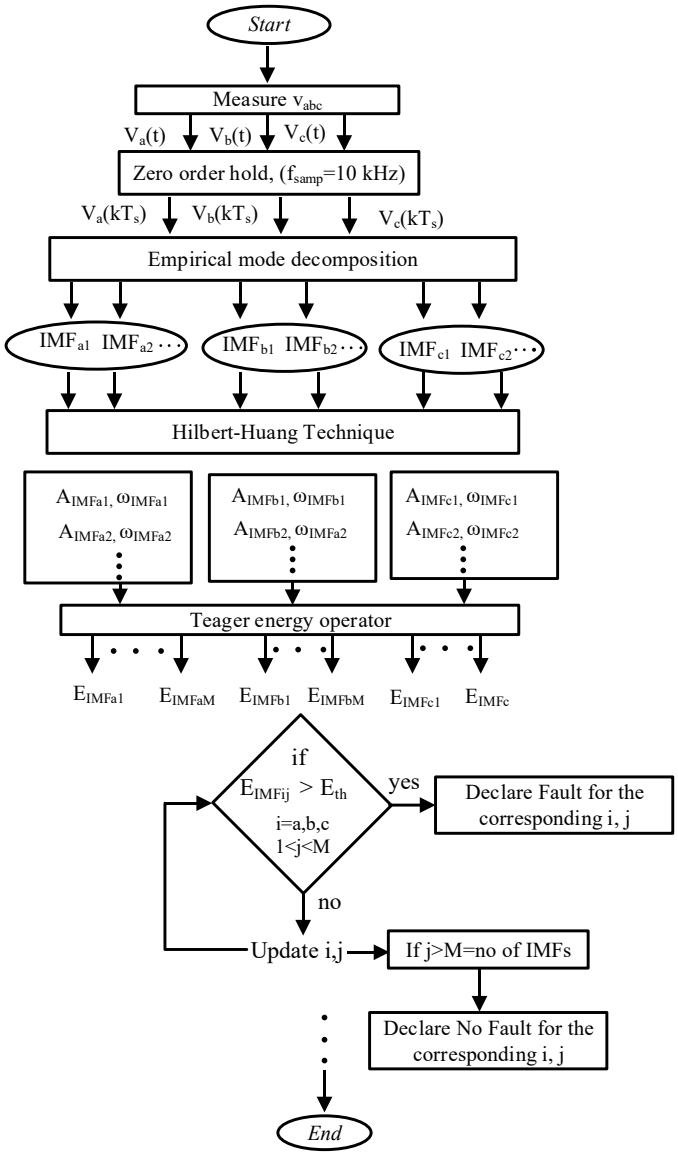


Figure 2.2 Flow-chart implementing Teager-Huang based fault detection.

Based on the two signal processing techniques, HHT and TEO, the flowchart for the combined technique in order to detect various symmetrical and asymmetrical grid faults in inverter-based MG is shown in Figure 2.2. It is observed that teager energy operator requires instantaneous amplitude and frequency to estimate the energy of a signal. These amplitude and frequency values are extracted using Hilbert-Huang technique and given to the energy operator to calculate the energy. This is done for every extracted IMF for each faulty voltage signal. It is noticed that in each fault case, the maximum information of amplitude and frequency is

contained in the IMF-1 compared to other IMFs. So in order to extract accurate information about the faulty phase energy, the IMF-1 energy alone is calculated using the teager operator .

2.3.2 System Description

The schematic of the grid-connected three-phase converter used for fault detection study is shown in Figure 2.3. The converter and controller parameters used to model the system are provided in TABLE 2.1. It consists of plant model (*LCL*-filter), thevenin model of grid, grid synchronization, outer DC-link voltage control, inner current control and pulse width modulation (PWM). Several types of short-circuit faults are created at the grid side and the voltage measured at PCC is fed to "Teager-Huang' fault detection unit to generate the 'trip' signal as shown in Figure 2.3.

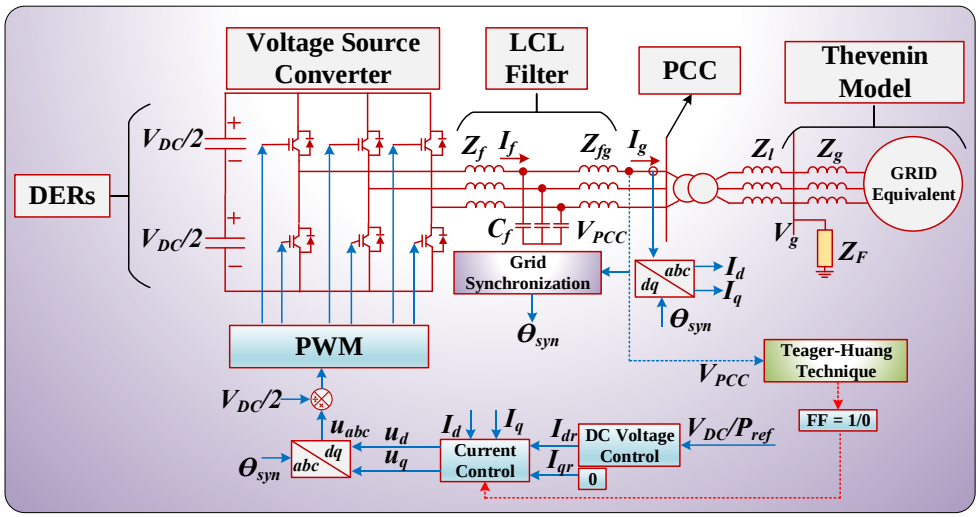


Figure 2.3 Grid-connected converter model for fault detection study.

TABLE 2.1: CONVERTER AND CONTROLLER PARAMETERS

Parameters and Symbols	Values
Rated Power (P_{rated})	2.2 kW
DC voltage (V_{DC})	400 V
Grid voltage (Secondary side) (V_g)	240 V_{rms}
PCC voltage (Primary side) (V_{PCC})	120 V_{rms}
Nominal current (Primary side) (I_N)	8.65 A_{peak}
Grid Frequency (f_g)	50 Hz
Proportional gain of the voltage control (K_{pV})	8
Integral gain of the voltage control (K_{iV})	7000
Proportional gain of the current control (K_{pi})	12
Integral/Resonant gain of the current control (K_{ii}/K_{ir})	7000
Settling time of the SRFPLL (t_{set})	120 ms
Grid side filter inductance (L_{fg})	1.8 mH
Converter side filter inductance (L_f)	0.5 mH
Sampling frequency (f_{sam}) and Switching frequency (f_{sw})	10 kHz

The computational time of the proposed Teager-Huang method is recorded in an Intel ®, Core ™, i7-6700 CPU @ 3.40Ghz processor computer. On average, the Teager energy calculation for one cycle (200 instantaneous energy calculations) takes 3ms. This is less than the recommended fault detection as per IEEE C37.114-2014 standard (10 ms to 50 ms).

2.4 Simulation Results

The simulation results to detect the faults using the proposed technique are provided in three scenarios. The first scenario results are provided for the model description provided in [123]. Second and third scenario results are the further analysis of the proposed fault detection technique corresponding to different characteristics of grid faults such as: variation in sag depth and phase-angle jumps (PAJs) during the grid fault occurrence.

a) Variation with Fault Resistance

For a single-line to ground (AG) fault, phase A voltage and all the IMFs of the phase A voltage are plotted in Figure 2.4. Here, the fault has occurred at the 0.7^{th} second. It can be clearly seen that the first IMF (IMF 1) is carrying more information of the fault. Hence, only the IMF 1 is considered for further analysis. The teager energy is calculated from (2.19).

The maximum teager energy depends on the fault resistance value as well. As shown in Table 2.2, the teager energy for low resistive faults is much higher compared to high resistive faults. The threshold set value should be able to detect all types of faults including the high resistive faults. The Teager energy during normal operation of the system is identified as 0.1×10^{11}J. To maintain the grid code in a MG, the voltage sag value allowed is 0.9 times the rated value. Therefore, at this magnitude of each phase voltage, the energy of the first IMF signal is calculated and chosen as threshold value by performing the test simulation for several times. If energy value of any IMF signal rises above the threshold, then it is considered as fault energy and the IMF corresponding to the phase (phase A, B, or C) is declared as faulty phase.

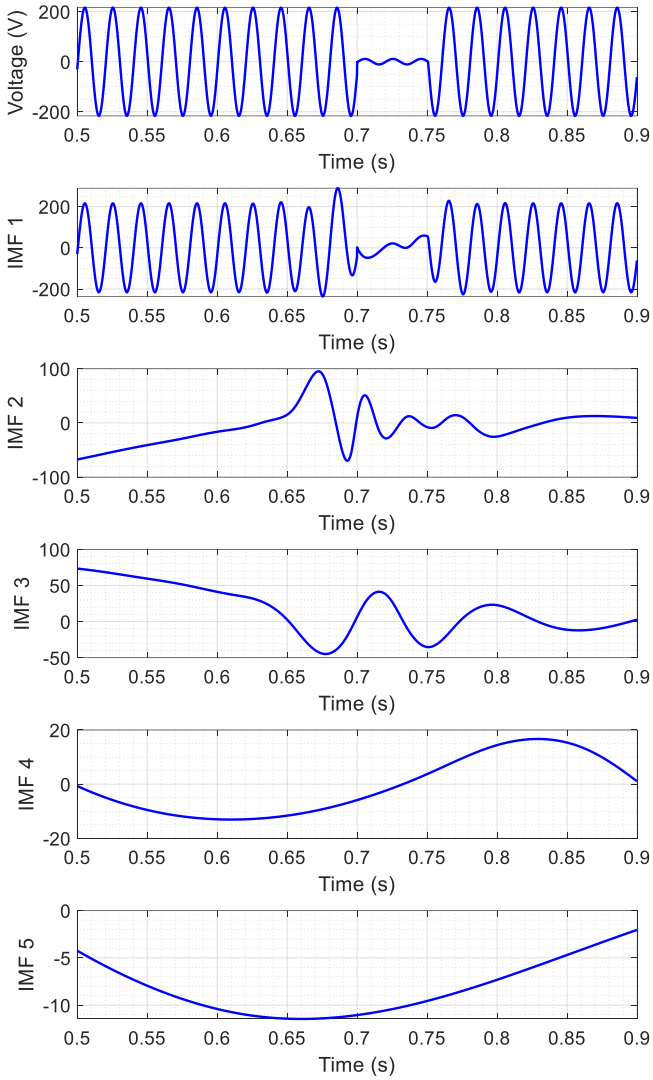


Figure 2.4 Phase-A voltage and all its IMFs during single-line to ground (AG) fault.

TABLE 2.2: TEAGER ENERGY AND FAULT RESISTANCE

Fault type	Fault resistance (Ω)	Teager energy (J)
LG	1	1.323×10^{11}
	10	0.837×10^{11}
LLG	1	4.143×10^{11}
	10	2.935×10^{11}
LL	1	2.706×10^{11}
	10	
LLLG	1	8.243×10^{11}
	10	7.113×10^{11}

b) Impact of addition of PAJ to Voltage Sag

As mentioned previously, the teager energy during a fault is proportional to square of the magnitude of the 1st intrinsic mode function (IMF-1) derived by performing the empirical mode decomposition of the phase voltage using the HHT technique. The impact of voltage sag depth measured at the PCC point during the fault is studied by varying it from 10% (0.1 pu) to 90% (0.9 pu) of the rated voltage. The estimated teager energy for varying sag depth is shown in Figure 2.5. The instantaneous energy values of the IMF-1 for each of the phases (A, B and C) are shown. Additionally, the average energy values of all the three phases are plotted. It is observed that the average teager energy significantly increases after voltage sag of 70% (0.7 pu). The average teager energy for 90% sag (0.9 pu) is calculated as 1.5×10^{18}J.

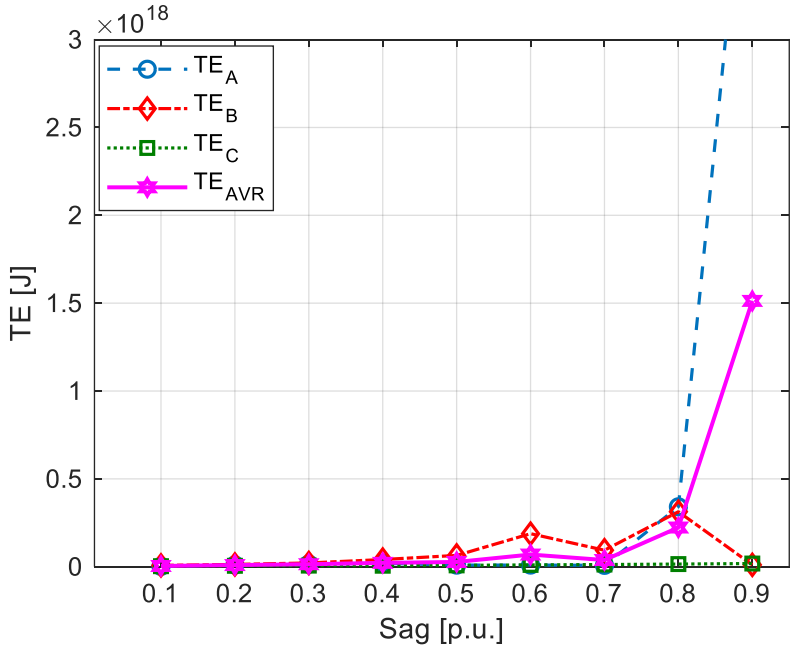


Figure 2.5 Variation of teager energy of IMF-1 with respect to different sag depth of the voltage during the grid fault.

In addition to the voltage sag, there is also a chance of occurrence of phase-angle jumps (PAJs) during a grid fault. PAJs occur due to the unequal X/R ratios between the fault and the grid impedance [68]. The impact of PAJ with a common 80% voltage sag on the estimated teager energy is shown in Figure 2.6, where PAJ is varied from -60° to 60°. It is observed that irrespective of the sign of the PAJ, the average teager energy of all three phases' increases with the increase in PAJ with respect to sag depth. This is due to the fact that during a PAJ both amplitude and frequency of the voltage signal abruptly changes which in turn affects the IMF-1 and hence the teager energy.

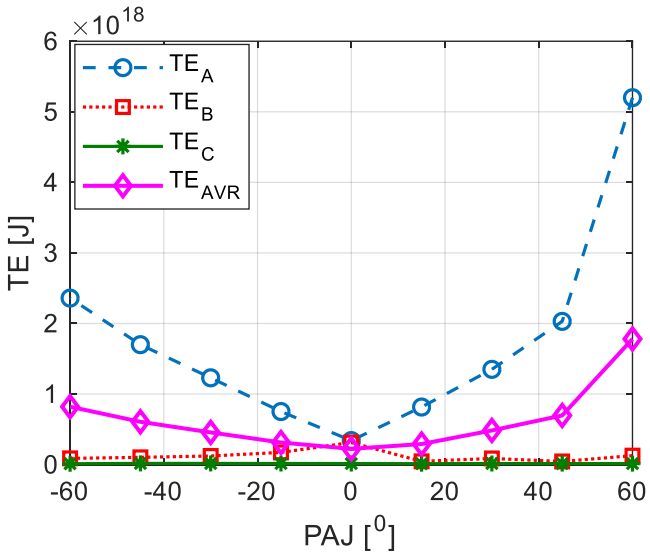


Figure 2.6 Variation of teager energy of IMF-1 with respect to different PAJ with 80% sag depth of the voltage during the grid fault.

c) Teager Energy of 7-types of Faults

The proposed Teager-Huang based teager energy is calculated for the standard seven types of power system faults [68]. In these faults, both unbalances in the voltage magnitude and PAJ are considered. The scenarios studied for all the seven types of faults to calculate the teager energy for IMF-1 are provided in TABLE 2.3. '*d*' is referred as the voltage sag depth and 'θ' is referred as the PAJ associated with the voltage sag during a specific fault.

TABLE 2.3: TEAGER ENERGY OF IMF-1 FOR DIFFERENT TYPES OF FAULT

Fault Type	Sag Depth (d) (pu)			Phase-angle Jump (θ) (°)			Teager Energy of IMF-1 (TE) (J)			Average Teager Energy of IMF-1 (J)
	d_A	d_B	d_C	θ_A	θ_B	θ_C	TE_A	TE_B	TE_c	TE_{AVR}
TYPE - A	0.65	0.65	0.65	-45°	-45°	-45°	3.43e17	6.73e16	7.25e16	1.60e17
TYPE - B	0.65	0	0	-45°	0°	0°	3.43e17	2.89e15	7.15e15	1.17e17
TYPE - C	0	0.3	0.6	0°	-35°	11°	5.81e14	4.09e14	4.94e15	1.97e15
TYPE - D	0.6	0.22	0.02	-30°	17°	-20°	1.17e17	7.19e16	8.78e15	6.58e16
TYPE - E	0	0.65	0.65	-40°	3°	-25°	7.15e15	6.31e16	8.56e15	2.62e16
TYPE - F	0.6	0.5	0. 2	-40°	3°	-25°	2.22e17	5.79e16	1.38e16	9.79e16
TYPE - G	0.25	0.45	0.65	-4°	-40°	15°	5.07e15	6.11e15	7.15e15	6.11e15

**Type-A: Three-phase fault, Type-B: Single-phase to ground fault, Type-C and Type-D: Phase to Phase fault, Type-E, Type-F and Type-G: Phase to Phase to Ground fault.

Figure 2.7 shows the relationship of teager energies for various faults. It is observed that the three-phase faults considered as Type-A faults provide the highest average teager energy value which is 1.6×10^{17}J. Thus, Type-A faults are considered as the most severe and less frequent grid fault. Type-B faults give the average teager energy value of 1.17×10^{17}J which is lesser than that of Type-A faults. Similarly, Type-C and Type-D have average teager energy of Type-D fault (6.58×10^{16}J) is observed to be higher than Type-C fault (1.97×10^{15}J). Occurrence of Type-E faults is quite rare as compared to Type-F and Type-G and gives average teager energy of 2.62×10^{16}J. Among the Type-F and Type-G faults, the former has more average teager energy value (9.79×10^{16}J) than the latter case (6.11×10^{15}J).

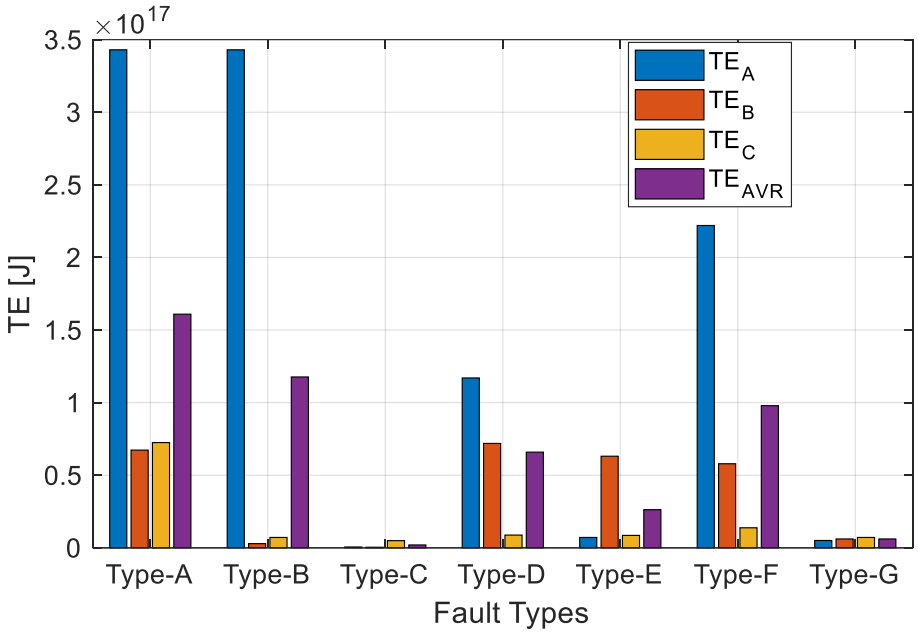


Figure 2.7 Variation of teager energy of IMF-1 with respect 7-types of faults.

Higher teager energy refers to the abrupt changes in either the estimated amplitude or the frequency during the grid faults. Higher value of teager energy in case of PAJ for a particular phase (either a, or b, or c) reveals that it affects the frequency of that particular phase more severely as compared to faults with only voltage sag. A converter that is connected with the grid uses the grid voltage frequency or phase-angle for control purposes. Hence, with the higher teager energy based grid fault, for instance the three-phase fault, there may be chances of large

amount of current flow through the converter which leads to its tripping. Thus, adequate current control action is necessary in case of PAJ related grid fault. This will be discussed later in this thesis.

2.5 Chapter Summary

This chapter contributes to the thesis in two ways as:

1) It discusses the advantages/disadvantages of various digital signal processing (DSP) techniques used for fault detection in both the conventional power system and modern power electronics-based power system.
2) It proposes a novel hybrid fault detection technique for grid-connected power converters.

The overview of the DSP techniques is provided under three categories: a) Frequency domain techniques, b) Time-frequency domain techniques, and c) Hybrid techniques. In line with the hybrid technique concept, the combination of Hilbert-Huang Transform (HHT) and Teager Energy Operator (TEO) to calculate the fault energy and hence to detect the fault, is proposed. This technique extracts the 1st intrinsic mode function (IMF-1) of the faulty voltage signal by the use of empirical mode decomposition (EMD) under the HHT principle. Then the instantaneous amplitude and frequency of the IMF-1 is used to calculate the teager energy using the TEO principle. The proposed technique is used to detect several voltage sags and PAJs during a grid fault. It is revealed that the addition of PAJ to the voltage sag increases the teager energy content in the faulty signal. Finally, the energies for the standard seven types of power system faults in which both the unbalances in the voltage magnitude and phase-angle in a three-phase system are estimated.

Chapter 3

Grid Synchronization Issues During Faults

Provision of fault ride-through capability during grid fault is a stringent grid code requirement for the power electronic converters during the grid integration of renewable energy sources. The grid-connected and grid following converters mostly use the conventional second-order synchronous reference frame phase-locked loop (SRFPLL) for grid synchronization. Loss of synchronization (LOS) with the grid is a common problem witnessed by the SRFPLL synchronized converters during severe grid fault. In this chapter, the cause of LOS with the conventional SRFPLL is explained as due to either large-signal or small-signal instability. LOS as a result of large-signal instability mainly occurs due to the violation of steady-state network constraints. On the other hand, even if the large-signal stability is ensured during fault, small-signal instability due to the inaccurate PLL parameter tuning can lead to LOS. The discrepancy of the approximated small-signal model of the SRFPLL that ignores the grid impedance is reported in this Chapter and on top of this, the parametric effect on the actual small-signal model of the SRFPLL is detailed. The considered parameters include the grid impedance magnitude/angle, fault current magnitude/angle, and phase-angle jumps during grid fault. This chapter identifies the occurrence of large phase-angle jumps (PAJs) during grid faults as a potential factor to trigger small-signal instability

for SRFPLL. The stability aspects relating to LOS are analysed during the occurrence of both symmetrical and asymmetrical grid faults.

3.1 Introduction

The unprecedented availability of various renewable energy resources such as solar and wind energy systems, have accelerated their deployment, as fossil fuel free electric power generations. Power electronic converters are the key interfacing unit for the grid integration of such renewables. These converters use complex and advanced control systems to deal with the renewable based source side intermittency. On the other hand, due to less inertia or being inertia-less, such converters are vulnerable to the grid side transients; for instance grid faults. The transmission system operator (TSO) and distribution system operator (DSO) of any country enforce several grid code requirements for these converters. Out of them, one of the stringent requirements is the provision of fault ride-through (FRT) capability.

These grid-connected power converters use the conventional synchronous reference frame phase-locked loop (SRFPLL) technique for grid synchronization due to its simple control architecture [30]. During the occurrence of any severe grid fault, the SRFPLL synchronized power converters face loss of synchronization (LOS) issue as reported in many real scenarios [87]-[90]. The LOS during the fault is triggered either due to the large-signal instability or small-signal instability of the SRFPLL control structure. The gain parameter design of the conventional SRFPLL is generally done keeping in mind the normal grid operating conditions. However such gain tuning provides insufficient damping and high settling time for the converters to provide FRT during severe faults. The damping factor can be enhanced to avoid LOS at the cost of inaccurate grid synchronization. Similarly lowering the settling time of the SRFPLL can provide faster FRT for the converters. However by doing so, the stability margin of the SRFPLL control structure will be at risk.

3.1.1 Contribution and Organization of this Chapter

During the grid fault as a result of LOS the power converters fail to provide FRT capability and hence the grid code requirement. The topic of LOS with SRFPLL grid synchronized power converter is explored in this chapter. The sub-section 3.2 provides a fault model of a grid-connected power converter that conveys the possibility of the occurrence of PAJs in addition to voltage sags during a grid fault. This PAJ is highly dependent on the electrical distance between the converter's connection point (PCC) and the grid point where the fault occurs. Sub-section 3.3 provides an overview of the modelling of the conventional SRFPLL that is used as a common unit for closed-loop grid synchronization either by three-phase or single-phase converters. The dependency of the gain parameter tuning on the damping factor, settling time and bandwidth are studied. Sub-section 3.4 discusses the possibility of the occurrence of LOS as a result of either large-signal or small-signal instability during both symmetrical and asymmetrical grid faults. While considering the LOS, the contribution of the grid impedance is also studied. Finally sub-section 3.5 summarizes the conclusion drawn from this chapter.

3.2 Fault Model of Grid-connected Power Converter

3.2.1 Fault Model during Symmetrical Fault

The single line diagram of a grid-connected three-phase voltage source converter (VSC) during a fault is shown in Figure 3.1. V_{PCC} and θ_{PCC} are the voltage magnitude and phase angle at the PCC, V_F and θ_F are the voltage magnitude and phase angle at the fault point and V_{th} and θ_{th} are the Thevenin equivalent voltage magnitude and angle of the grid. The line impedance connecting the PCC and the fault point is represented by $Z_l = R_l + j\omega L_l$. The fault impedance is represented by $Z_F = R_f + j\omega L_f$. The considered fault type is a voltage sag. Also due to the nature of the equivalent impedance (combination of grid and fault) at the fault point, a phase-angle jump (PAJ) is also associated with the voltage sag magnitude. The short circuit fault can be associated with different grounding scenarios (different Z_f).

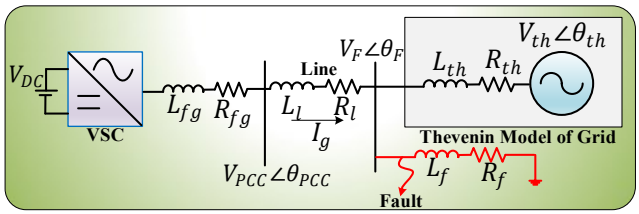


Figure 3.1: Single line diagram of the fault model of the grid connected VSC.

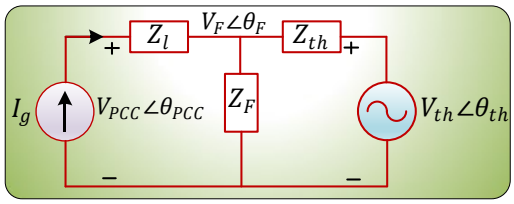


Figure 3.2: Norton equivalent model of grid-connected VSC during symmetrical fault.

The voltage sag magnitude $|(V_F)|$ and the PAJ $|(\theta_F)|$ at the fault point can be expressed in terms of the equivalent Thevenin impedance from the grid side and impedance provided due to different grounding types of the fault as given by

$$|V_F| = \frac{\sqrt{{R_f}^2 + (\omega L_f)^2}}{\sqrt{(R_f + R_{th})^2 + (\omega(L_f + L_{th}))^2}} |V_{th}| \tag{3.1}$$

$$|\theta_F| = \tan^{-1}\frac{\omega L_f}{R_f} - \tan^{-1}\frac{\omega(L_f + L_{th})}{R_f + R_{th}} \tag{3.2}$$

3.2.2 Fault Model during Asymmetrical Fault

In contrast to the symmetrical fault, the converter model during asymmetrical fault can be represented based on the sequence network decomposition such as positive, negative and zero sequences. The asymmetrical faults can be single-line to ground (SLG), double-line to ground (DLG) and line-line (LL) fault. The sequence decomposed networks for each of these faults are given in Figure 3.3, Figure 3.4 and Figure 3.5 respectively. It should be noted that LL fault do not allow the flow of zero sequence current component.

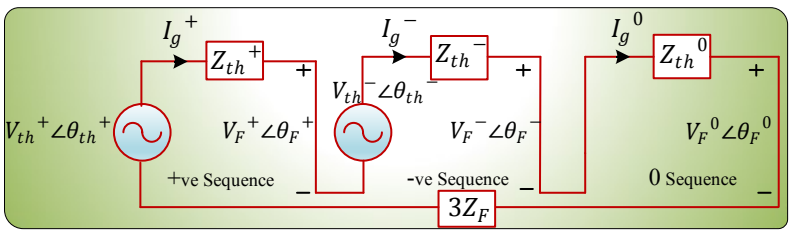


Figure 3.3: Norton equivalent model of grid-connected VSC during SLG fault.

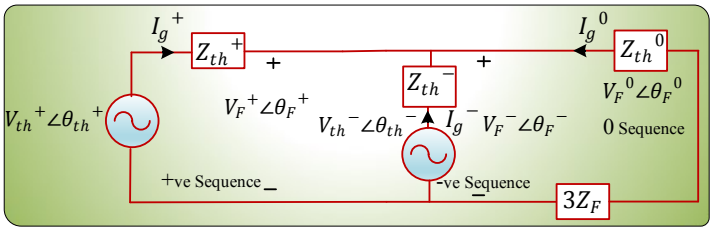


Figure 3.4: Norton equivalent model of grid-connected VSC during DLG fault.

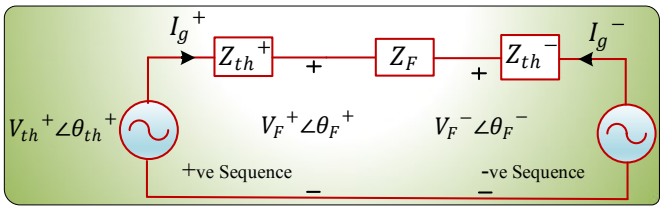


Figure 3.5: Norton equivalent model of grid-connected VSC during LL fault.

The expressions for the magnitude of positive (V_F^+), negative (V_F^-) and zero sequence (V_F^0) components measured at the fault point for all the three asymmetrical faults (SLG, DLG, and LL) are given by

$$V_F^+ = V_{th}^+ - \frac{Z_{th}^+(V_{th}^+ + V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_{th}^0 + 3Z_F} \tag{3.3a}$$

$$V_F^- = V_{th}^+ - \frac{Z_{th}^-(V_{th}^+ + V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_{th}^0 + 3Z_F} \tag{3.3b}$$

$$V_F^0 = \frac{Z_{th}^0(V_{th}^+ + V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_{th}^0 + 3Z_F} \tag{3.3c}$$

$$V_F^+ = \frac{(V_{th}^+ Z_{th}^- + V_{th}^- Z_{th}^+)(Z_{th}^0 + 3Z_F)}{Z_{th}^+ Z_{th}^- + Z_{th}^+ Z_{th}^0 + Z_{th}^- Z_{th}^0 + 3Z_F(Z_{th}^+ + Z_{th}^-)} \tag{3.4a}$$

$$V_F^- = \frac{(V_{th}^+ Z_{th}^- + V_{th}^- Z_{th}^+)(Z_{th}^0 + 3Z_F)}{Z_{th}^+ Z_{th}^- + Z_{th}^+ Z_{th}^0 + Z_{th}^- Z_{th}^0 + 3Z_F(Z_{th}^+ + Z_{th}^-)} \tag{3.4b}$$

$$V_F^0 = \frac{Z_{th}^0}{Z_{th}^0 + 3Z_F} V_F^+ \tag{3.4c}$$

$$V_F^+ = V_{th}^+ - \frac{Z_{th}^+(V_{th}^+ - V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_F} \tag{3.5a}$$

$$V_F^- = V_{th}^- - \frac{Z_{th}^-(V_{th}^+ - V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_F} \tag{3.5b}$$

$$V_F^0 = 0 \tag{3.5c}$$

In (3.4), (3.5) and (3.6), the Thevenin theorem is implemented to find out the positive, negative and zero sequence thevenin voltages (V_{th}^{+}, V_{th}^{-}, V_{th}^{0}) and the corresponding positive, negative and zero sequence thevenin impedances (Z_{th}^{+}, Z_{th}^{-}, Z_{th}^{0}). During the calculations, the power converter is replaced by a voltage dependent current- controlled source at the PCC point. The PAJs seen at the PCC in the corresponding sequence network will be the combined effect of the fault impedance and thevenin equivalent impedances.

As pointed out earlier, the power electronic converter requires a grid synchronization unit along with the voltage sequence component extractor to estimate the phase-angle for the current controller. The current controller can be implemented either in the synchronous or stationary reference frame during the fault, which will be discussed in the Chapter 5. The conventional synchronous reference frame phase-locked loop (SRFPLL) along with a pre-filter is used for grid synchronization during such unbalanced grid voltages for asymmetrical grid faults. In this thesis work, during fault, the emphasis is on the positive sequence component (voltage and current) based control only.

3.3 Design of SRFPLL for Grid Synchronization

Accurate and faster grid parameter estimation is essential for grid-connected power converters. This is mainly done by the grid synchronization unit which can be implemented as closed-loop or open-loop structure. Accordingly, different types of grid synchronization techniques have been discussed in Chapter-1. The most widely used technique for closed loop grid synchronization is the phase-locked loop (PLL). Grid-connected converters use the phase-angle estimation by the PLL to control the grid current in the synchronous reference frame (*dq*-frame) using the PI controller. Grid synchronization using PLL requires the grid voltage in natural frame (*abc*-frame) to be transferred to the *dq*-frame as it uses the *q*-axis of

the voltage to estimate frequency and phase-angle. Accordingly, it is named as "synchronous reference frame phase-locked loop (SRFPLL)". The basic structure of a three-phase grid voltage (measured at the PCC (V_{PCC})) synchronization using the SRFPLL is shown in Figure 3.6. This assumes a balanced three-phase voltage. In contrast, during unbalanced grid voltage (e.g. asymmetrical grid faults), SRFPLL deploys a positive sequence extractor as a pre-filter to eliminate the double-frequency ripples. The extended SRFPLL based grid synchronization in such cases is presented in Figure 3.7. The pre-filter can be implemented using various advanced digital filters [31]-[37]. In this work, positive sequence grid voltage extraction using the dual second-order generalized integrator (DSOGI) is used to maintain a trade-off between accurate grid synchronization and harmonic rejection capability [37]. The control structure and implementation details are explained in Chapter-4. It is worth noting that such pre-filters need to be tuned with the grid voltage estimated frequency.

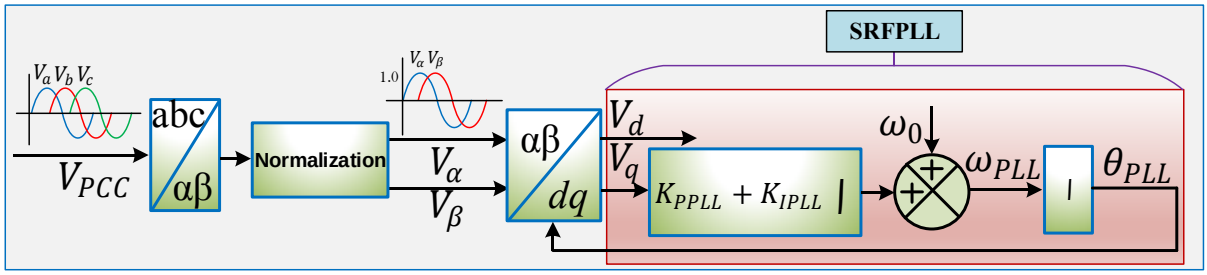


Figure 3.6: Three-phase grid synchronization using SRFPLL.

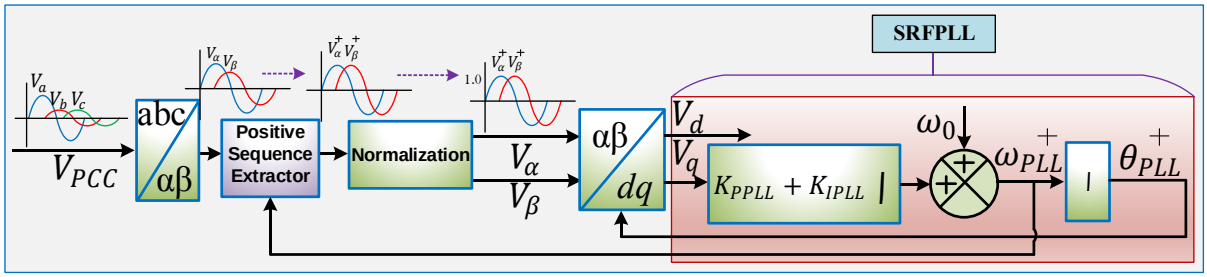


Figure 3.7: Three-phase grid synchronization using DSOGI+SRFPLL.

For DSOGI, the frequency feedback is provided by the SRFPLL estimation in order to avoid any phase-angle offset during off-nominal grid frequency variations. However, this frequency feedback strategy degrades the grid synchronization dynamics of DSOGI phase-locked loop (DSOGIPLL) which is essential from the converter's controller point of view for instance, FRT response. This aspect will be discussed in the subsequent chapters.

SRFPLL is also used for the single-phase grid synchronization as shown in Figure 3.8. Unlike three-phase, single-phase grid voltage requires an extra quadrature signal generator (QSG) to generate the three-phase equivalent in-phase (V_α) and in-quadrature (V_β) components. The V_α and V_β are then frame transferred to *dq*-frame. After this, the synchronization is similar to that of three-phase system. The QSG used in this work is second-order generalized integrator (SOGI). Implementation of SOGI will be detailed in Chapter-4.

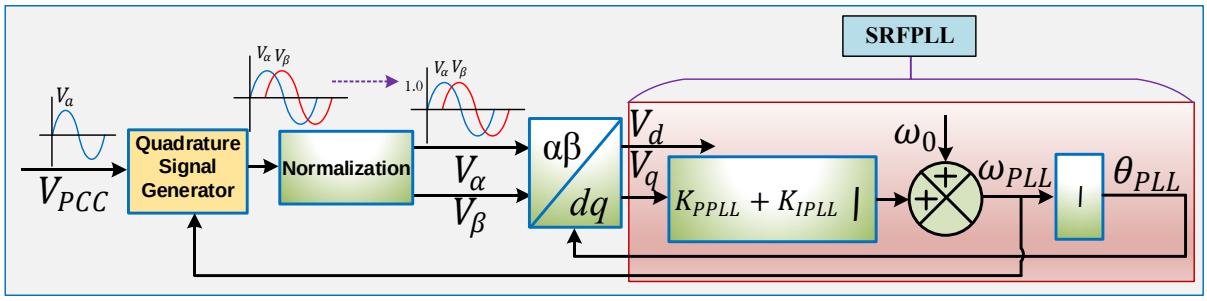


Figure 3.8: Single-phase grid synchronization using SOGI+SRFPLL.

As it can be seen from the above figures, whether it is three-phase or single-phase voltage, the common unit of the grid synchronization process is the SRFPLL that estimates the frequency and phase-angle to be used for frame transformation and/or control purpose.

The basic structure of the SRFPLL unit during the phase-angle locking is given in the Figure 3.9. It uses a PI controller whose input signal is V_q. The PI gains (K_{PPLL} and K_{IPLL}) are the designed parameters that decide the estimation dynamics of the frequency and phase-angle. The output of the PI controller is considered as the frequency estimation error and is added to

the nominal grid voltage frequency ($\omega_0 = \omega_g$) to provide the estimated frequency by the SRFPLL. The integration of the estimated frequency provides the estimated phase-angle (θ_{PLL}) of the grid voltage measured at the PCC (V_{PCC}). It should be noted that in Figure 3.9, the PCC and the grid are assumed to be same (i.e. the grid impedance is ignored). While designing the PI gain parameters, the closed-loop control structure provided in Figure 3.9 is linearized around the initial grid voltage phase-angle (i.e. $\theta_g = 0$). The grid voltage magnitude is assumed to be normalized (i.e. $|V_g| = 1.0$ pu). With this assumption, V_q can be expressed as (3.6). For small angle deviation around the initial grid voltage phase-angle, sine of the phase-angle error is approximated to the absolute value of the phase-angle. This makes the control loop a typical second-order control system whose transfer function relating θ_{PLL} to θ_g can be given by

$$V_q = \sin(\theta_g - \theta_{PLL}) = \sin(\theta_e) \approx \theta_e \tag{3.6}$$

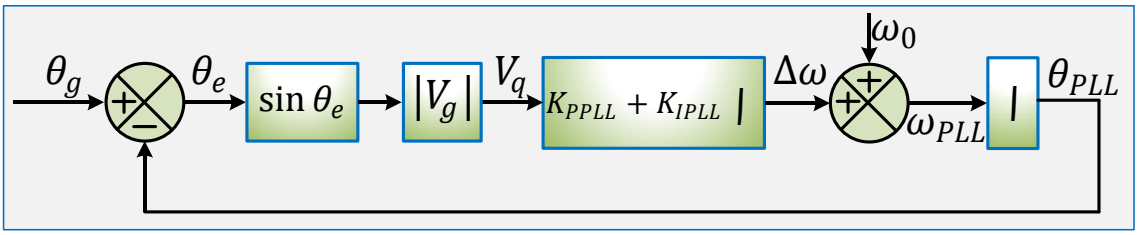


Figure 3.9: Basic control structure of SRFPLL.

$$\frac{\theta_{PLL}}{\theta_g} = \frac{K_{PPLL}s + (K_{IPLL} = \frac{K_{PPLL}}{T_i})}{s^2 + K_{PPLL}s + (K_{IPLL} = \frac{K_{PPLL}}{T_i})} \tag{3.7}$$

Equation (3.7) can also be presented as

$$\frac{\theta_{PLL}}{\theta_g} = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \tag{3.8}$$

Using (3.7) and (3.8), the relationship among the gain parameters (K_{PPLL} and K_{IPLL}), the natural frequency (ω_n) and damping factor (ζ) can be given as

$$\omega_n = \frac{K_{PPLL}}{T_i}, \qquad \zeta = \frac{\sqrt{K_{PPLL}T_i}}{2} \tag{3.9}$$

Linear control system analysis states that the second-order system takes four times the time constant ($4\tau = 4/(\zeta\omega_n)$) to reach 1% of steady-state error. Viewing (3.7) from this settling time (t_s) aspect, the relationship between the PLL gains (K_{PPLL} and K_{IPLL}) and (t_s) can be given by

$$K_{PPLL} = 2\zeta\omega_n = \frac{9.2}{t_s}, \qquad T_i = \frac{2\zeta}{\omega_n} = \frac{t_s\zeta^2}{2.3} \tag{3.10}$$

One important point to be noted here is that the tuning of the K_{PPLL} and K_{IPLL} as per (3.10) is valid provided the grid voltage is normalized. The normalization is done adaptively in the $\alpha\beta$-frame as

$$V_{\alpha\beta(pu)} = \frac{V_{\alpha\beta}}{\sqrt{{V_\alpha}^2 + {V_\beta}^2}} \tag{3.11}$$

Usually, the value of ζ in (3.8) is chosen to be 0.707 to provide a critically damped response during the grid synchronization using SRFPLL [38]. Similarly, t_s is selected based on the application. It can be varied from two fundamental (40 ms) to six fundamental time periods (120 ms). As per (3.10), lower settling time with fixed ζ provides higher natural frequency (ω_n) and poor harmonic rejection capability. On the other hand, higher settling time improves

the harmonic rejection capability at the cost of degrading the dynamics response. This is one of the limitations of the SRFPLL based grid synchronization technique.

The dependency while tuning K_{PPLL} and K_{IPLL} based on either the set values of (ζ, t_s) or (ζ, ω_n) is shown in Figure 3.10 and Figure 3.11 respectively. For the first set of test ζ is varied from 0.3 to 1.5 and t_s is varied from 40 ms to 150 ms. For the second set of test, ζ is varied from 0.3 to 1.5 and ω_n is varied from 1256 rad/s (200Hz) to 31.41 rad/s (5 Hz). It is observed from Figure 3.10 that the K_{PPLL} increases sharply as t_s decreases towards 2-3 fundamental period (40-60 ms) and is independent of the ζ which follows the relationship as given by (3.10). However, K_{IPLL} is observed to be affected both by ζ and t_s as it follows an inverse relationship to the square of the multiplication of both these factors (refer (3.7)). The rate of increase is much higher at lower values of ζ and t_s. This reveals the fact that to achieve faster grid synchronization (lower t_s/higher K_{PPLL}), K_{IPLL} needs to be returned to offer sufficient damping during any grid voltage disturbances (transients).

In contrast, if K_{PPLL} and K_{IPLL} are designed according to ω_n (or f_n) as shown in Figure 3.11, it can be observed that for a fixed ζ, higher value K_{PPLL} provides a wider bandwidth and hence will degrade the harmonic rejection capability of the SRFPLL loop filtering though it will result in faster grid synchronization. On the other hand, K_{IPLL} is observed to follow a square relationship with ω_n i.e. setting K_{IPLL} to a lower value will result in higher harmonic rejection performance by SRFPLL.

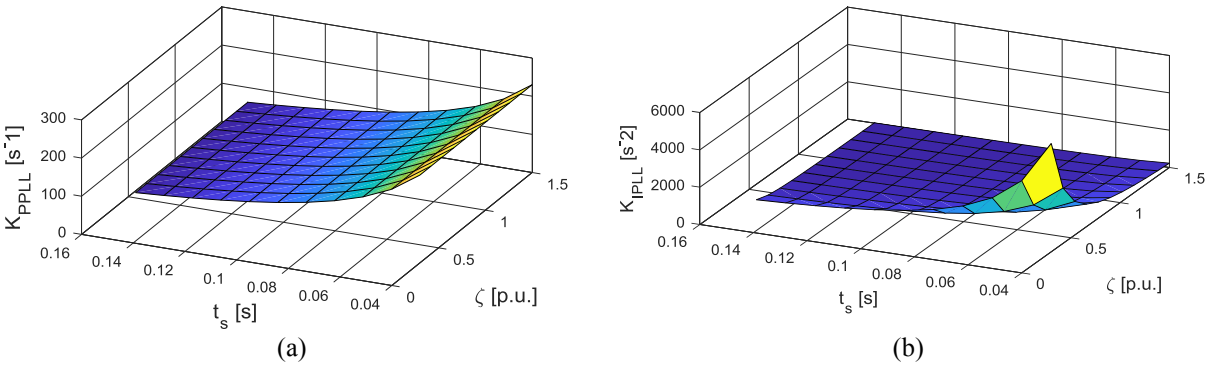


Figure 3.10: Variations of (a) K_{PPLL} and (b) K_{IPLL} with respect to ζ and t_s

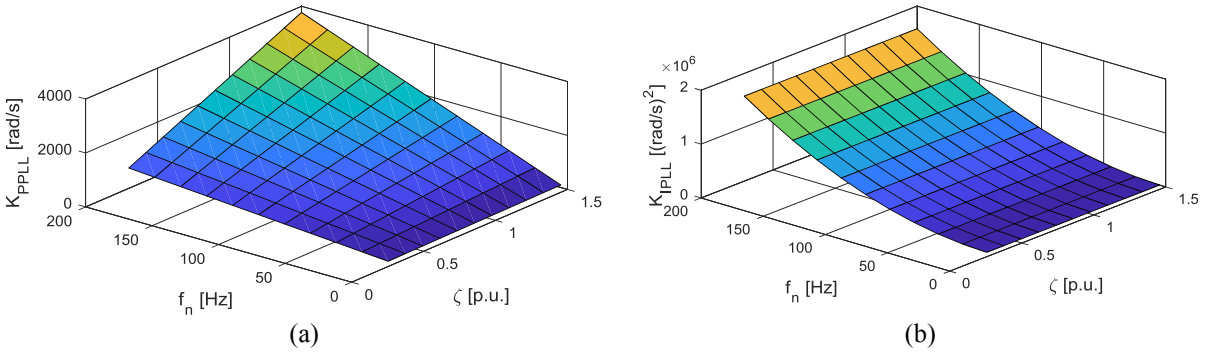


Figure 3.11: Variations of (a) K_{PPLL} and (b) K_{IPLL} with respect to ζ and f_n

The modelling of SRFPLL and its gain parameter tuning discussed above face discrepancies during the grid voltage transients. Moreover in a weak grid where the grid impedance value is of significant magnitude, the PCC point and the grid point cannot be assumed to be same as considered above for PLL modelling. Additionally, during grid faults (either severe symmetrical or asymmetrical), voltage observed at the PCC point experience phase-angle jumps (PAJs) in addition to voltage sags [68]. In such scenarios, the assumption made in (3.6) will lead to erroneous phase-angle estimation by SRFPLL which will have adverse impact on the current controller of synchronized power converters. To avoid this issue with the conventional linearized model of SRFPLL modelling, understanding of an accurate model of the SRFPLL considering the grid interaction of synchronized power converter is needed and explained in the following sub-sections.

3.4 Loss of Grid Synchronization Issue with SRFPLL during Faults

Loss of grid synchronization (LOS) phenomena mainly occurs in case of grid-connected converter during the occurrence of severe symmetrical or asymmetrical faults. During this, the frequency estimated by the SRFPLL sharply deviates from the nominal value and becomes uncontrolled. This results in erroneous phase-angle estimation by SRFPLL, by virtue of which the converter experiences uncontrolled current flow. The root causes of LOS during faults are: i) very low voltage magnitude, ii) high grid impedance or iii) high amount of current injection (active/reactive). From the stability point of view LOS event can be explained as 1) Large-signal instability and 2) Small-signal instability [40]-[66]. For the understanding of both types of stability, quasi-static model of the SRFPLL is considered where the grid interaction of power converter is represented by the grid impedance [40], [41].

3.4.1 Large-signal Stability Analysis

The quasi-static model used for the explanation of large-signal stability analysis is shown in Figure 3.12. It can be seen that unlike the conventional SRFPLL model, in this case the input to the PLL loop (V_q) consists of two components as given by

$$V_q = V_{qn} + V_{qp} \tag{3.12}$$

where first term is called the grid synchronization term (V_{qn}) and it acts as negative feedback to the SRFPLL similar to the conventional PLL design discussed above. The second term is known as the self-synchronization term (V_{qp}) which is a positive feedback to the SRFPLL control loop. To maintain the large-signal stability during the occurrence of any grid fault, the condition to be fulfilled is given by

$$|V_{qn}| > |V_{qp}| \tag{3.13}$$

$$|V_g \sin\theta_e| > |I_g Z_g \sin(\theta_I + \theta_Z)| \tag{3.14}$$

The steady-state current limit to avoid LOS due to large signal instability thus can be expressed by

$$|I_g| < \frac{|V_g \sin\theta_e|}{Z_g \sin(\theta_I + \theta_Z)} \tag{3.15}$$

Equation (3.15) can be correlated with the fault variables during the fault discussed in sub-section 3.2, where $|V_g|$ is the amount of fault magnitude at the grid side ($|V_F|$), θ_e is the amount of PAJ during the grid fault (θ_F), Z_g is the equivalent impedance seen at the PCC, θ_Z is the impedance angle, θ_I is the injected current vector angle and $|I_g|$ is magnitude of injected current. The maximum current limit for large signal stability limit is derived considering the PAJ to be $\pm$ 90° as given by

$$|I_{gmax}| < \frac{|V_g|}{Z_g \sin(\theta_I + \theta_Z)} \; @\theta_e = \pm 90° \tag{3.16}$$

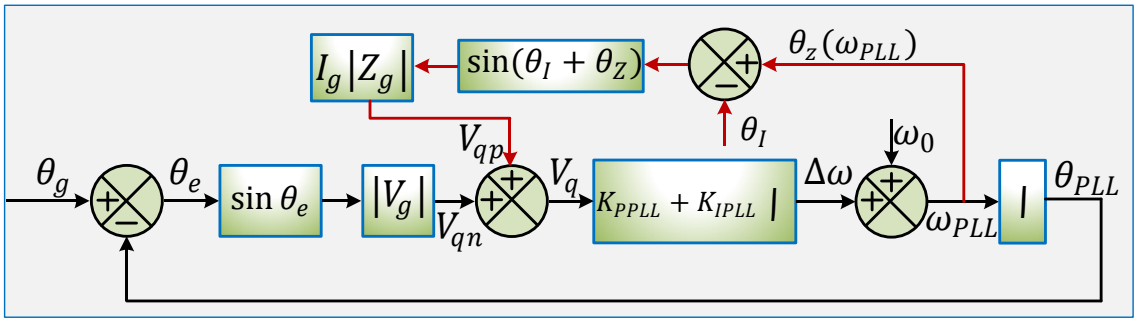


Figure 3.12: Quasi-static model of SRFPLL.

Also, the current limit value depends on the type of current injection (θ_I), and/or type of grid impedance (θ_Z) for the same amount fault voltage magnitude. A graphical illustration of the current injection limit is shown in Figure 3.13. Point A refers to the general case that determines the steady-state current injection limit. Two other points A1 and A2 are also shown in the Figure 3.13. This operating point A2 is derived by assuming a pure reactive (1.0 pu) and zero active current injection i.e. θ_I = -90°. This makes (3.16) dependent on the resistance value of the grid impedance (R_g) in addition to the fault magnitude. Similarly point A1 refers to pure active (1.0 pu) and zero reactive current injection i.e. θ_I = 0°. In this case, the current injection depends on the inductive part of grid impedance (X_g). It can be observed that point A1 lies over A2 by considering the line impedance to be resistive ($R_g > X_g$). If the grid impedance is more inductive, point A1 will appear below A2. The exceptional case can be derived from (3.16) as an infinite amount of current injection is possible without affecting the large-signal stability. This will happen when the injected current vector aligns with that of the grid impedance vector i.e., $\theta_I = \theta_Z$.

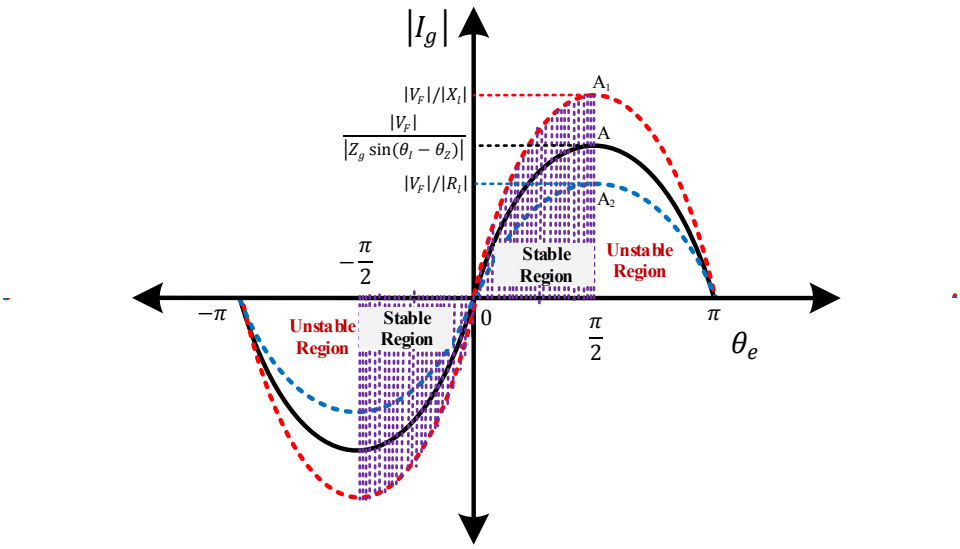


Figure 3.13: Graphical representation of the steady-state limit for current injection during fault.

Let us now examine the occurrence of LOS due to the violation of steady-state current limit during two events: a) severe symmetrical grid fault and pure reactive current injection and b) asymmetrical fault and pure reactive current injection.

a) *Event 1*: Severe symmetrical fault and pure reactive current injection ($|V_F|$ = 0.1 pu, θ_I = -90°, $I_{gmax} \cong 9.5\ A_p$ and R_g = 0.09 pu)

In Figure 3.14(a), the current injected is of purely lagging power factor with a magnitude of $8.65A_p$ that corresponds to 1.0 pu for a 2.2 kW three-phase inverter (considered in this work).

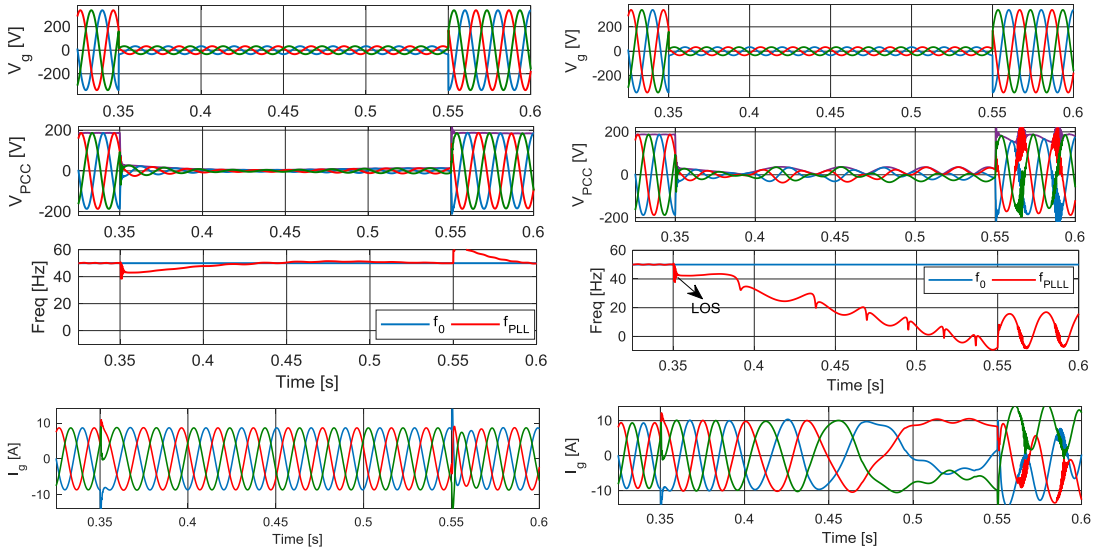


Figure 3.14: (a) No LOS at $I_g = 8.65A_p$ and (b) LOS at $I_g = 10A_p$ during 90% symmetrical sag and no PAJ.

It is observed that the frequency estimated by the SRFPLL is well maintained between 40 Hz lower bound and 70 Hz upper bound. The reactive current injected to the grid is noticed to be well synchronized both during fault inception at t = 0.35 s and recovery at t = 0.55 s. The maximum current injection limit is calculated to be $9.5A_p$ for this fault condition. On the other hand, in Figure 3.14(b), the peak of injected current is increased to $10A_p$. In this case, the frequency estimation by SRFPLL leads to LOS during the fault. Accordingly, the injected current experiences uncontrolled flow during the fault period. This is because of large-signal

instability based LOS caused by the violation of the steady-state current limit i.e. $10A_p > 9.5A_p$.

b) *Event 2*: Asymmetrical fault and pure reactive current injection ($|V_F^+| = 0.3$ pu, $\theta_I = -90°$, $I_{gmax}^+ \cong 9.5$ A_p and $R_g = 0.27$ pu)

In contrast to the severe symmetrical fault there are less chances of LOS occurrence during asymmetrical fault considering the same network resistance value. For instance, a two-phase to ground fault at the grid side is considered in this case where 100% sag is created in phase-B and phase-C. This generates 33% of positive sequence voltage magnitude. With a resistance value of 0.09 pu and current injection of $10A_p$ during fault, LOS does not occur. However, to show the LOS phenomenon, the grid resistance value is increased to 0.27 pu (considering the fault point is far away from PCC). When the value of grid resistance is set as 0.27 pu, no LOS is observed for positive sequence current injection of $8.65A_p$ as shown in Figure 3.15(a), while the inverter experiences a LOS during the injection of $10A_p$ as seen in Figure 3.15(b). Thus, it can be concluded that LOS is more common to severe symmetrical fault while less for asymmetrical fault (can happen on special cases).

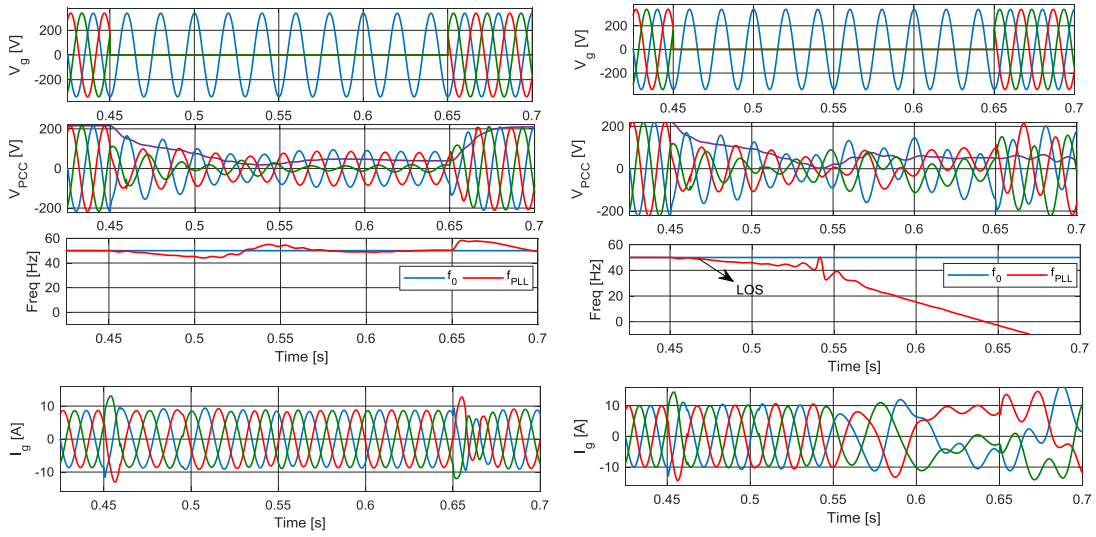


Figure 3.15: (a) No LOS at $I_g = 8.65A_p$ and (b) LOS at $I_g = 10A_p$ during 100% sag in phase-B and phase-C and no PAJ.

3.4.2 Small-signal Stability Analysis

Loss of synchronization can also occur due to small-signal instability of SRFPLL control loop. Even if the large-signal stability limit is met as discussed above, due to inaccurate PLL gain parameter tuning, the frequency estimated by PLL can go out of synchronism and thereby provide erroneous phase-angle estimation for the converter controller. To understand the mechanism of LOS due to small-signal instability, the accurate small-signal model of the SRFPLL considering the grid interaction of the converter is shown in Figure 3.16. The linearization is done around the grid operating frequency (i.e. $\omega_{PLL} = \omega_0$). It can be seen that there are three constants (K_1, K_2 and K_3) appearing in the positive feedback loop of the SRFPLL due to the grid interaction. The new transfer function relating the estimated phase-angle (θ_{PLL}) to the grid voltage (at the fault point) phase-angle (θ_g) is given by

$$\frac{\theta_{PLL}}{\theta_g} = \frac{(K_{PPLL}\cos\theta_e)s + (K_{IPLL}\cos\theta_e)}{s^2(1 - K_{PPLL}I_gK_3) + s(K_{PPLL}\cos\theta_e - K_{IPLL}I_gK_3) + (K_{IPLL}\cos\theta_e)} \tag{3.17}$$

where, $K_1 = \frac{{L_g}^2\omega_0}{|Z_g(\omega_0)|}$, $K_2 = \frac{R_gL_g}{|Z_g(\omega_0)|^2}$ and $K_3 = K_2\left|Z_g(\omega_0)\right| + K_1\sin(\theta_z(\omega_0) + \theta_I)$

It is to be noted that (3.17) is completely different from (3.7). Thus, the gains of PLL (K_{PPLL} and K_{IPLL}) are designed considering that (3.7) is no longer valid during the fault analysis. The expression for damping factor and settling time considering (3.17) is given by

$$\text{settling time: } t_s = \frac{9.2(1-K_{PPLL}I_gK_3)}{K_{PPLL}\cos\theta_e} \text{ and } \zeta = \frac{K_{PPLL}\cos\theta_e - K_{IPLL}I_gK_3}{2\sqrt{(1-K_{PPLL}I_gK_3)}\sqrt{K_{IPLL}\cos\theta_e}} \tag{3.18}$$

The main assumption that is made during the normal operating condition as given by (3.7) is invalid ($\cos\theta_e \approx 1$ and $\sin\theta_e \approx \theta_e$) for larger phase-angle error which will occur due to the PAJ during a grid fault. At higher PAJ, the damping factor decided by (3.8) is insufficient to avoid LOS. This necessitates a higher damping factor for PLL during the fault. Similarly, the higher

settling time value makes the PLL dynamics slower at higher PAJ and the converter current controller is highly affected to provide adequate FRT during fault.

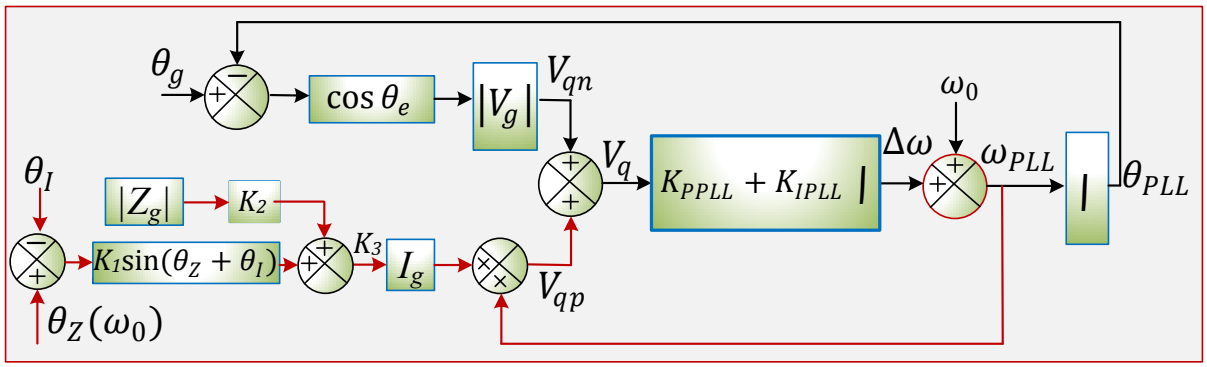


Figure 3.16: Small-signal model of SRFPLL considering the grid interaction of power converter.

A graphical presentation of the variations of damping factor (ζ) and settling time (t_s) considering a wide range of grid impedance angle (θ_Z varies from 0° to 90°) and phase-angle error due to various PAJs (θ_e varies from 0° to 60°) are provided in Figure 3.17(a) and Figure 3.17(b) respectively. It can be observed that conventional SRFPLL is designed considering the operating point marked in the figures (ζ = 0.707 and t_s = 120 ms assuming θ_e = 0° and θ_Z = 0° by ignoring the grid impedance). In Figure 3.17, a pure lagging power factor reactive current injection is considered. It can be seen that both ζ and t_s exhibit a highly non-linear characteristics for the accurate small-signal model of the SRFPLL, during grid interaction and PAJs. Thus, LOS occurs due to small-signal instability at higher PAJs during the grid fault or higher impedance angle at the PCC.

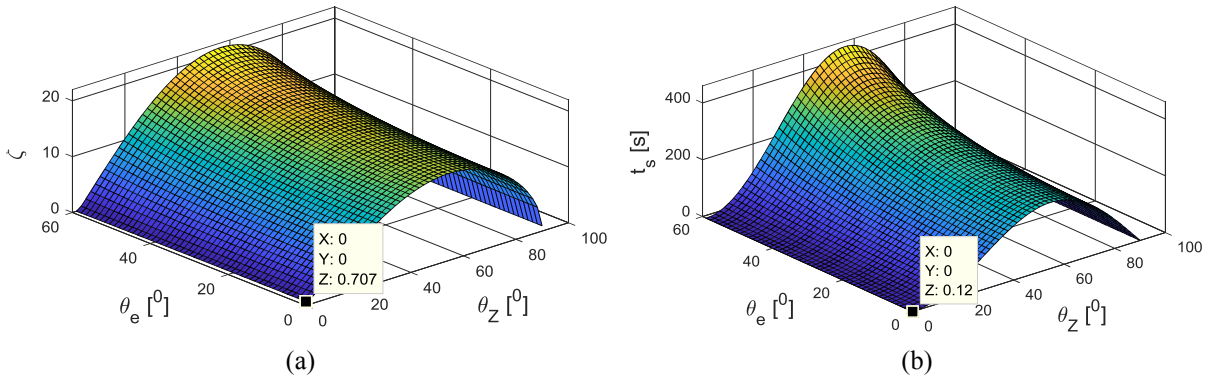


Figure 3.17: Variations of (a) ζ and (b) t_s with respect to θ_e and θ_Z.

The small-signal instability based loss of synchronism due to various PAJs at the grid voltage during grid fault can also be studied. The same test cases are analysed as done for large-signal stability study. However, in this case, it is ensured that the current injection meets the large-signal stability criteria. At first, during the severe symmetrical fault, the current injection is maintained at 8.65 A_p which is below the stability limit. At this stage PAJ of 0°, -5°, -30° and -45° are added to the fault.

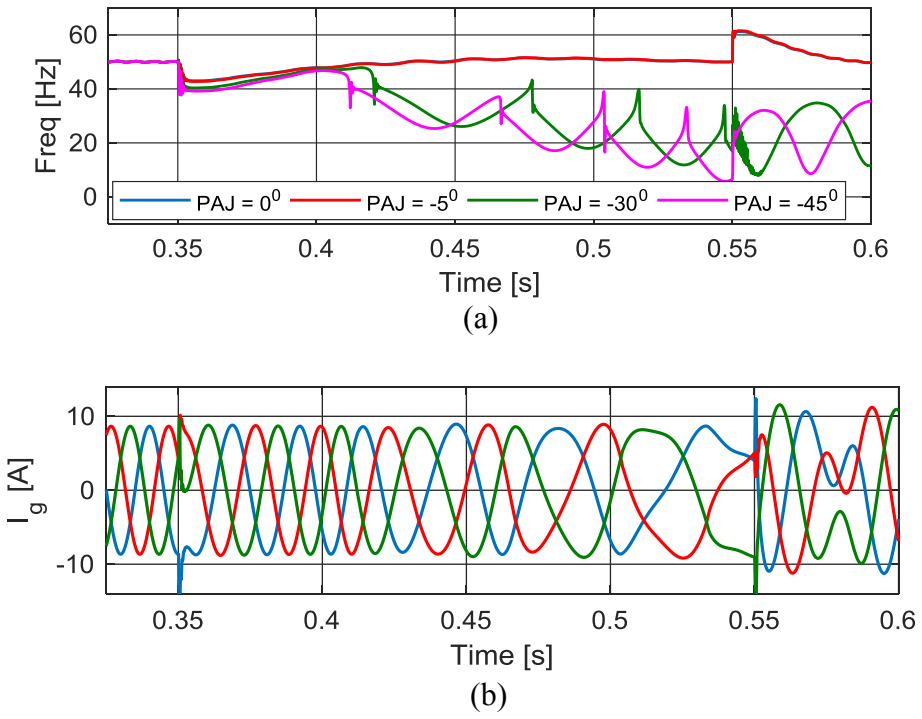


Figure 3.18: Variations of (a) Frequency w.r.t PAJ and (b) I_g at PAJ = -45° during 90% symmetrical fault with PAJ.

The frequency response of the SRFPLL estimation is shown in Figure 3.18(a). It is observed that with 0° and -5° PAJ, the frequency is restored during both fault inception and recovery time. However with -30° and -45°, the frequency seems to be uncontrolled during the fault period and even during the recovery. It is also noticed that with higher PAJ, the point of LOS appears earlier (i.e. for -45° LOS starts at t = 0.41 s while for -30° it occurs at t = 0.42 s). The converter current during the -45° PAJ is shown in Figure 3.18(b).

Similar to symmetrical fault, the LOS due to small-signal instability in case of asymmetrical faults having various PAJs are shown in Figure 3.19(a). In this case, the LOS is observed for -45° PAJ. The positive sequence grid current injection during the -45° PAJ is shown in Figure 3.19(b). It can be observed that though the peak current is maintained at $8.65A_p$ during the fault, the converter still experiences LOS due to the occurrence of PAJ which triggers the instability.

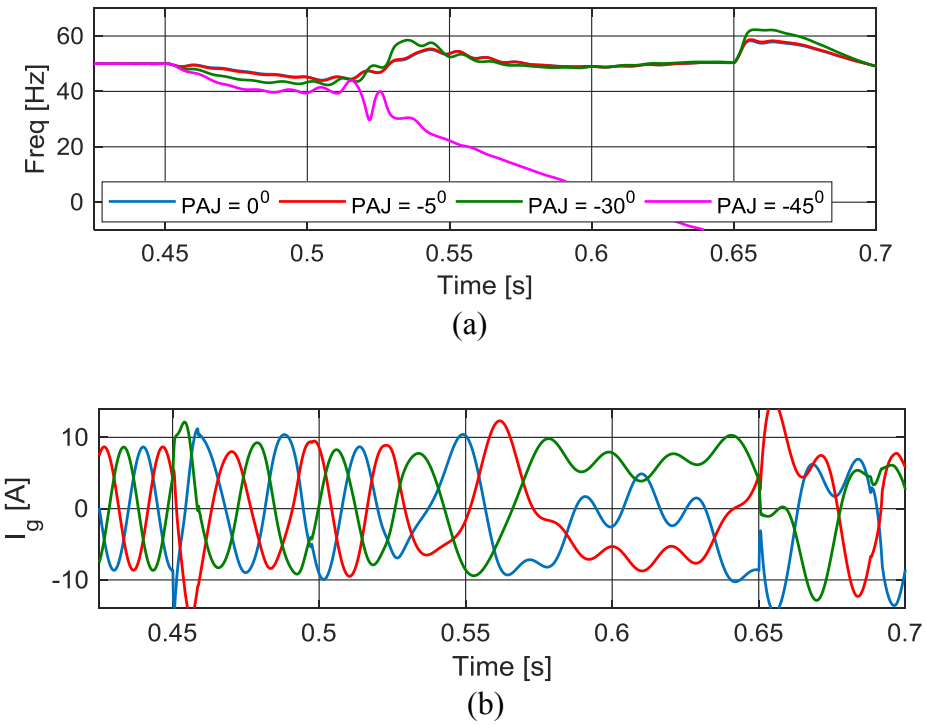


Figure 3.19: Variations of (a) Frequency w.r.t PAJ and (b) I_g at PAJ = -45° during 100% sag in phase-B and phase-C with PAJ.

As explained above, during LOS event, whether due to large-signal instability or small-signal instability, the estimated frequency is observed to deviate at a faster rate and move towards zero Hz or even negative value. In real cases, the frequency is not allowed to deviate so much even during normal operating conditions. Thus in the rest of the thesis, the estimated frequency by SRFPLL is band limited between 45 Hz to 55 Hz while carrying out the converter's FRT study during various grid faults with and without PAJs.

3.5 Chapter Summary

This chapter presents the theoretical discussion on the most underestimated synchronization issue with the conventional SRFPLL synchronized power converters during grid fault known as "loss of synchronization (LOS)". By providing the fault model of a grid-connected converter, the chapter details the chances of the occurrence of PAJ in addition to voltage sag during the fault. The PAJ observed at the PCC point, where the converter is connected to the grid, is dependent on type of grid impedance. The conventional SRFPLL modelling is presented where the contribution of grid impedance is neglected during the gain parameter tuning of the PLL. Additionally, the assumption of linearized phase-angle approximation as done in conventional SRFPLL is no longer valid for large PAJs as a result severe grid faults. Thus a more accurate model of the SRFPLL (quasi-static model) is used to study the possible causes of the occurrence of LOS. LOS can happen either due to the large-signal or small-signal instability experienced by the conventional SRFPLL grid synchronization. The large-signal instability occurs when the steady-state current injection limit during the fault is violated. On the other hand, the inaccurate gain parameter tuning of the SRFPLL can lead to small-signal instability based LOS. The expression for the required damping factor and settling time for the accurate small-signal quasi-static model of SRFPLL is provided which

depicts non-linear variations with respect to parameters such as grid impedance angle and PAJs. It is concluded that the damping factor and the settling time set for the conventional SRFPLL is insufficient to maintain synchronism at the occurrences of large PAJs during grid faults. Several test cases are presented to have a clear picture of the occurrences of LOS during both symmetrical and asymmetrical fault without and with PAJs, as the cause for large-signal and small-signal instability respectively.

The understanding of the LOS phenomena and its adverse impact on the converter's FRT capability necessitates the development of a robust adaptive grid synchronization technique. In the next chapter, the modifications done to the conventional SRFPLL during the fault to make it adaptive will be discussed with reference to the growing body of literatures. Additionally, a hybrid grid synchronization transition for power converters is proposed.

Chapter 4

Adaptive and Hybrid Grid Synchronization Techniques

This chapter initially provides a brief overview of the existing adaptive grid synchronization techniques for grid-connected power converters. The techniques are focused on modifying the conventional second-order SRFPLL synchronization technique in order to mitigate the loss of synchronization (LOS) issue discussed in Chapter-3. Understanding the limitation of the proposed techniques, a hybrid grid synchronization technique is proposed. It consists of a hybrid phase-angle estimation. It switches between the conventional SRFPLL to the arctangent phase-angle estimation during the grid fault having phase-angle jump (PAJ). A novel transition scheme is proposed for the smooth transfer between the two phase-angle estimators. Moreover, during asymmetrical fault with PAJ, an improved frequency-adaptive dual second order generalized integrator (DSOGI) based pre-filter is proposed which avoids the frequency feedback from SRFPLL.

The proposed hybrid grid synchronization concept is also explored for the single-phase grid synchronization (SOGIPLL in this thesis). With the proposed technique, SRFPLL independent frequency estimators are proposed to feed SOGI during fault. The phase-angle is estimated using the arctangent function on the SOGI outputs like three-phase systems.

The frequency transition between the SRFPLL estimated frequency and the proposed PLL free frequency estimators follows the same transition framework proposed for the phase-angle transitions. Finally a benchmark study is performed to compare the synchronization dynamics of the proposed hybrid grid synchronization with the existing techniques during several grid faults.

4.1 Introduction

The renewable energy sources based power generation use power electronic converters (inverters) for their grid integration. The intermittency during their power generation due to uncertainty in the climatic conditions poses several techno-economic challenges to the existing grid. Hence, the interfacing converters exploit complex control systems to deal with source-side dynamics. On the other hand, due to less inertia or inertia-less property, unlike conventional synchronous generators, these converters are more vulnerable towards the grid side transients: for instance grid faults. As per the requirement by the modern grid codes, during any fault occurrence, these converters should provide reactive power support to boost the grid voltage magnitude for a specified amount of time instead of instant tripping. This is known as fault ride-through (FRT) / low voltage ride-through (LVRT).

As mentioned in Chapter-1, the grid-connected converters operating in the grid following mode requires grid synchronization unit to inject current to the grid by maintaining high power quality. Several grid synchronization techniques have been provided by the researchers which are discussed in Chapter-3. Nevertheless, phase-locked loop (PLL) concept has been widely used by industries due to its simple implementation and robust performance during normal grid operating conditions [30], [131]. The converters use the frequency and phase-angle information estimated by PLL for their inner current control either in stationary or

synchronous reference coordinates. On the contrary, the PLL (conventional second-order) based grid synchronization suffers during severe grid faults having PAJs [132]. Due to insufficient damping and larger settling time, high PAJ during fault leads to LOS [58]. Moreover, during asymmetrical faults, several advanced digital filters have been proposed that are implemented along with SRFPLL to extract positive sequence components of the unbalanced three-phase voltage. The use of these advanced filters always undergoes a design trade-off between the grid synchronization dynamics and computational complexity. Out of several pre-filters, dual second-order generalized integrator (DSOGI) is mostly used due to its good harmonic rejection capability. The resonant frequencies of the two SOGI BPFs are usually tuned by the SRFPLL frequency estimations and the structure is called the DSOGIPLL. In the context of PAJ associated grid faults, the poor dynamics of the SRFPLL frequency estimation is reflected in the delayed estimation of sequence components using DSOGIPLL.

Single-phase grid synchronization technique is generally used by small power rated converters (less than 5 kW) for the grid integration of residential rooftop solar (PV) systems. In contrast to the three-phase grid synchronization, single-phase grid synchronization technique requires a quadrature signal generation (QSG). The purpose is to generate the equivalent in-phase (V_α) and in-quadrature components (V_β) of the grid voltage which are used to extract the phase-angle information. The QSG unit combined with PLL, functions as an equivalent three-phase system. Several attempts have been made to implement the QSG over the years. The first technique includes a transform delay which can provide a delay of one-fourth of fundamental period (5 ms) to the original signal to generate the quadrature signal [133]. Due to the delay effect, this technique is found to be inefficient during transients observed in the system. The idea of differentiating the original sinusoidal signal to get the quadrature component is provided in [134]. This technique adds the problem of noise due to

the differentiation process in the real time. Orthogonal signal generation using Hilbert transform technique [135] suffers from complexities like real-time implementation and computational burden.

QSG using second-order generalized integrator (SOGI) is developed in [136] and has gained much attention for real time application. The SOGI in combination with the synchronous reference frame phase-locked loop (SRFPLL) is called as SOGIPLL. It has been reported that SOGIPLL provides a good in-loop filtering to reject noise and harmonics in the grid voltage during synchronization [137]. SOGIPLL uses two feedback paths during grid synchronization. One is the estimated frequency which is fed to the SOGIQSG unit to generate the in-phase and in-quadrature components. The second one is the estimated phase-angle which is used for Park transformation ($\alpha\beta/dq$). The presence of these two feedback paths create interdependency between the estimated frequency and phase-angle by SOGIPLL. The interdependency functions well during normal grid operating conditions. However, during grid faults having voltage sag, and PAJ, SOGIPLL provides poor performance and unable to provide fast and accurate grid synchronization for single-phase grid-connected converters. Wrong estimation of grid parameters drives the current controller of the converters to unstable region during the fault and hence results in poor FRT behaviour. In addition to this, the PLL gains (similar to three-phase SRFPLL) of the SOGIPLL require adequate tuning to provide a good trade-off between fast (high bandwidth PLL) and robust (low bandwidth PLL and good harmonic rejection capability) grid synchronization.

In terms of control structure DSOGI pre-filter which is discussed previously for three-phase application, is the combination of two SOGI BPFs. Hence as per above discussions, poor frequency adaptability is the common issue for both SOGIPLL (for single-phase grid synchronization) or DSOGIPLL (for three-phase grid synchronization) during the PAJ related

grid faults. This will lead to poor grid synchronization performance that affects the FRT dynamics of grid-connected converters significantly.

4.1.1 Contribution and Organization of this Chapter

To avoid LOS issue with the conventional second-order SRFPLL during grid fault, four existing adaptive grid synchronization techniques are reviewed in Section 4.2. Their control structure and limitation in implementation are discussed. In Section 4.3, the structure of the proposed hybrid grid synchronization principle is presented. Section 4.3 is divided into two sub-sections to address the application of the hybrid grid synchronization in regards to three-phase and single-phase systems separately. Sub-section 4.3.1 explains the application for three-phase systems and 4.3.2 for single-phase systems. Both the three-phase and single-phase hybrid grid synchronization techniques consist of hybrid frequency and hybrid phase-angle estimators. The hybrid phase-angle estimator is common to both three-phase and single-phase systems. It estimates the phase-angle of the grid voltage measured at the point of common coupling (PCC) using arctangent function instead of SRFPLL estimation during PAJ associated with grid fault. On the contrary, hybrid frequency estimator uses the arctangent derived frequency to improve frequency adaptability of DSOGI pre-filter to extract positive sequence three-phase voltage components during asymmetrical faults.

The idea of the hybrid frequency estimator is also implemented in the single-phase system to feed the SRFPLL independent frequency estimation for SOGI. Three different frequency estimators are presented in this chapter such as: 1) arctangent derived (same as three-phase system), 2) Teager Energy Operator and, 3) Fixed Delay technique. The first one relies on the $\alpha\beta$-components of PCC voltage while the second and third method can estimate the frequency using either measured single-phase or α-component of the PCC voltage. A common transition technique for the above-mentioned hybrid phase-angle and hybrid frequency estimators is

proposed and presented in Section 4.4. Section 4.5 provides a benchmark study of the proposed hybrid grid synchronization with the existing technique during various grid fault scenarios. Benchmarking is done separately for three-phase and single-phase grid synchronization applications. Finally, Section 4.6 summarises the contributions of Chapter-4.

4.2 Overview of Existing Adaptive Synchronization Techniques

4.2.1 Adaptive Gain Tuning of SRFPLL

As discussed in Chapter 3, the proportional and integral gains of the conventional SRFPLL is designed based on the small-signal model which considers the PLL closed loop control as a second-order transfer function. This is recalled again in this chapter and given by (4.1). The conventional way of designing the PI gains takes into account the ideal grid condition i.e., Z_g = 0. In contrast, when the grid is weak the impact of grid impedance cannot be overlooked. The conventional way of tuning the PI gains becomes inappropriate under such conditions. The transfer function that defines the complete small-signal model of the SRFPLL considering the grid interaction of the VSC is given by

$$\frac{\theta_{PLL}(s)}{\theta_g(s)} = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} = \frac{K_{PPLL}\cos\theta_e s + K_{IPLL}\cos\theta_e}{s^2(1 - K_{PPLL}I_g K_3) + s(K_{PPLL}\cos\theta_e - K_{IPLL}I_g K_3) + K_{IPLL}\cos\theta_e} \tag{4.1}$$

where settling time: $t_s = \frac{9.2(1-K_{PPLL}I_g K_3)}{K_{PPLL}\cos\theta_e)}$ and damping ratio: $\zeta = \frac{K_{PPLL}\cos\theta_e - K_{IPLL}I_g K_3}{2\sqrt{(1-K_{PPLL}I_g K_3)}\sqrt{K_{IPLL}\cos\theta_e}}$

Adaptive tuning of the PI gains are proposed in [132] for the complete model of the SRFPLL. The control structure representing such adaptive gain tuning is shown in Figure 4.1(a). It can

be seen that both the proportional and integral gains (K_{PPLL} and K_{IPLL}) are varied in real time. The triggering parameters are chosen as the magnitude of positive and negative sequence voltage ($|V^{+}|$, $|V^{-}|$) with their corresponding transformation angle ($|\theta^{+}|$, $|\theta^{-}|$). The gains are updated based on a look up table containing the pre-defined gains during any fault. From (4.1) it can be seen by varying both K_{PPLL} and K_{IPLL} simultaneously, the settling time (t_s) for grid synchronization can be reduced by keeping the damping factor (ζ) unaffected. However this impacts the closed-loop stability of the SRFPLL. Increasing K_{PPLL} and decreasing K_{IPLL} in real time adaptively will impact current controller bandwidth during FRT, particularly if the bandwidth of the SRFPLL is high enough to enter the instability region. Moreover, the simultaneous update of PI gains (increasing K_{PPLL} and decreasing K_{IPLL}) might give faster FRT performance but due to the reduction of bandwidth, the higher order harmonic rejection capability of the PLL gets deteriorated.

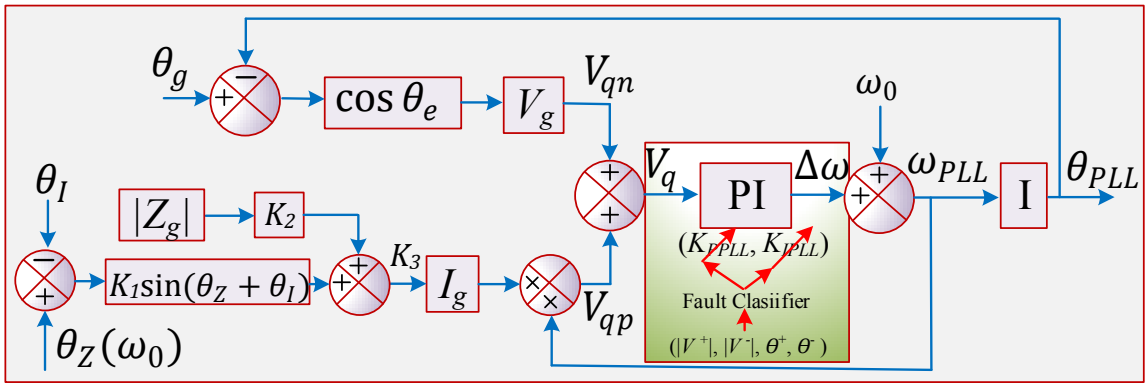


Figure 4.1 (a): Adaptive gain tuning (increasing K_{PPLL} and decreasing K_{IPLL}) of small-signal SRFPLL model using fault classifier-based look-up table.

The extra oscillations experienced by the conventional second-order SRFPLL due to PAJ can be reduced by controlling the damping ratio. Such an approach is proposed in [138], where the integral gain of the SRFPLL PI loop is made adaptive based on grid voltage amplitude estimation. The real time variations of (K_{IPLL}) regulate the damping ratio (ζ) as per relation (4.1) without affecting the settling time (K_{PPLL} is unchanged) as shown in Figure 4.1(b). In

[138], the adaptive K_{IPLL} design is chosen as the frequency error-based droop relationship. With this technique, though the oscillations in the estimated frequency, as a result of PAJ during the grid fault, are minimized, the unchanged settling time could not improve the FRT duration of conventional SRFPLL synchronized VSC. To deal with this, in addition to using an adaptive K_{IPLL} design, K_{PPLL} can also be varied as per strategy given in [138] to reduce the settling time (t_s). However, this may create a risk to the stability margin of the SRFPLL closed loop system.

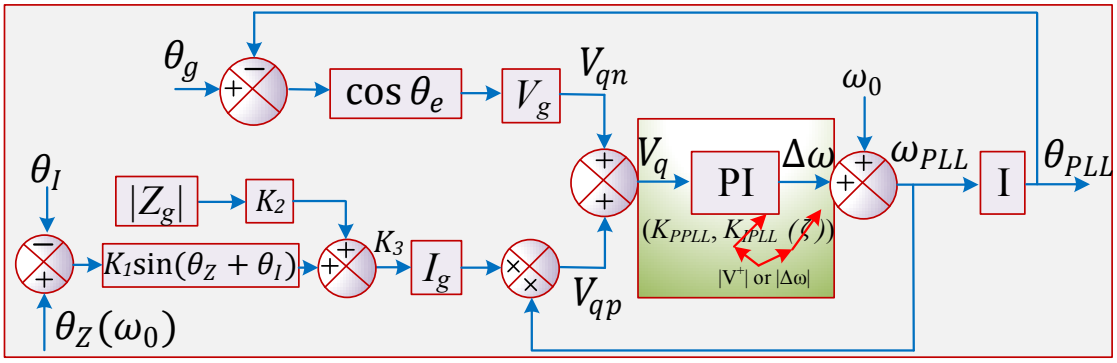


Figure 4.1 (b): Adaptive gain tuning (decreasing K_{IPLL} based on $\Delta\omega$ or $|V^+|$) of small-signal SRFPLL model.

4.2.2 First order SRFPLL

As observed previously, the adaptive PI gain tuning of SRFPLL during fault either decreases the settling time or increases the damping ratio and hence helpful for robust FRT of VSC. From the understanding of the loss of grid synchronization as discussed in Chapter 3, adequate damping factor is vital as compared to the settling time. This prioritises the design for adaptive K_{IPLL} of the SRFPLL. On the other hand, during the boundary condition of large signal stability limit (discussed in Chapter 3), only one equilibrium point exists during the fault. In such a scenario any positive value of the K_{IPLL} leads to loss of synchronism. This scenario is avoided by the transition of second-order SRFPLL to first-order SRFPLL during the fault [58], [59]. This is achieved by resetting the integrator (K_{IPLL} = 0) during the fault

inception and recovery time as shown in Figure 4.2. This solution provides an infinite damping based on (4.1). In [58], the rate of change of frequency (ROCOF) error is selected as the enabling parameter to set and reset the K_{IPLL}. The expression for the estimated phase-angle in such cases is given by

$$\frac{\theta_{PLL}(s)}{\theta_g(s)} = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} = \frac{K_{PPLL}\cos(\Delta\theta)s}{s^2(1 - K_{PPLL}I_g K_3) + s(K_{PPLL}\cos(\Delta\theta))} \tag{4.2}$$

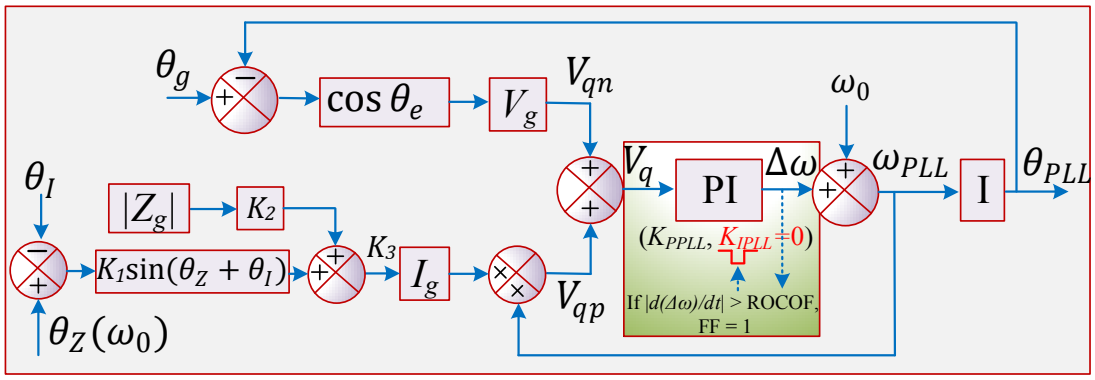


Figure 4.2: Adaptive gain tuning (K_{IPLL} = 0 based on rate of change of frequency error) of small-signal SRFPLL model by switching from second-order SRFPLL to first-order SRFPLL during fault.

The transition to first-order SRFPLL although provides sufficient damping to avoid loss of synchronism (LOS) it is unable to provide a faster settling time required for FRT for cases other than LOS. This is because the settling time is dependent on K_{PPLL} which is already providing a trade-off between settling time and harmonic rejection capability. Such huge settling times will not promptly inject the full reactive current (1.0 pu) during the voltage sags of 50% or more during the FRT period (usually ≅150 ms).

4.2.3 Freezing SRFPLL

Based on the discussion in 4.2.1 and 4.2.2, it is understood that the adaptive tuning of the PI gains of the SRFPLL during fault is always a trade-off between its dynamic and steady state performance. Instance of occurrence of grid fault based transients is rare in comparison to the

normal operating conditions. Hence, the SRFPLL parameters are designed keeping in mind the normal grid conditions. Additionally, grid faults may or may not always have associated PAJs. PAJs mainly occur if the X/R ratios of the fault impedance and grid impedances are unequal [68]. Moreover, during severe symmetrical faults (≅ 100% sag), the PAJ seen at the grid side does not affect the PCC voltage. Note that the SRFPLL takes the PCC voltage as the reference to synchronise the VSC. In all these cases, where the PAJ is of no concern, oscillations and overshoot observed in the estimated frequency by SRFPLL is very less. The loss of synchronization as a result of severe symmetrical fault is inevitable if the large signal stability is violated (refer Chapter 3). Thus to overcome the loss of synchronism during such instances (as a result injecting current more than the steady-state limit), freezing of the PLL loop is recommended [53]. The control structure of the freezing PLL is shown in Figure 4.3. The enabling parameter to freeze the PLL during fault is selected as the amount the voltage sag i.e. magnitude of the voltage at the PCC. In such cases, the SRFPLL is totally ignorant regarding the event during the fault and it estimates the frequency exactly equal to the grid frequency (ω_g). Accordingly, the phase-angle (θ_{PLL}) estimated is always the reference value set during the normal grid conditions.

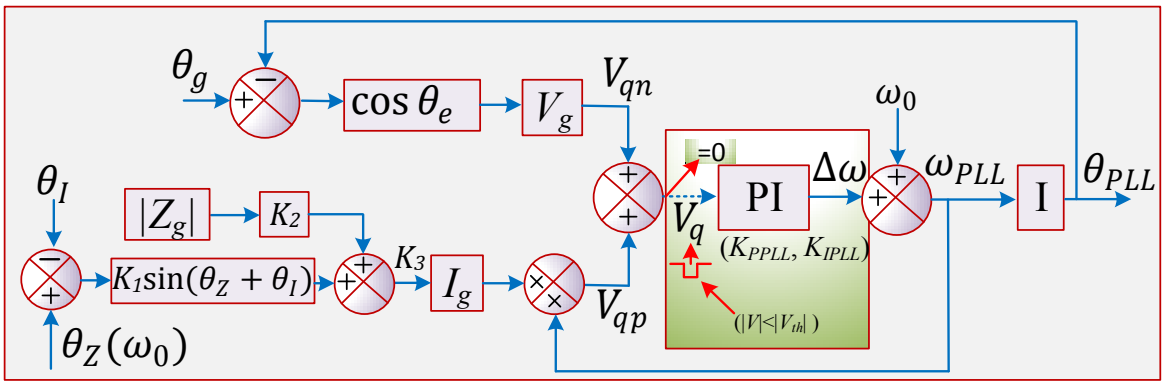


Figure 4.3: Control structure of the freezing SRFPLL in the small-signal model.

During any PAJ at the grid voltage where the fault level is not so severe (sag depth is not near to 100%), there occurs a steady-state phase-angle error between the actual phase-angle due to

PAJ and that estimated by the freeze PLL. This leads to unregulated active and reactive power flows during the FRT, thereby violating the grid codes.

In conclusion, the freezing PLL can provide a robust current controller performance during the FRT, to mitigate severe fault conditions such as zero voltage ride-through (ZVRT) requirements. However, additional phase-angle compensation is required during non-severe faults having PAJ to follow the grid code accurately.

4.2.4 Adaptive Current Injection based Techniques

Several adaptive current injection methods have been proposed to overcome the loss of synchronism as a result of large signal instability occurring during severe grid faults. Ref [55] proposed to halt the current injection during severe faults (having voltage sag depth below the impedance level) at the PCC. This method certainly avoids any LOS during fault but violates the grid code. A limited active and reactive current injection strategy is proposed to deal with LOS issue. This strategy is unable to inject the maximum current limit and thus is not suitable to meet the grid code requirements [56].

Current injection based on the X/R ratio of the impedance between the fault point and PCC can eliminate the LOS issue [57]. Such controlled current injection makes the positive feedback to the SRFPLL to zero as a result of grid interaction of VSC, i.e. $V_{qp} = 0$. Derivation of such adaptive current injections is provided as

$$\begin{gathered} V_{qp} = 0 \Rightarrow I_g Z_g \sin(\theta_Z + \theta_I) = 0 \\ \sin(\theta_Z + \theta_I) = 0 \Rightarrow |\theta_I| = |\theta_Z| \Rightarrow \left|\frac{I_{qr}}{I_{dr}}\right| = \left|\frac{X_g}{R_g}\right| \Rightarrow |I_{dr}| = \left|\frac{R_g}{X_g}\right| |I_{qr}| \end{gathered} \tag{4.3}$$

The control structure for such X_g/R_g dependent current injection is shown in Figure 4.4. The adaptive selection of active current reference should be enabled during severe fault scenarios, otherwise during non-severe faults or normal grid conditions, sufficient active power dispatch

will not be possible and hence the electrical stress on the chopper resistance will increase. Measurement of the grid impedance can be possible using either off-line or on-line methods [139].

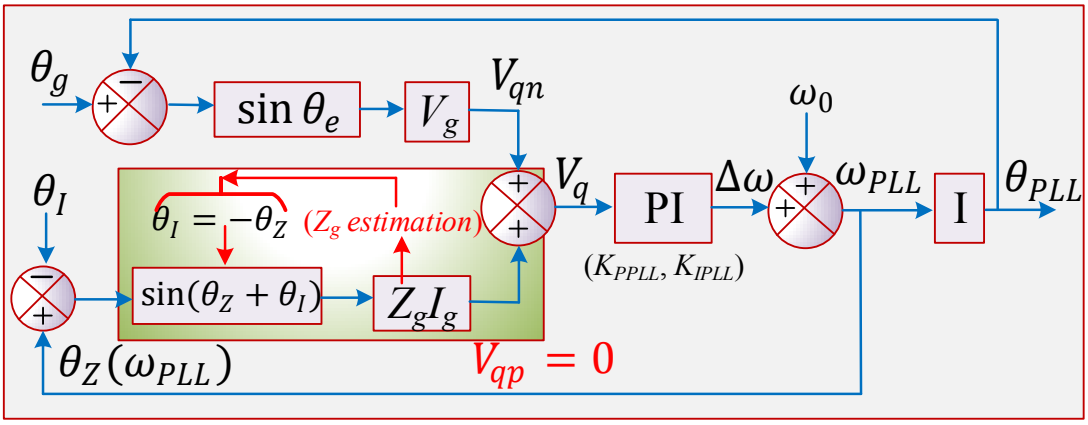


Figure 4.4: X/R ratio dependent grid current injection strategy during faults.

The main challenge with such type of current injection is the precise measurement of grid impedance (R_g, X_g). During severe grid faults, inaccurate measurement of grid impedance leads to poor FRT performance of VSC. Additionally, if maximum current and the maximum reactive current injection (as per grid code) are equal, a compromise between the full reactive current injection and remaining active current injection will be needed.

Based on the above discussions, the main objective of this chapter is to propose a simple, reliable and faster grid synchronization technique for improved FRT of power converters. The proposed technique is used in parallel to the conventional SRFPLL. It is activated to synchronize the converter only during grid faults with PAJ. It is compatible with both three-phase and single-phase systems that use conventional SRFPLL based closed-loop synchronization techniques. Further, the optimal design and simple control structure of the conventional second-order SRFPLL is retained to accurately track normal grid operating conditions. The next Section discusses the proposed hybrid grid synchronization technique.

4.3 Proposed Hybrid Grid Synchronization Technique

The overall control schematic of the proposed hybrid grid synchronization technique is shown in Figure 4.5(a). The overview of the frequency and phase-angle estimators used in the proposed hybrid concept for three-phase and single-phase systems is shown in Figure 4.5(b).

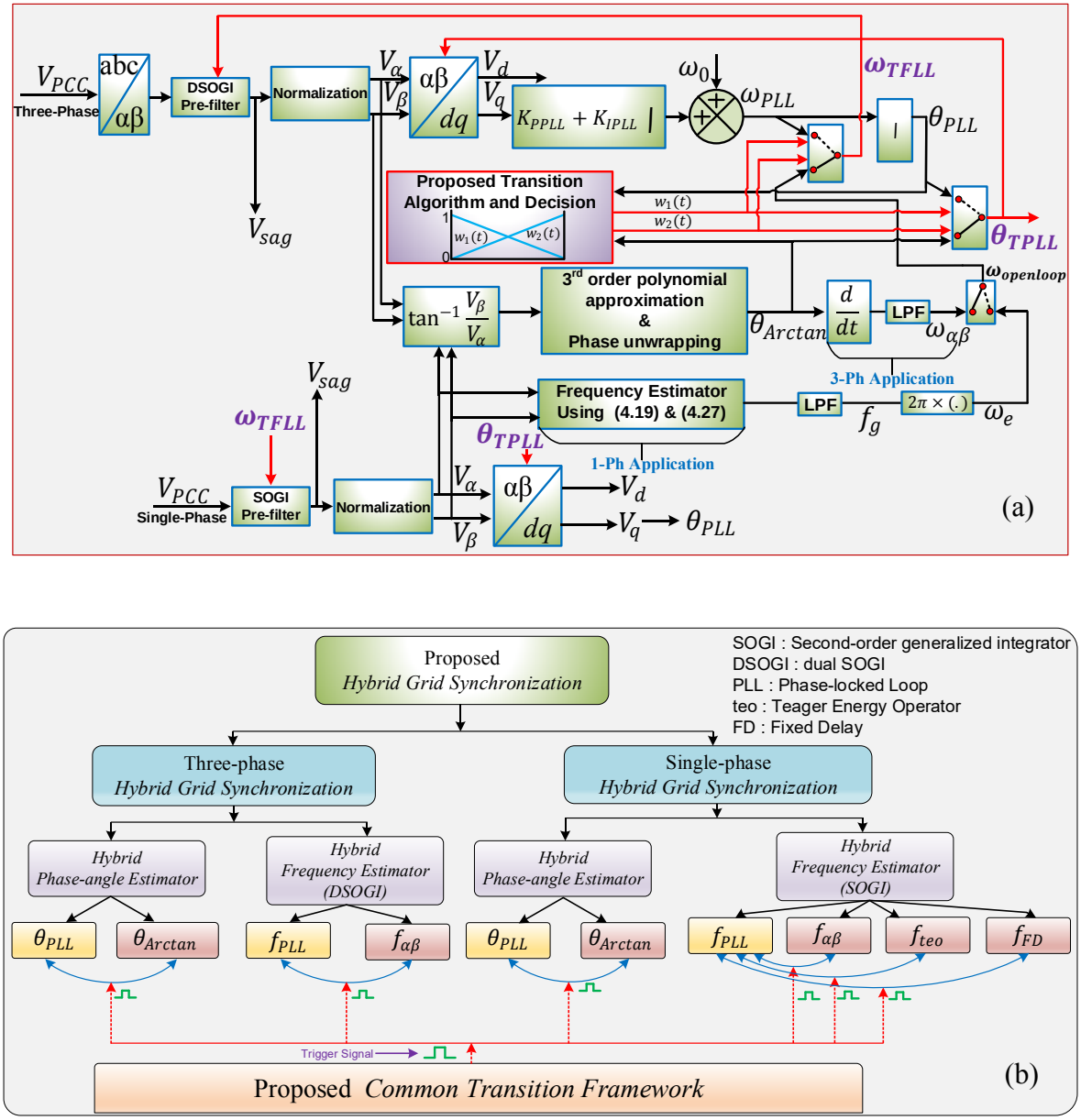


Figure 4.5: (a) Control schematic of the proposed hybrid grid synchronization transition technique and (b) Overview of frequency and phase-angle estimators used for the proposed technique for three-phase and single-phase grid synchronization.

4.3.1 Three-phase Hybrid Grid Synchronization

4.3.1.1 Hybrid Phase-angle Estimator

It consists of two phase-angle estimators for the grid synchronization purposes. During the occurrence of grid fault having PAJ, the phase-angle estimation is switched from the SRFPLL (θ_{PLL}) to the arctangent based estimation (θ_{arctan}). The grid synchronization during the fault with such hybrid phase-angle estimation is named as "Transition Phase-locked Loop (TPLL)" and the corresponding phase-angle is denoted as "θ_{TPLL}". It is worth noting that such phase-angle estimation using the arctangent function adds computational burden for low cost digital signal processor (DSP). To minimise the computation complexity for such DSP, a third-order polynomial approximation of the "arctan" function followed by phase unwrapping is presented as follows.

As shown in Figure 4.5, for phase-angle estimation, arctangent function is used over the $\alpha\beta$ components of the grid voltage measured at the PCC as

$$\theta_{arctan} = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \tag{4.4}$$

The above arctangent function in (4.4) can be written as a third-order polynomial function as given by

$$\tan^{-1}(x) \cong \frac{\pi}{2} \times \frac{a_3x^3 + a_2x^2 + a_1x + a_0}{b_3x^3 + b_2x^2 + b_1x + b_0} \tag{4.5}$$

Where, $x = \frac{V_\beta}{V_\alpha}$. The numerator and denominator coefficients are calculated using the properties of arctangent function as four basic constraints in the domain [0, ∞). Based on the first constraint, which says $\tan^{-1}(0) = 0$, the value of $a_0 = 0$ in (4.5). As per second constraint, $\lim_{x\to\infty} \frac{2\tan^{-1}(x)}{\pi} = 1$, we can get the relation as $a_3 = b_3 = 1$. Further a third

constraint on (4.5) is applied as $\tan^{-1}(x) + \tan^{-1}\left(\frac{1}{x}\right) = 1$. On solving these three constraints together, (4.5) leads to a single coefficient (k) based polynomial as given by

$$\tan^{-1}(x) \cong \frac{\pi}{2} \times \frac{x^3 + x^2 + kx}{x^3 + 4k^2x^2 + 4k^2x + 1} \tag{4.6}$$

Applying an iterative process known as Remez Algorithm [140] based min-max criteria (4.6) can be solved to form a quadratic equation for k as $4k^2 - k - 1 = 0$. On solving we get $k \approx 0.6404$. Putting the value for k and by replacing $x = \frac{V_\beta}{V_\alpha}$, (4.6) can be rewritten as

$$\theta_{arctan} = \tan^{-1}(x) \cong \frac{\pi}{2} \times \frac{{V_\beta}^3 + {V_\beta}^2 V_\alpha + 0.6404 V_\beta {V_\alpha}^2}{{V_\beta}^3 + 1.6404 {V_\beta}^2 V_\alpha + 1.6404 V_\beta {V_\alpha}^2 + {V_\alpha}^3} \tag{4.7}$$

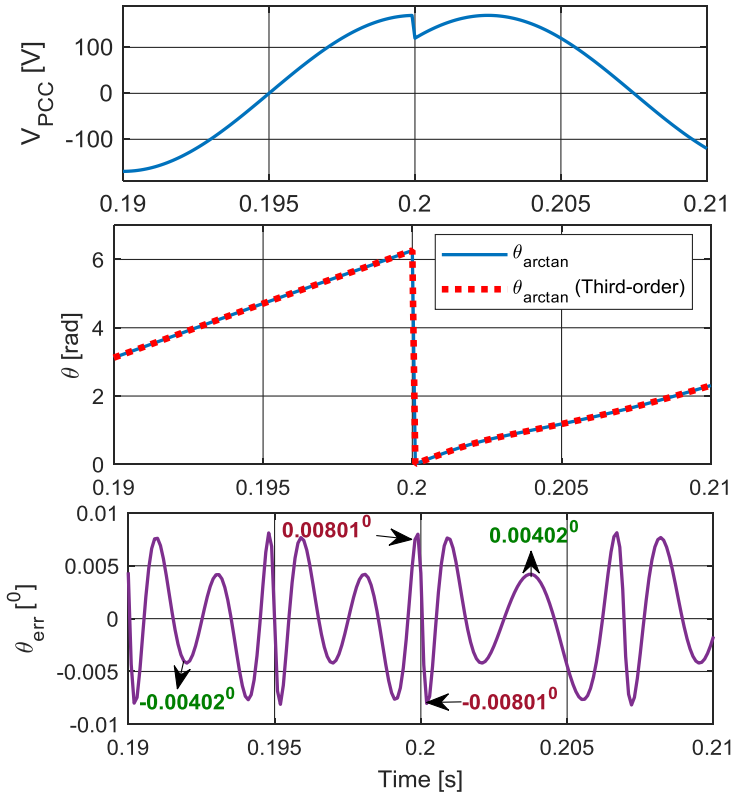


Figure 4.6: Graphical representation of third-order polynomial approximation of arctangent function.

A graphical representation of such approximation during a -45° PAJ at t = 0.2 s in the grid voltage is shown in Figure 4.6. The maximum error between (4.4) and (4.7) during the phase-jump oscillates between ± 0.00801°, while the minimum error oscillates between ±0.00402°. Such insignificant errors are neglected especially when PAJ of large magnitude is considered.

The phase-angle estimated using arctangent varies between $-\pi/2$ to $+\pi/2$. This angle needs to be unwrapped and bounded between 0 to $+2\pi$ for control purposes. For unwrapping, the four-quadrant phase-angle approximation is used as given by

$$If \begin{cases} V_\beta > 0 \; and \; V_\alpha > 0 \; then \;\; \theta_{arctan} = \dfrac{\pi}{2} + \theta_{arctan}; \\ V_\beta > 0 \; and \; V_\alpha < 0 \; then \; \theta_{arctan} = \dfrac{\pi}{2} + \theta_{arctan}; \\ V_\beta < 0 \; and \; V_\alpha < 0 \; then \; \theta_{arctan} = \dfrac{3\pi}{2} + \theta_{arctan}; \\ V_\beta < 0 \; and \; V_\alpha > 0 \; then \; \theta_{arctan} = \dfrac{3\pi}{2} + \theta_{arctan}; \end{cases} \tag{4.8}$$

The instance of phase-angle unwrapping during a -45° PAJ at t = 0.2 s in the grid voltage is shown in Figure 4.7.

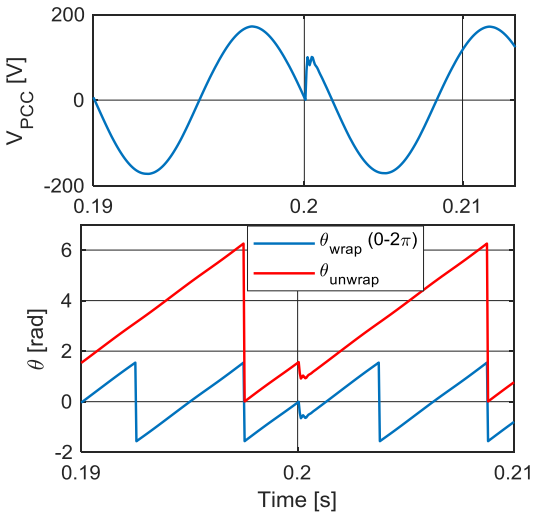


Figure 4.7: Graphical representation of phase-angle unwrapping of arctangent function based phase-angle estimation.

4.3.1.2 Hybrid Frequency Estimator

In case of three-phase unbalanced grid voltage during asymmetrical faults, phase-angle estimation using arctangent function suffers from double power frequency oscillations. This is avoided by using frequency-adaptive dual second-order generalized integrator (DSOGI) based pre-filter for the grid voltage. It extracts the positive sequence three-phase voltage components. It basically behaves as a bandpass filter (BPF) with its centre frequency tuned by a frequency estimator. The SRFPLL structure is used to provide the frequency and hence it is called DSOGIPLL for three-phase applications. The basic control structure of DSOGI is shown in Figure 4.8. The drawback of this control structure is the presence of two interdependent loops. One is for the frequency and another for the phase-angle (as shown in red colour arrow in Figure 4.8). During grid transients like voltage sag, frequency variations or phase-jumps such technique suffers from the PLL in-loop delay which affects the FRT of the converter control. Further, the frequency-adaptive nature of the DSOGIPLL makes it complex to implement and reduces the stability margin.

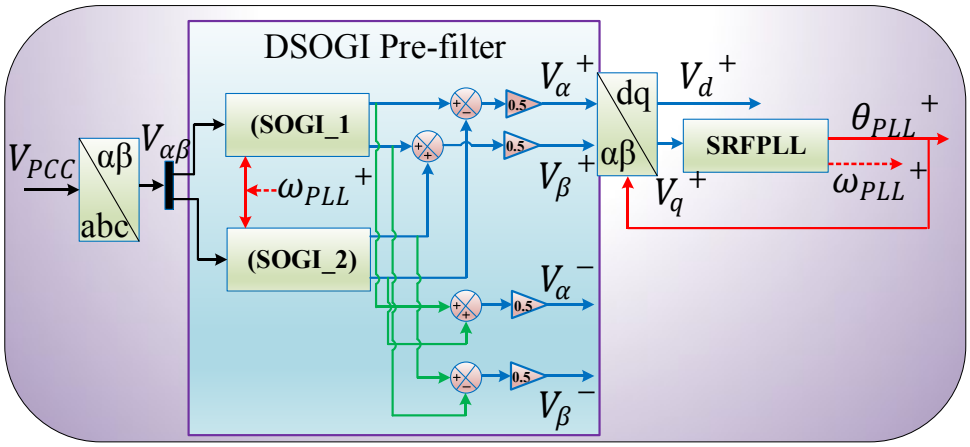


Figure 4.8: Basic control structure of dual second-order generalized integrator with the SRFPLL (DSOGIPLL).

Unlike the conventional DSOGIPLL concept, the frequency adaptability of the DSOGI pre-filter is enhanced using transition based hybrid frequency estimations. In addition to phase-

angle transition as discussed above, the frequency estimation is switched from SRFPLL technique to the rate of change of arctangent phase-angle estimation. The expression for the frequency estimation is given by

$$f_{\alpha\beta}{}^{+} = \frac{\omega_{\alpha\beta}{}^{+}}{2\pi} = \frac{1}{2\pi}\frac{d\left(\theta_{arctan}{}^{+}\right)}{dt} = \frac{1}{2\pi}\frac{d[\tan^{-1}(V_{\beta}{}^{+}(t)/V_{\alpha}{}^{+}(t))]}{dt} = \frac{\dot{V_{\beta}}{}^{+}(t)V_{\alpha}{}^{+}(t) - V_{\alpha}{}^{+}(t)\dot{V_{\beta}}{}^{+}(t)}{[V_{\alpha}{}^{+}]^2 + [V_{\beta}{}^{+}]^2} \tag{4.9}$$

where '+' represents the positive sequence phase-angle. The discrete implementation of the frequency estimation is shown in Figure 4.9. A first-order infinite impulse response (IIR) based digital filter as shown in Figure 4.10 is used at the output of the frequency estimation. It is used to generate the filtered frequency ($f_{\alpha\beta(f)}{}^{+}$) as given by

$$f_{\alpha\beta(f)}{}^{+} = c(f_{\alpha\beta}{}^{+}) + (1-c)(f_{\alpha\beta(f)}{}^{+}(n-1)) \tag{4.10}$$

'c' is called the forget factor which is related to the filter cut off frequency (f_c) and sampling frequency (f_{sam}) and calculated as $c = 1 - e^{-2\pi f_c/f_{sam}}$.

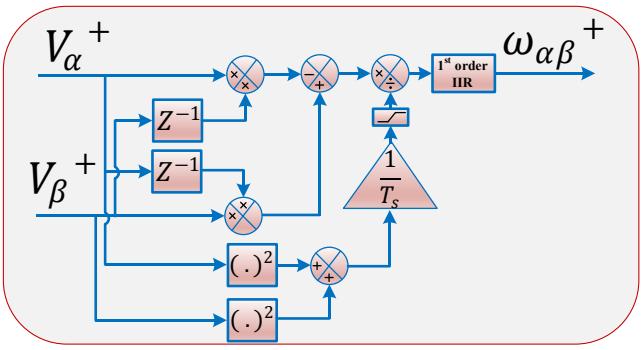


Figure 4.9: Frequency estimation using the arctangent derived function in αβ-frame.

The overall schematic of the hybrid frequency and phase-angle estimations controlled by the hybrid grid synchronization scheme is shown in Figure 4.11. The positive sequence

component of the three-phase unbalanced voltage is extracted using the proposed hybrid frequency-adaptive DSOGI pre-filter during asymmetrical faults.

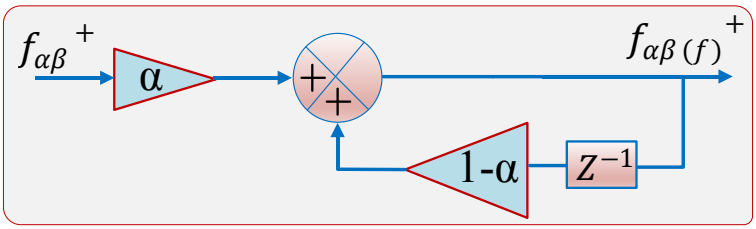


Figure 4.10: Schematic of first-order IIR based low-pass filter.

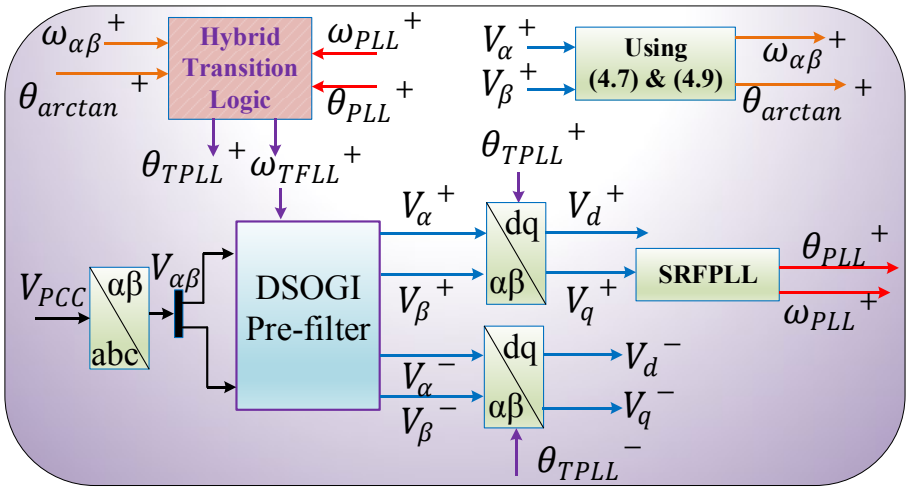


Figure 4.11: Sequence component extraction and synchronization using adaptive DSOGIPLL under the proposed hybrid grid synchronization principle.

4.3.2 Single-phase Hybrid Grid Synchronization

In contrast to a three-phase system, a single-phase system requires QSG unit to generate the quadrature component of the measured single-phase voltage. A second-order generalized integrator (SOGI) is used for this purpose. Similar to the DOSGIPLL for three-phase synchronization discussed above, it also relies on the SRFPLL frequency estimation. The complete control structure (SOGI in cascade with SRFPLL) is called as SOGIPLL and shown in Figure 4.12. The implementation difficulties while feeding frequency back by SRFPLL as

in DOSGIPLL are also applicable to SOGIPLL, especially during faults. Hence, improvement of the frequency adaptability of SOGIPLL is the primary objective of the proposed single-phase hybrid grid synchronization. Similar to the three-phase technique, single-phase hybrid grid synchronization includes both hybrid phase-angle and hybrid frequency estimators. These will be detailed in the following sub-sections.

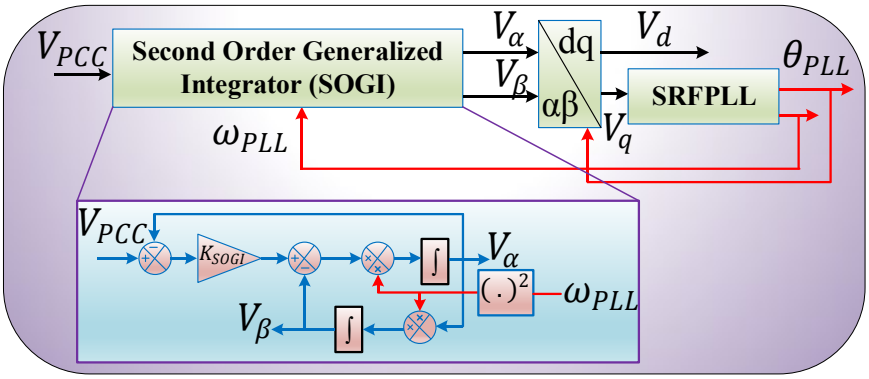


Figure 4.12: Basic control structure of second-order generalized integrator with the SRFPLL (SOGIPLL).

4.3.2.1 Hybrid Phase-angle Estimator

The hybrid phase-angle estimator used for single-phase hybrid grid synchronization is implemented in the same way like that for a three-phase system. During the PAJ as a result of grid faults, arctangent function is used to estimate the phase-angle using the equivalent *αβ*-components (generated from SOGI) of the measured single-phase voltage. On the fault recovery, phase-angle estimation is switched to the SRFPLL estimation.

4.3.2.2 Hybrid Frequency Estimator

Three methods are proposed for single-phase grid synchronization, to estimate and feed the frequency to the SOGI during grid faults having PAJ. These estimators are used in parallel with the SRFPLL estimator and thus referred as hybrid frequency estimator in this thesis. The

three frequency estimators implemented are: 1) arctangent derived [141], 2) Teager Energy Operator (TEO) [124] and 3) Fixed Delay (FD) method [143]. Out of these three techniques, the implementation of the arctangent derived frequency using the $\alpha\beta$-component of the voltages as a substitute to SRFPLL estimation is already presented during the discussion of three-phase hybrid grid synchronization and will not be explained again. The frequency estimation for SOGI using TEO and FD technique will be detailed as below. The frequency estimation using these two techniques require only single-phase voltage signal.

a) Frequency Estimation Using Teager Energy Operator (TEO)

The frequency of the single-phase voltage (measured at the PCC) can be estimated using teager energy using either 3 or 5 samples depending on the information of the PCC voltage amplitude [124]. Accordingly, a two-step estimation of the grid voltage frequency (ω_g) is carried out as follows.

Step: 1. Let us say, the sampled (sampling time T_s) PCC voltage ($V_{PCC}(n)$) is represented by a cosine signal as given by

$$V_{PCC}(n) = |V(n)| \cos(\omega_g n T_s + \varphi_g) \tag{4.11}$$

According to the teager energy operator principle, energy of $V_{PCC}(n)$ can be calculated using its three consecutive samples as given by

$$\begin{aligned} E[V_{PCC}(n)] &= \frac{1}{T_s{}^2} \times [V_{PCC}(n)^2 - V_{PCC}(n-1)V_{PCC}(n+1)] \\ &= |V(n)|^2 \sin^2(\omega_g T_s) \quad = |V(n)|^2 (\omega_g T_s)^2 \end{aligned} \tag{4.12}$$

Putting (4.11) in (4.12), we can simplify (4.12). The discrete difference of the PCC voltage signal ($\dot{V_{PCC}}(n)$) as per discrete energy separation algorithm (DESA)-II can be obtained as [124],

$$\dot{V_{PCC}}(n) = \frac{V_{PCC}(n+1) - V_{PCC}(n-1)]}{2T_s}$$

$$= \frac{|V_{PCC}(n+1)|\cos\left(\omega_g(n+1)T_s + \varphi_g\right) - |V_{PCC}(n-1)|\cos(\omega_g(n-1)T_s + \varphi_g)}{2T_s} \quad (4.13)$$

$$= V_{PCC}(n)\sin(\omega_g T_s)\sin(\omega_g T_s + \varphi_g)$$

The teager energy of the rate of the change of the PCC voltage ($\dot{V_{PCC}}(n)$) is given by

$$\begin{aligned} E\left[\dot{V_{PCC}}(n)\right] = {} & \frac{1}{4 \times {T_s}^2} \\ & \times \left[\{V_{PCC}(n+1) - V_{PCC}(n-1)^2\} - \left(V_{PCC}(n+2) - V_{PCC}(n)\right)\right. \\ & \left. \times \left(V_{PCC}(n) - V_{PCC}(n-2)\right)\right] \end{aligned} \quad (4.14)$$

Putting the value for $V_{PCC}(n)$ in (4.14), and solving trigonometric identities we get

$$E\left[\dot{V_{PCC}}(n)\right] = |V(n)|^2 \sin^4(\omega_g T_s) \quad (4.15)$$

Dividing (4.15) by (4.12) and solving for $f_g = \frac{\omega_g}{2\pi}$, we get

$$f_g = \frac{1}{2 \times \Pi \times T_s} \times \sin^{-1}\left(\sqrt{\frac{E\left[\dot{V_{PCC}}(n)\right]}{E[V_{PCC}(n)]}}\right) \quad (4.16)$$

The implementation of (4.16) is shown in Figure 4.13.

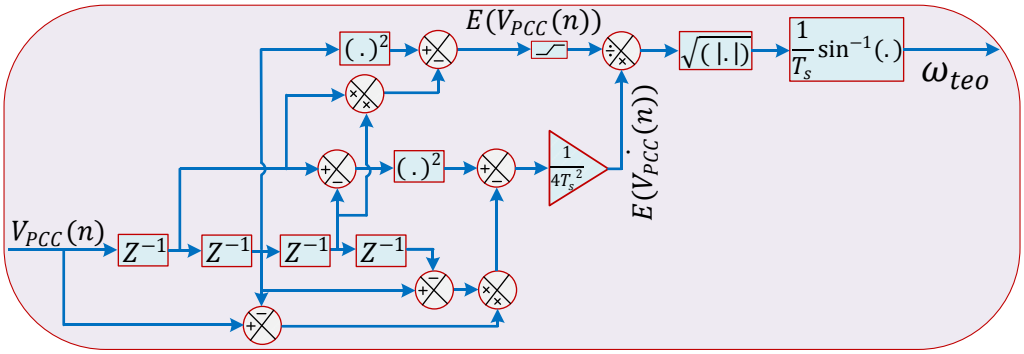


Figure 4.13: Exact model of frequency estimation of single-phase voltage signal using teager energy operator.

Here, it is observed that the frequency estimation takes five samples ($5T_s$) to solve (4.16), provided the amplitude of the signal i.e. $|V(n)|$ is unknown. If the input voltage can be normalized (i.e. $|V(n)|$ = 1.0 pu), the frequency can be estimated from (4.12), using only three consecutive samples ($3T_s$) by following Step 2.

Step: 2. From (4.12) we get,

$$\sin^2(\omega_g T_s) = \frac{E[V_{PCC}(n)]}{|V(n)|^2}$$

$$\Rightarrow \sin^2(\omega_g T_s) = E\left[v_g(n)\right], \text{ if } |V(n)| = 1.0 \text{ pu} \tag{4.17}$$

$$\Rightarrow \omega_g = \frac{1}{T_s}\sin^{-1}\sqrt{E[V_{PCC}(n)]} \rightarrow f_g = \frac{1}{2\pi T_s}\sin^{-1}\sqrt{E\left[v_g(n)\right]}$$

Approximation of '$\sin^{-1}$' to reduce computational burden is done using its Taylor series expansion under the assumption that sampling frequency (f_s =10 KHz) > 8 times the fundamental frequency (f =50 Hz). This gives

$$\sin^{-1}(x) \approx x \tag{4.18}$$

thus (4.17) is simplified as

$$f_g = f_{teo} = \frac{1}{2 \times \Pi \times T_s} \times \sqrt{[V_{PCC}(n)^2 - V_{PCC}(n-1)V_{PCC}(n+1)]} \tag{4.19}$$

and the approximation model is shown in Figure 4.14. This is called the approximated model for frequency estimation using teager energy operator.

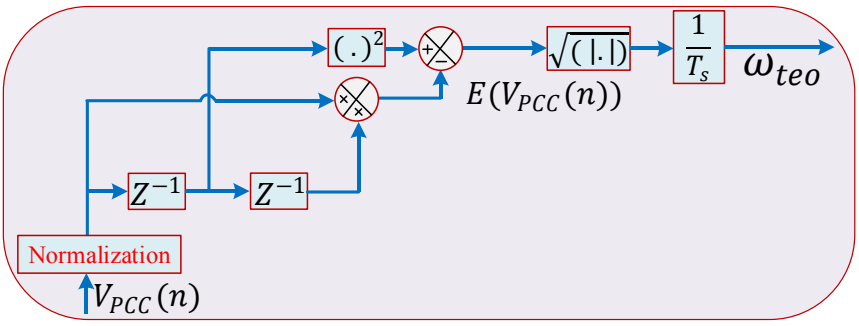


Figure 4.14: Approximated model of frequency estimation of normalized single-phase voltage signal using teager energy operator.

Two normalization methods are presented below to normalize the single-phase PCC voltage and feed to the teager energy operator to estimate the frequency using (4.19) for SOGI during fault.

i) Normalization Method-1

The *Normalization Method-1* normalizes the single-phase voltage signal ($V_{PCC}(n)$) using an additional band pass filter (BPF) as shown in Figure 4.15. A recursive discrete Fourier transform (DFT) and inverse DFT (IDFT) concept is used to implement the BPF, whose centre frequency is made adaptive in nature as shown in Figure 4.16 [142]. The frequency estimated by the TEO is provided as a feedback to decide the number of samples as $N = ceil\left(\frac{f_{sam}}{f_{teo}}\right)$. The ceil function is used to round off the sample size during non-integer frequency jumps. The designed BPF takes 20 ms extra time to provide the normalized PCC voltage signal. The transfer function of the BPF is represented in the discrete domain as

$$TF(z) = \frac{V_{pu}(z)}{V_{PCC}(z)} = \frac{1 - Z^{-N}}{N(1 - e^{j\frac{2\pi}{N}}Z^{-1})} \tag{4.20}$$

where $V_{PCC}(n)$ is the measured single-phase voltage signal and $V_{pu}(n)$ is the filtered and normalized signal which is fed to the TEO.

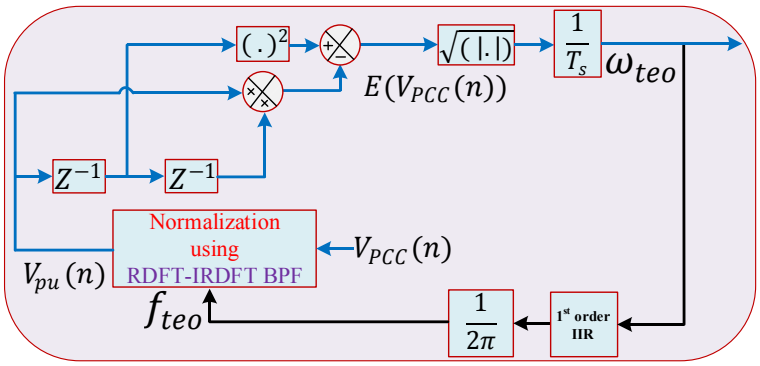


Figure 4.15: RDFT-IRDFT based normalization of single-phase voltage.

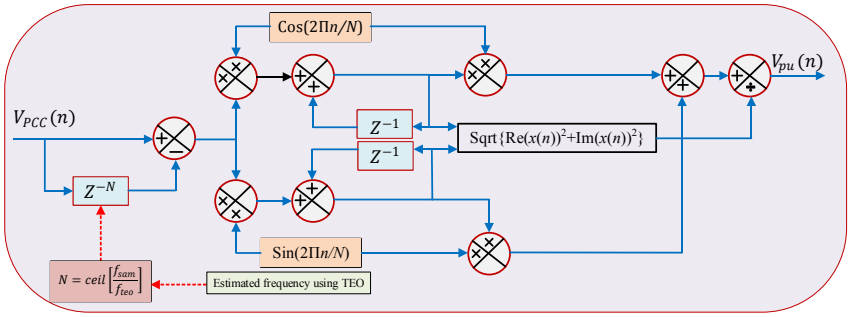


Figure 4.16: Schematic of RDFT-IRDFT based normalization.

The schematic of the proposed adaptive SOGIPLL (shown in green colour) [142] along with the hybrid grid synchronization scheme to feed the SOGI filter with the hybrid frequency (ω_{TFLL}) is shown in Figure 4.17. The phase-angle required for the Park transformation can be provided by θ_{TPLL} as discussed previously. Such hybrid frequency and phase-angle estimation is controlled by the common transition logic which will be discussed later in this chapter. Moreover, the current control of single-phase converter during fault having both voltage sag and PAJ along with FRT strategy using the hybrid grid synchronization shown in Figure 4.17 will be detailed in Chapter-6.

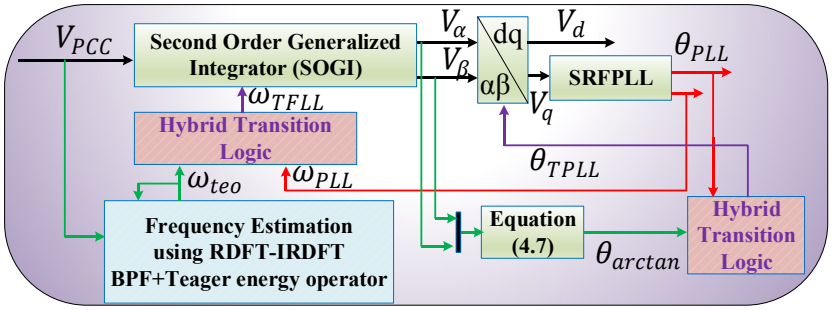


Figure 4.17: Hybrid Frequency adaptive SOGI using frequency estimation by the combination of RDFT-IRDFT BPF and teager energy operator during grid faults.

ii) Normalization Method-2

As it can be observed from Figure 4.17, the implementation of adaptive and hybrid grid synchronization includes an additional BPF along with the SOGI BPF. This makes the whole structure computational intensive for low cost DSP though it outperforms the conventional SOGIPLL during grid transients. To simplify the structure given in Figure 4.17, the normalization of the single-phase voltage is using the outputs from SOGI BPF. The normalized in-phase component i.e. the α-component of the PCC voltage (V_α) is fed to the teager energy operator for frequency estimation as shown in Figure 4.18. This is named as *Normalization Method-2*. The normalization of V_α is done using

$$V_{\alpha pu} = \frac{V_\alpha}{\sqrt{{V_\alpha}^2 + {V_\beta}^2}} \tag{4.21}$$

The estimated frequency by teager (ω_{teo}) is fed to the SOGI BPF to retain its frequency-adaptive nature like SOGIPLL. Such frequency estimation will be used during grid transients such as voltage sag or PAJ. During normal operating condition, frequency estimation will be switched back to the SRFPLL estimation for accurate frequency tracking along with good harmonic rejection capability. Phase-angle estimation will be followed in the same way as described in *Normalization Method-1*.

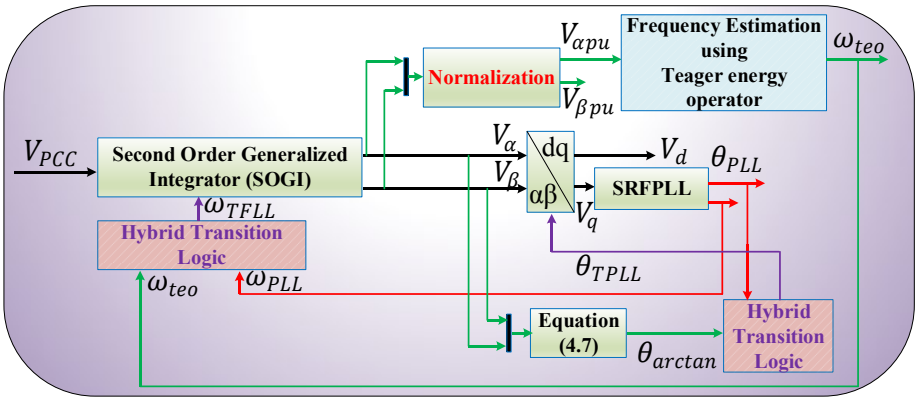


Figure 4.18: Hybrid Frequency adaptive SOGI using frequency estimation by the combination of SOGI BPF and teager energy operator during grid faults.

b) Frequency Estimation using Fixed Delay Technique

The frequency of any single-phase voltage signal can be estimated by providing fixed amount of delay to it [143]. Such frequency estimation technique provides faster grid synchronization property provided the input voltage signal is purely sinusoidal. However, during distorted voltage conditions (lower and higher order harmonic contents), the estimated frequency is diluted with harmonics in addition to fundamental component (50 Hz). To deal with this issue [143] used various advanced pre-filters such as second-order low pass filter (LPF) and cascaded delayed signal cancellation (CDSC). With the use of this filter, though the estimated frequency contains pure 50 Hz component, such implementation increases the computational complexity of the whole frequency estimation process. During off-nominal (frequency ≠ 50 Hz) variations, such filters add additional phase-angle delay to the actual phase-angle unless the pre-filters are made frequency adaptive. In order to estimate the phase-angle using the arctangent function, [143] used additional QSG unit (to generate V_β) that needed the calculation of trigonometric functions (sine and cosine terms).

To reduce the computational burden and avoid the use of additional trigonometric functions to generate V_β, in this thesis, the frequency estimation principle is used with the SOGI filtered

V_α signal. SOGI acts as a BPF that effectively eliminates the lower and higher order harmonics in the measured single-phase voltage signal. The resonant frequency of the SOGI BPF is made adaptive with estimated frequency feedback. The peculiarity of this implementation is that it simultaneously generates the V_β by the principle of SOGI using two integrators. The phase-angle is estimated using the third-order polynomial approximations of the arctangent function on the V_α and V_β as mentioned earlier. The proposed SOGI BPF does not add any additional phase-angle delay during off-nominal frequency variations as its frequency-adaptive behaviour is retained (like SOGIPLL). The frequency estimation technique is explained as below:

The in-phase component ($V_\alpha(n)$) of the measured single-phase voltage signal (measured at the PCC) can be expressed as

$$V_\alpha(n) = |V(n)| \cos(\omega_g n T_s) \tag{4.22}$$

Two fixed delayed signals of $V_\alpha(n)$ are generated by delaying by 'T_1' and 'T_2' as given by

$$V_{\alpha1}(n) = V_\alpha\left(n - \frac{T_1}{T_s}\right) \tag{4.23a}$$

$$V_{\alpha2}(n) = V_\alpha\left(n - \frac{2T_1}{T_s}\right) \tag{4.23b}$$

The signal s1(n) can be evaluated as given by

$$s1(n) = V_{\alpha1}(n)^2 - V_\alpha(n)V_{\alpha2}(n) \tag{4.24}$$

Similarly another signal s2(n) is calculated as

$$s2(n) = V_{\alpha1'}(n)^2 - V_{\alpha'}(n)V_{\alpha2'}(n) \tag{4.25}$$

where $V_{\alpha'}(n) = V_{\alpha 1}\left(n - \frac{2T_1}{T_s}\right)$ and $V_{\alpha 1'}(n)$ and $V_{\alpha 2'}(n)$ are delayed with respect to $V_{\alpha'}(n)$ by 'T_1' and 'T_2' respectively.

Dividing (4.25) by $s1(n - \frac{T_1}{T_s})$, the frequency of the single phase voltage signal (f_g=$\omega_g/2\pi$) can be obtained as

$$f_g(n) = \frac{\cos^{-1}\left(\frac{0.5 \times s2(n)}{s1\left(n - \frac{T_1}{T_s}\right)} - 1\right)}{4\pi T_1} \tag{4.26}$$

The relation between 'T_1' and 'T_2' is chosen to be $T_2 = 2T_1$ to simplify the trigonometric identities for frequency estimation. The value for T_1 is tested as 1ms, 2 ms, 4 ms and 8 ms to observe the overshoot and settling time of the estimated frequency dynamics. The optimum value is chosen to be 2 ms. At the output of the frequency estimation, first-order IIR filter is used to provide noise immunity. The complete schematic of the frequency estimation process is given in Figure 4.19.

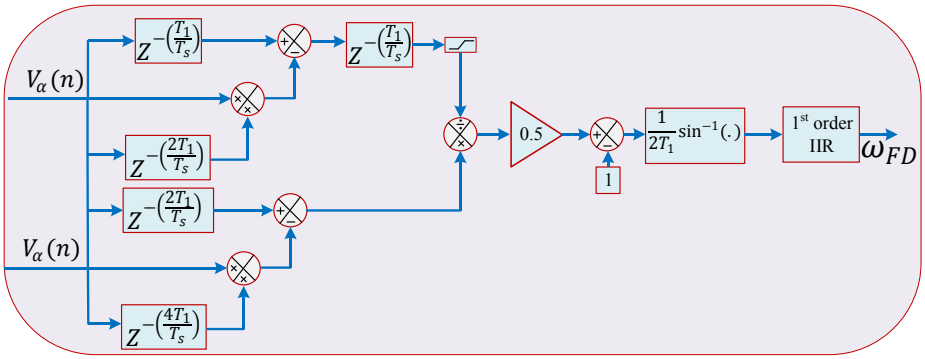


Figure 4.19: Exact model of frequency estimation of single-phase voltage signal using fixed delay (FD) technique.

It is worth noting that, if the input voltage signal can be normalized then the frequency can be estimated using only signal s1(n) by approximating the $\sin^{-1} x \cong x$ under the condition that

sampling frequency ($f_s = \frac{1}{T_s}$ =10 KHz) > 8 times the fundamental frequency (f =50 Hz) and as given by

$$f_g = f_{FD} = \frac{1}{2 \times \Pi \times T_s} \times \sqrt{[V_{\alpha 1pu}(n)^2 - V_{\alpha pu}(n) V_{\alpha 2pu}(n)]} \tag{4.27}$$

Normalization Method-2 is chosen over *Normalization Method-1* to provide priority to faster estimation with lower overall computational complexity to normalize $V_\alpha(n)$ and (4.27) is followed to estimate the frequency as an alternative way as shown in Figure 4.20.

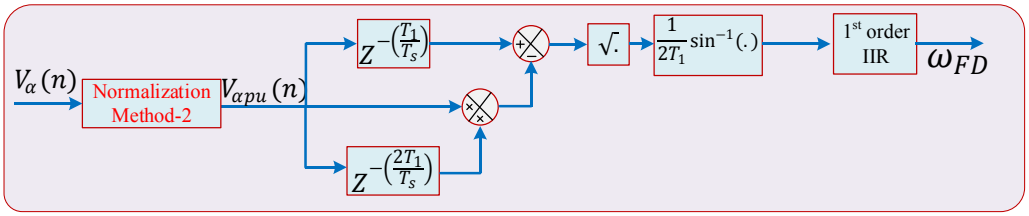


Figure 4.20: Approximated model of frequency estimation of single-phase voltage signal using fixed delay (FD) technique.

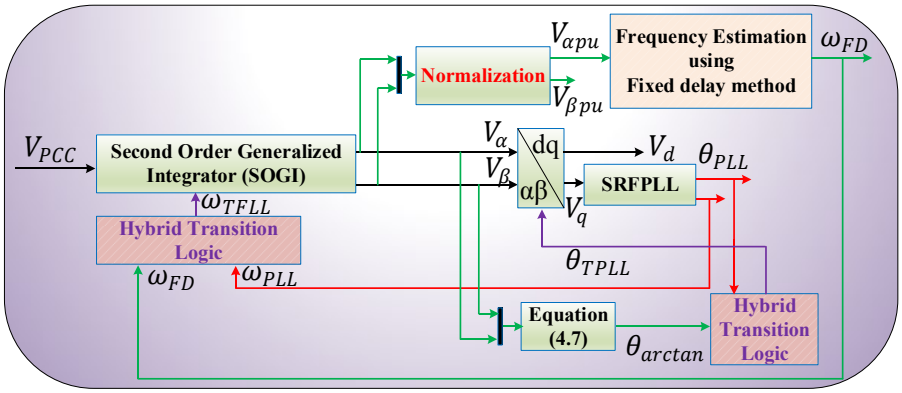


Figure 4.21: Hybrid Frequency adaptive SOGI using frequency estimation by the combination of SOGI BPF and fixed delay method during grid faults.

As per the hybrid grid synchronization principle, the frequency estimation using the fixed delay technique will only be used to provide robustness to PAJ during grid faults. During the normal grid operating condition, the frequency and phase-angle estimation will be switched back to the SRFPLL estimation. The complete hybrid frequency adaptive and phase-angle fed SOGIPLL is shown in Figure 4.21.

4.4 Proposed Transition Framework for Hybrid Grid Synchronization

In Section 4.3, it is observed that to cope with the spurious PAJ during a grid fault, faster phase-angle and frequency estimation techniques are proposed to provide an efficient grid synchronization and robust converter controller performance during FRT. On the contrary, during normal operating conditions (no Fault), the frequency and phase-angle estimations are switched back to the SRFPLL technique. A smooth transition framework as discussed below is therefore required.

The flow chart of the proposed transition framework is shown in Figure 4.22. The phase-angle error ($\Delta\theta_{limit}$) limit is initialized at first. The phase-angle difference between the SRFPLL estimated phase (θ_{PLL}) in the dq-frame and arctangent estimated phase (θ_{arctan}) in the αβ-frame is calculated. The phase error ($\Delta\theta_{err}$) is compared with the $\Delta\theta_{limit}$, which is set as $\pm 7^0$ [144]. As soon as PAJ occurs due to the grid faults and $\Delta\theta_{err}$ exceeds $\Delta\theta_{limit}$ in the rising slope, the counter (t_{cnt}) counts for 10 samples (i.e. $t_{d1} = 10T_s$). If the error still exits, then the first transition process is enabled. During this transition, the phase-angle required for the frame transformation and current controller will switch from SRFPLL to the arctangent based phase estimation. Once the fault is cleared, and $\Delta\theta_{err} \approx 0^0$, the second transition is activated. Before switching back to SRFPLL during second transition, the counter $t_{d2} = t_d$ is delayed for at least the settling time of the SRFPLL to ensure smooth recovery of the phase estimation from arctangent to the SRFPLL in the steady-state. An instance of such phase-angle transition is shown in Figure 4.23. During the same transition time, the frequency estimation changes from SRFPLL to the open-loop (PLL independent) techniques. During the transition, instead of directly switching between the phase-angle and frequency estimation techniques, two weight functions (w_1 and w_2) are defined to act as

gains for the two estimated phase-angles i.e. SRFPLL and arctangent. w_1 and w_2 are two positive and negative ramp functions ranging from 0 to 1, which decide the transition time for the hybrid synchronization technique. During the occurrence of grid fault having PAJ, the converter is switched to the LVRT mode following the proposed hybrid grid synchronization transition.

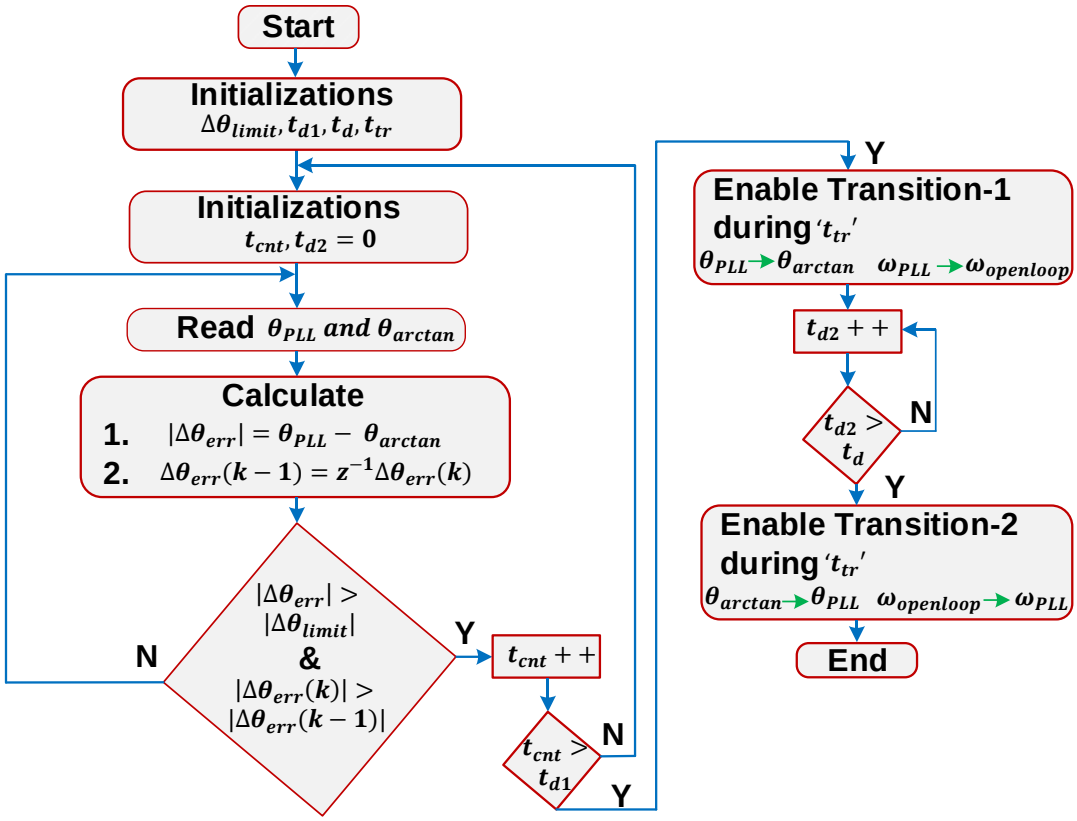


Figure 4.22: Flow chart for the proposed phase-angle transition based hybrid grid synchronization.

The mathematical expression for the phase-angle required for frame transformation as well as current controller operation (θ_{TPLL}) as a function of weighted θ_{PLL} and θ_{arctan} is given by

$$\theta_{TPLL} = w_1(kT_s)\theta_{PLL} + w_2(kT_s)\theta_{arctan} \tag{4.28a}$$

Similarly the frequency (resonant frequency) (ω_{TFLL}) required for the SOGI /DSOGI based pre-filter is estimated by the combination of ω_{PLL} and $\omega_{openloop}$ as given by

$$\omega_{TFLL} = w_1(kT_s)\omega_{PLL} + w_2(kT_s)\omega_{openloop} \tag{4.28b}$$

The $\omega_{openloop}$ is referred here as any one of the techniques (e.g. arctan derived (in $\alpha\beta$-frame) for both three-phase and single-phase, teager energy operator and fixed delay method for single-phase grid-connected converter applications) provided in Section 4.3.

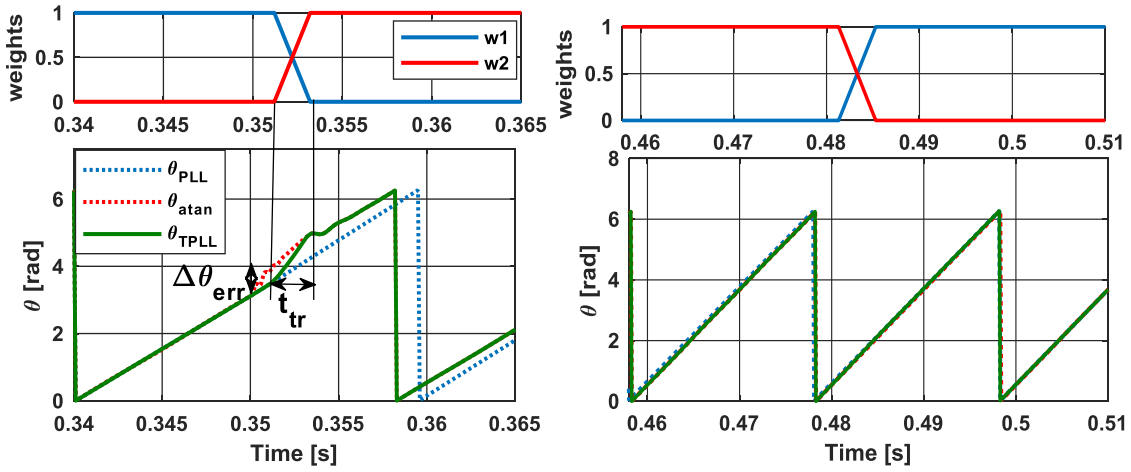


Figure 4.23: Instance of phase-angle transition between SRFPLL and Arctangent.

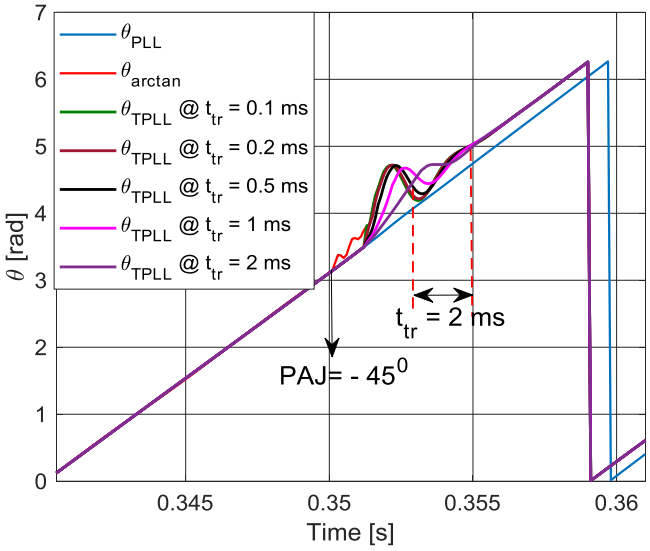


Figure 4.24: Transition framework for the proposed hybrid grid synchronization technique with various transition times (t_{tr}) during -45° PAJ.

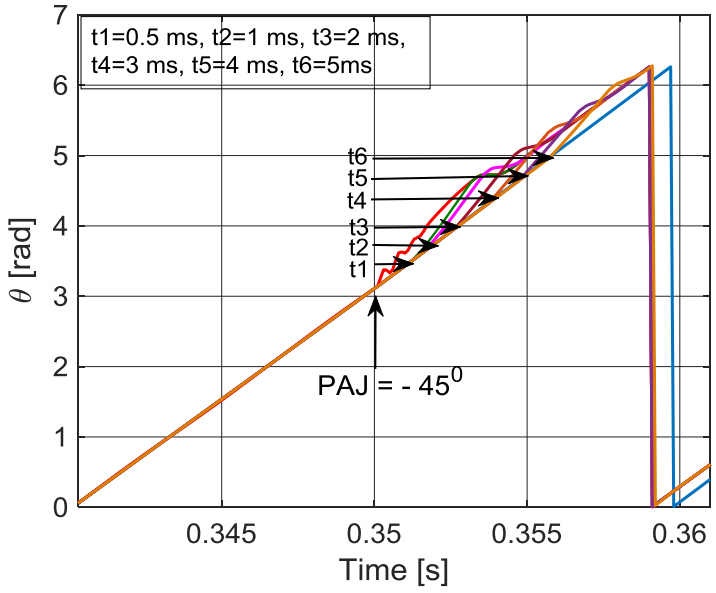


Figure 4.25: Transition framework for the proposed hybrid grid synchronization technique with various counter times (t_{cnt}) during -45° PAJ.

In (4.28), the relation between the two weight functions is, $w_2(kT_s)$ = 1-$w_1(kT_s)$. The value of k can be decided depending on the transition time set for the proposed technique. The value of T_s is kept the same as sampling time, i.e., 0.1ms. The value for k is varied between 1

to 20, which implies a variation in the transition time (t_{tr}) from 0.1 ms to 2 ms respectively as shown in Figure 4.24. All the tests are performed with a transition time of 2 ms to ensure a smooth transition. Higher transition time is not suitable for the current controller to respond during grid voltage PAJs. Similarly, an observation is made with varying the counter time (t_{cnt}) from 0.5 ms to 5 ms during the occurrence of the PAJ (fault inception point) as shown in Figure 4.25. The t_{tr} is maintained at 2 ms for all of the t_{cnt}. It is noticed that the sum of counter time and transition time ($t_{cnt} + t_{tr}$) should be selected in such a way that the transition process will avoid discontinuity of sawtooth wave (phase-angle with modulo 2π). Simulation is done by considering the transition at the discontinuity point and a worst case scenario in terms of overshoots in the current controller is observed. The values chosen for $t_{cnt}= t_{d1}$ and t_{tr} in this work are 1 ms and 2 ms respectively considering the PAJ occurs at π radian points of the sawtooth wave as shown in Figure 4.24.

Such transition between the two phase estimation techniques (SRFPLL and arctangent) can help the converters to operate robustly during grid faults as compared to the SRFPLL technique, which delays the phase estimation for more than 100 ms. The converter's current controller performance during FRT when subjected to various PAJ as a result of grid fault (both symmetrical and asymmetrical) using the proposed hybrid grid synchronization technique will be detailed in Chapter-5 (three-phase converter) and Chapter-6 (single-phase converter).

4.5 Benchmark of Hybrid Grid Synchronization Performance

The performance of the proposed hybrid grid synchronization transition is tested by using both simulation and selected real time experiments. Grid synchronization performance of three-phase and single-phase grid connected applications are discussed separately.

For benchmarking the performance of the proposed hybrid grid synchronization in the context of three-phase grid-connected application, other PLL techniques are implemented. They include: i) the conventional second-order SRFPLL, ii) first-order SRFPLL and, iii) freeze PLL. It has already been proven that the first-order SRFPLL outperforms the other adaptive gain tuning of the PLL during grid faults having PAJ (discussed in sub-section 4.2.1). The test scenarios chosen for comparison are: a) Non-severe symmetrical fault with PAJ (60% sag and -45° PAJ), b) Severe symmetrical fault with PAJ that leads to loss of grid synchronization (90% sag and -45° PAJ) and c) asymmetrical fault with PAJ (90% sag in phase-B and phase-C with -45° PAJ). During asymmetrical fault, DSOGI pre-filter is used to extract the positive sequence of the unbalanced grid voltage. The resonant frequency of the DSOGI is made adaptive with hybrid frequency estimator during fault.

In the single-phase grid connected applications, the performance is compared with the SOGIPLL technique. Test cases chosen are: i) 60% sag, ii) -45° PAJ, iii) frequency variations, iv) addition of DC offset and v) addition of lower order harmonics in the voltage. Initially, the performance of the proposed improved frequency-adaptive SOGI is compared with the conventional SOGIPLL during the above grid conditions. Then the transition scheme of the proposed hybrid grid synchronization is applied considering a symmetrical fault (60% sag and -45° PAJ simultaneously). During the fault, the transition dynamics among the hybrid frequency and phase-angle estimators are compared with the SOGIPLL. The resonant frequency of the SOGI BPF is tuned with the proposed phase-angle decoupled frequency

estimators during the fault under the hybrid grid synchronization principle such as a) estimation using Teager Energy Operator and b) estimation using Fixed Delay method.

4.5.1 Benchmark of Three-phase Hybrid Grid Synchronization Performance

Case A: Non-severe Symmetrical Fault with PAJ

The symmetrical fault occurs at the grid voltage (V_g) between time t = 0.35 s and t = 0.55 s. The sag depth generated is 60% of the rated voltage. PAJ of -45° is added to the fault inception and recovery point. The three-phase voltage measured at the PCC (V_{PCC}) is fed to the grid synchronization unit. The parameters plotted for comparison are $\alpha\beta$-and dq-components of V_{PCC}, estimated frequency and phase-angle. The grid synchronization dynamics for the conventional second-order SRFPLL is shown in Figure 4.26 (a). The synchronization delay observed at the event of fault is 120 ms which is typically the settling time of the PLL. The damping ratio is set to 0.707. Such low damping ratio results in oscillating frequency. For the first-order SRFPLL, such oscillations are absent as shown in Figure 4.26 (b). This is due to the fact that, the first-order SRFPLL provides infinite damping ratio (K_{IPLL} = 0) during grid fault while the settling time remains the same as 120 ms. The proportional gain of the PLL (K_{PPLL}) is not affected by switching from second-order SRFPLL to first-order SRFPLL during the fault. The dynamics of freezing PLL is shown in Figure 4.26 (c). Due to the deactivation of PLL block, it is unable to track the PAJ. This leads to the steady-state error in V_q during the fault. The steady-state error in the estimated phase-angle (θ_{PLL} (Freeze)) is shown in Figure 4.26 (c). In contrast, the proposed hybrid synchronization technique quickly synchronizes with the grid after a PAJ during grid fault and avoids PLL settling time as shown in Figure 4.26 (d) (refer θ_{TPLL} in the Figure).

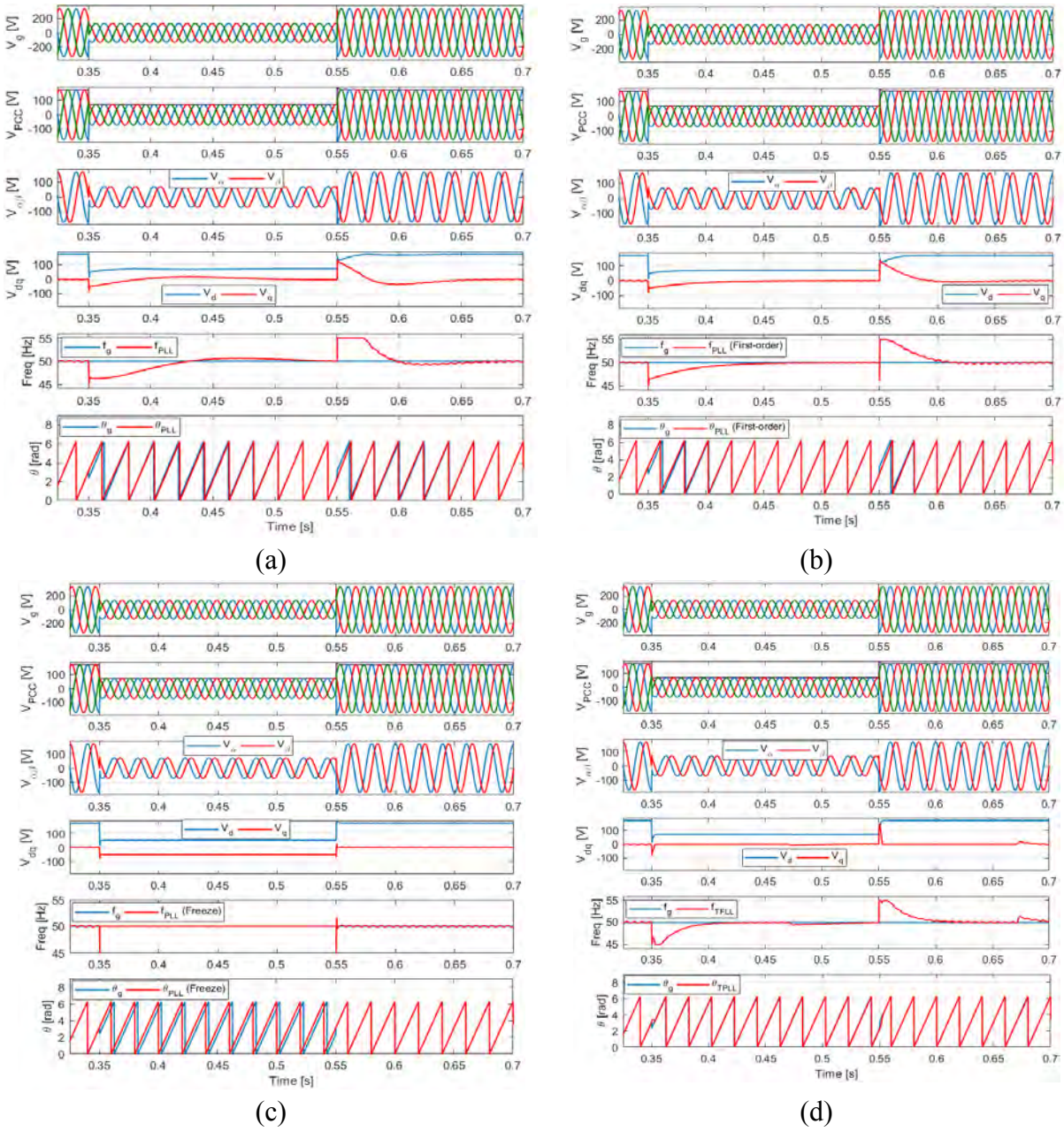


Figure 4.26: Grid synchronization performance comparison during 60% symmetrical sag with -45° PAJ, (a) conventional second-order SRFPLL (b) first-order SRFPLL (c) Freeze PLL and (d) proposed hybrid grid synchronization transition.

Case B: Severe Symmetrical Fault with PAJ

The performance comparison of various grid synchronization techniques during a severe symmetrical fault (90% sag with -45° PAJ) are presented in Figure 4.27.

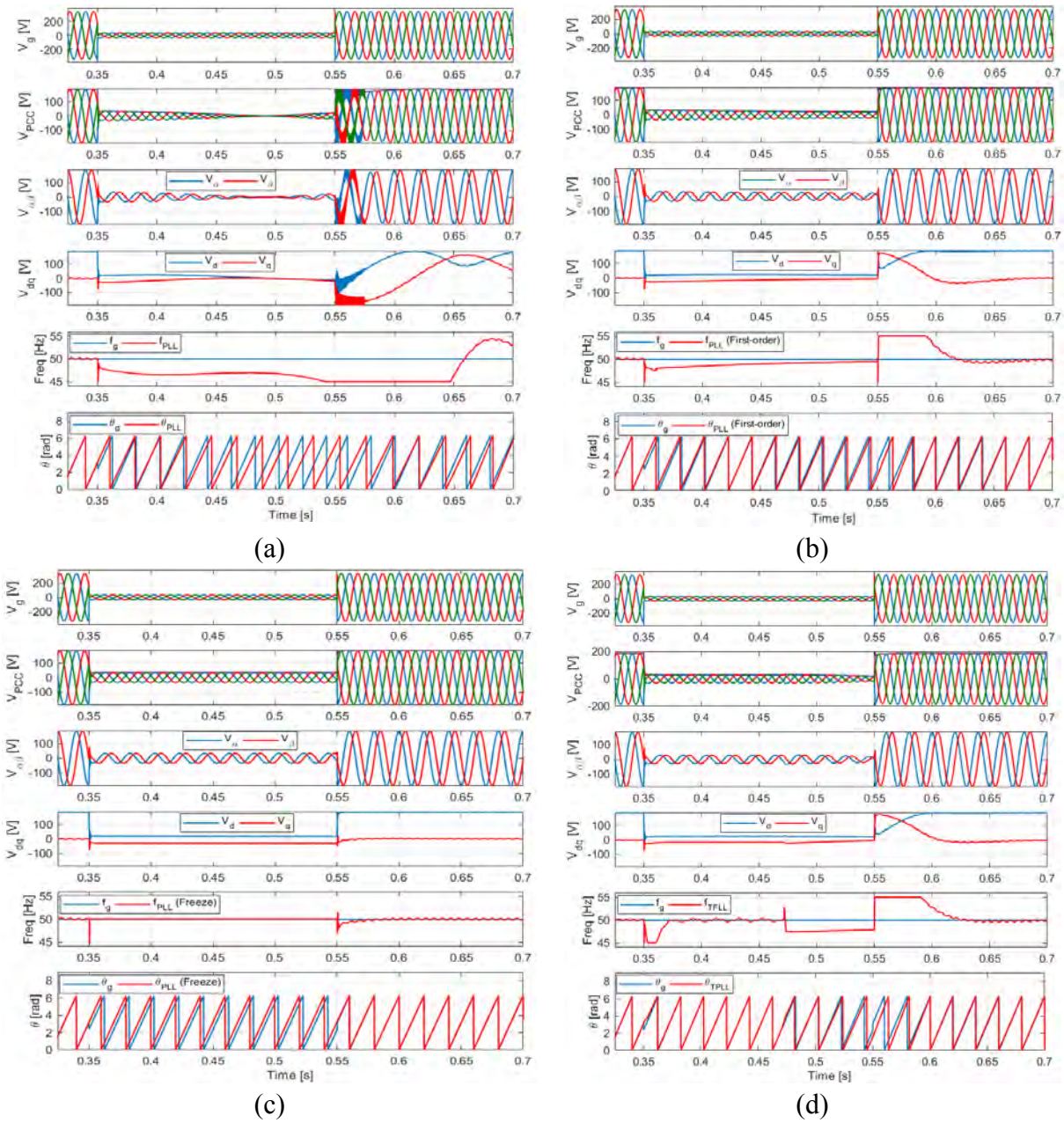


Figure 4.27: Grid synchronization performance comparison during 90% symmetrical sag with -45° PAJ, (a) conventional second- order SRFPLL (b) first-order SRFPLL (c) Freeze PLL and (d) proposed hybrid grid synchronization transition.

Such a severe fault leads to loss of grid synchronization in case of second-order SRFPLL due to insufficient damping factor (0.707) as shown in Figure 4.27 (a). The lower level of saturation for estimated frequency for all the grid synchronization technique is set to 45 Hz while the upper limit is 55 Hz. The first-order SRFPLL shows an improvement to LOS with improved damping ratio as shown in Figure 4.27 (b). The freezing PLL behaves the same way as observed during non-severe symmetrical and PAJ and the response is shown in Figure 4.27 (c). The proposed hybrid technique is observed to smoothly transit during the fault inception and recovery (refer Figure 4.27 (d)). On the transition back to second-order SRFPLL during the fault period, it is observed to follow the uncontrolled SRFPLL frequency for a period of 80 ms until the fault recovery happens at the end of 200 ms duration i.e. at t = 0.55 s. Such ill condition during the severe symmetrical fault can be avoided by adding an adaptive damping technique in addition to the proposed hybrid grid synchronization technique which is not within the scope of this thesis.

Case C: Asymmetrical Fault with PAJ

The dynamic performance comparisons during the asymmetrical fault are shown in Figure 4.28. As mentioned earlier, frequency adaptive DSOGI pre-filter is used to extract the positive sequence component of the unbalanced three-phase voltage during the fault. As anticipated, the conventional DSOGIPLL exhibits the poorest performance among all of the techniques which is shown in Figure 4.28 (a). The frequency dynamics of the first-order SRFPLL is observed to be faster with improved damping during asymmetrical fault as noticed in Figure 4.28 (b). Freezing PLL results in a steady-state frequency error as shown in Figure 4.28 (c) (refer ${\theta_{PLL}}^{+}$ (Freeze) in the figure). In contrast, the proposed frequency-adaptive DSOGIPLL with hybrid grid synchronization principle provides a robust dynamic

performance in terms faster settling time with adequate damping during both the inception and recovery of the asymmetrical fault with PAJ as shown in Figure 4.28 (d).

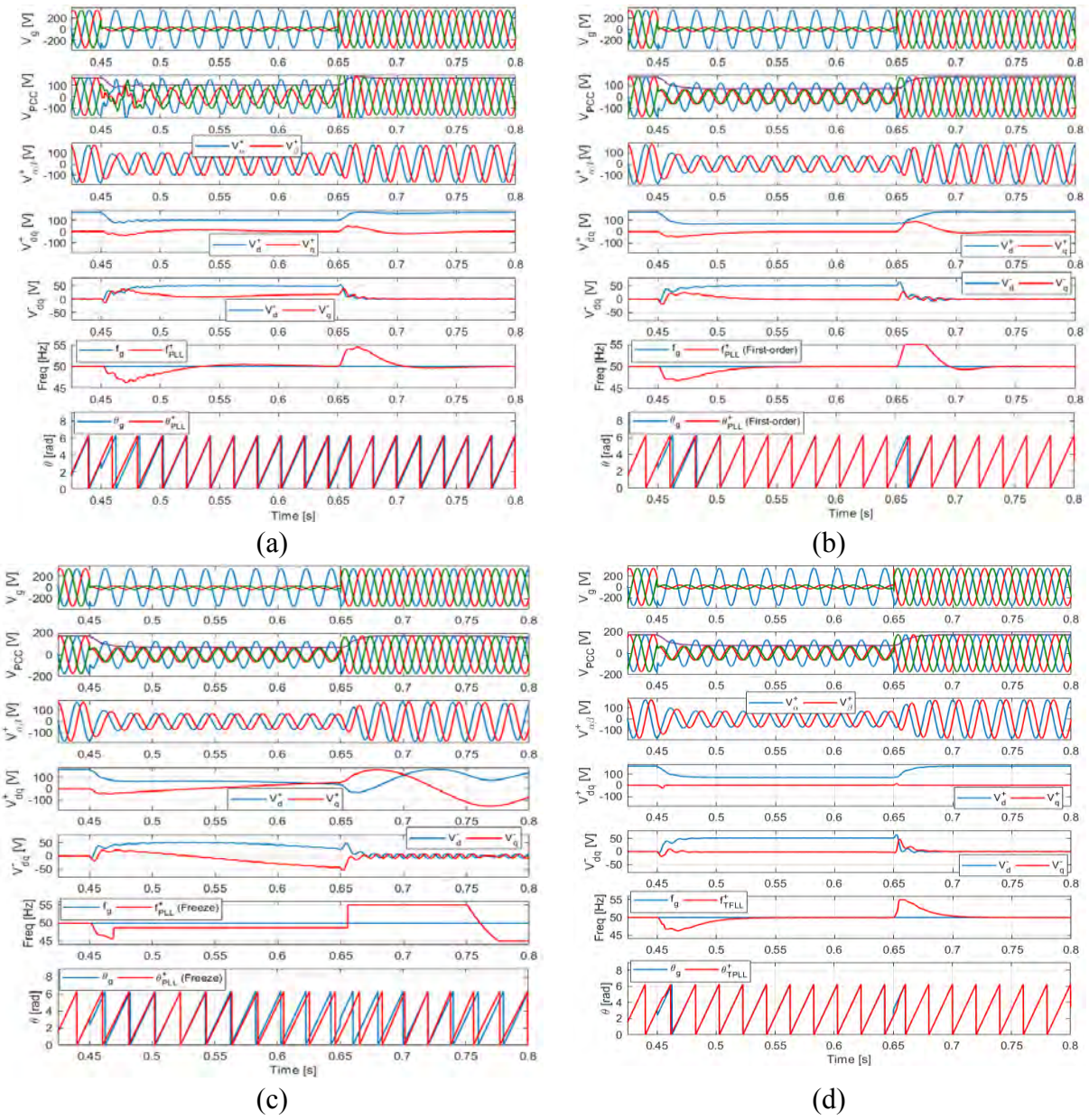


Figure 4.28: Grid synchronization performance comparison during asymmetrical sag (90% sag in phase-B and phase-C) with -45° PAJ, (a) conventional second-order SRFPLL (b) first-order SRFPLL (c) Freeze PLL and (d) proposed hybrid grid synchronization transition.

Case D: Selected Experimental Results

The grid synchronization performance of the proposed hybrid synchronization technique is compared with other grid synchronization techniques using real time experiments. The laboratory set up used for experiments is provided in the Appendix. The fault created is a non-severe symmetrical fault which contains 60% symmetrical voltage sag at the grid voltage along with -45° PAJ. The fault duration is 150 ms which is typically a low-voltage ride-through period.

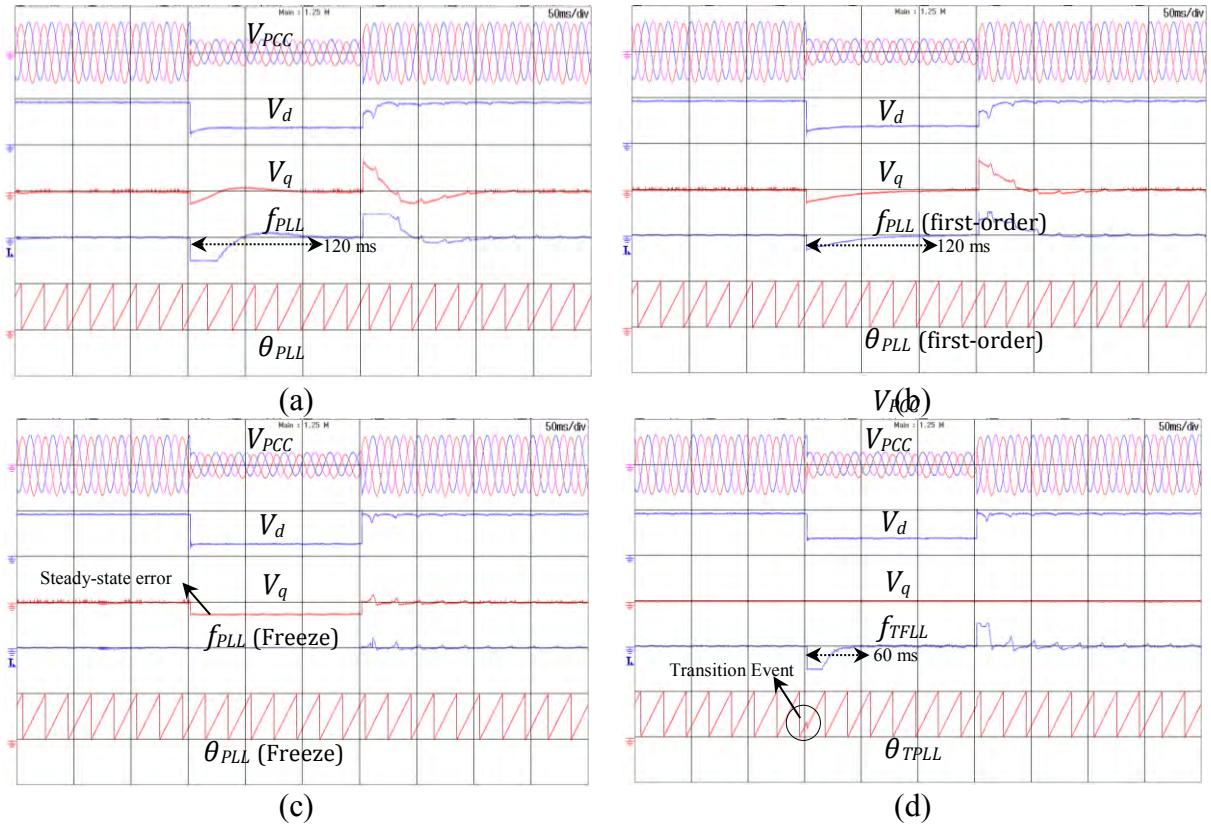


Figure 4.29: Experimental validation of the grid synchronization performance comparison during 60% symmetrical sag with -45° PAJ, (a) conventional second-order SRFPLL (b) first-order SRFPLL (c) Freeze PLL and (d) proposed hybrid grid synchronization transition.

The performance of the second-order SRFPLL is shown in Figure 4.29(a). The settling time is observed to be 120 ms that matches with simulation results. The dynamics of first-order SRFPLL and freezing PLL is shown in Figure 4.29 (b) and (c) respectively. The proposed

hybrid grid synchronization performance is presented in Figure 4.29 (d). The experimental results are found to match with obtained simulation analysis done in *Case A*.

4.5.2 Benchmark of Single-phase Hybrid Grid Synchronization Performance

A. Simulation Results

The performance of the conventional SOGIPLL is compared with the adaptive SOGIPLL in which the three types of frequency estimators are used to feed the SOGI BPF. The first one is using TEO with the "*Normalization Method -1*" (nor-1), second is with "*Normalization Method -2*" (nor-2) and the third one is frequency estimation using fixed delay (FD) technique with "*Normalization Method -2*" (nor-2) . Initially, their transient performances are evaluated as shown in Figure 4.30 (a). The transient events are: 60% voltage sag at t = 0.25 s, -45° PAJ at t = 0.5 s and frequency variations of +1 Hz at t = 0.8 s. All the techniques exhibit maximum impact during the PAJ. The settling time is highest for the conventional SOGIPLL (more than 100 ms) during all the transient events and it is observed to be the lowest for SOGI+TEO (nor-2) technique (around 40 ms). The frequency overshoot during the PAJ for both SOGI+TEO (nor-2) and SOGI+FD (nor-2) technique are around 8 Hz. For conventional SOGIPLL and SOGI+TEO (nor-1) frequency overshoots are around 9 Hz and 5 Hz respectively. As shown in Figure 4.30(b), with the addition of lower-order harmonics in the measured voltage (10% THD), the SOGI+TEO (nor-1) provides the robust estimation performance. The SOGI+TEO (nor-2) and SOGI+FD (nor-2) are affected equally with harmonically polluted grid voltage. Conventional SOGIPLL's harmonic rejection capability is observed to be better than SOGI+TEO (nor-2) and SOGI+FD (nor-2) and less than SOGI+TEO (nor-1) technique. This is because SOGI+TEO (nor-1) use an additional BPF formed by the cascade combination of RDFT and IRDFT as discussed previously.

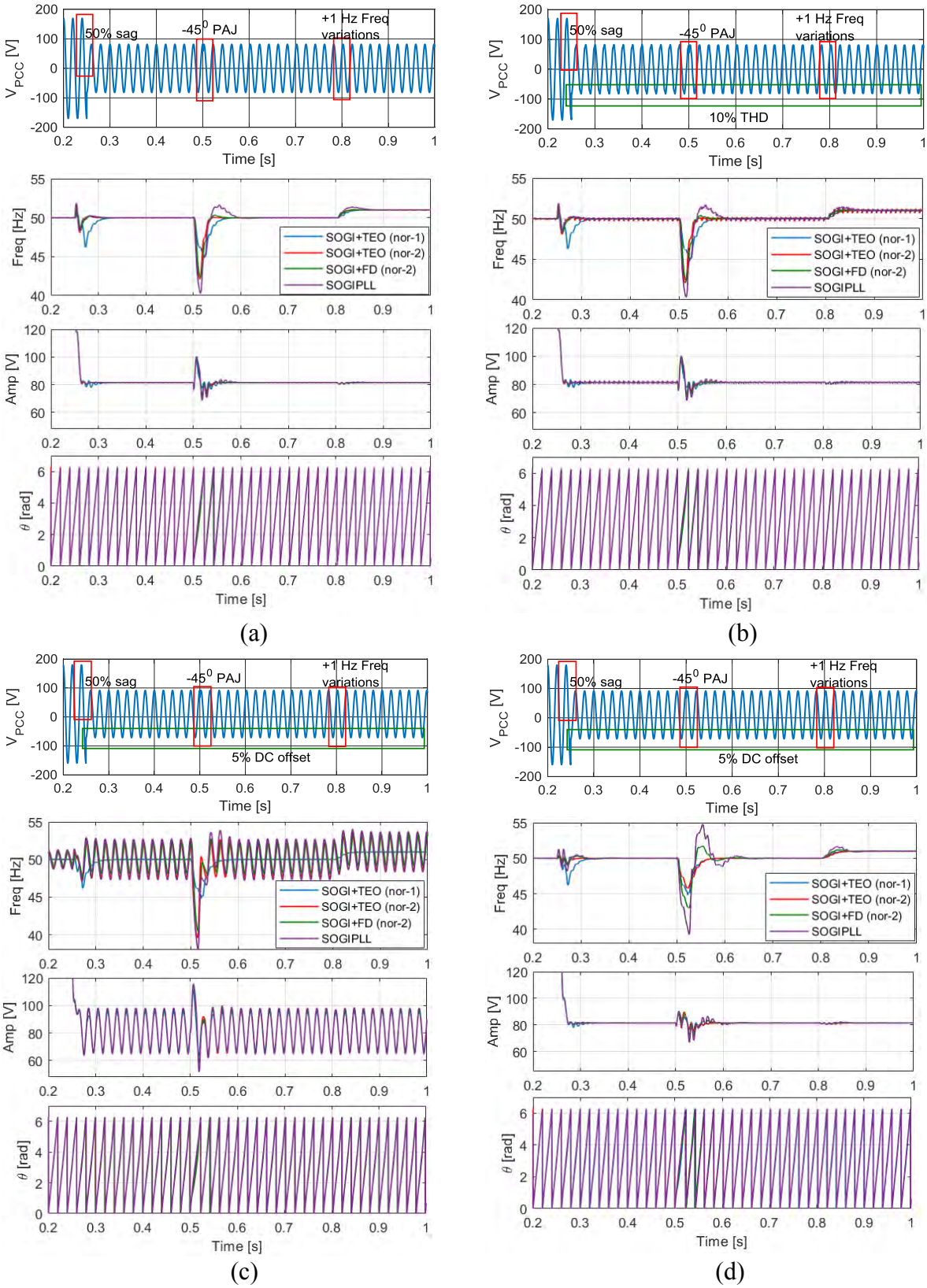


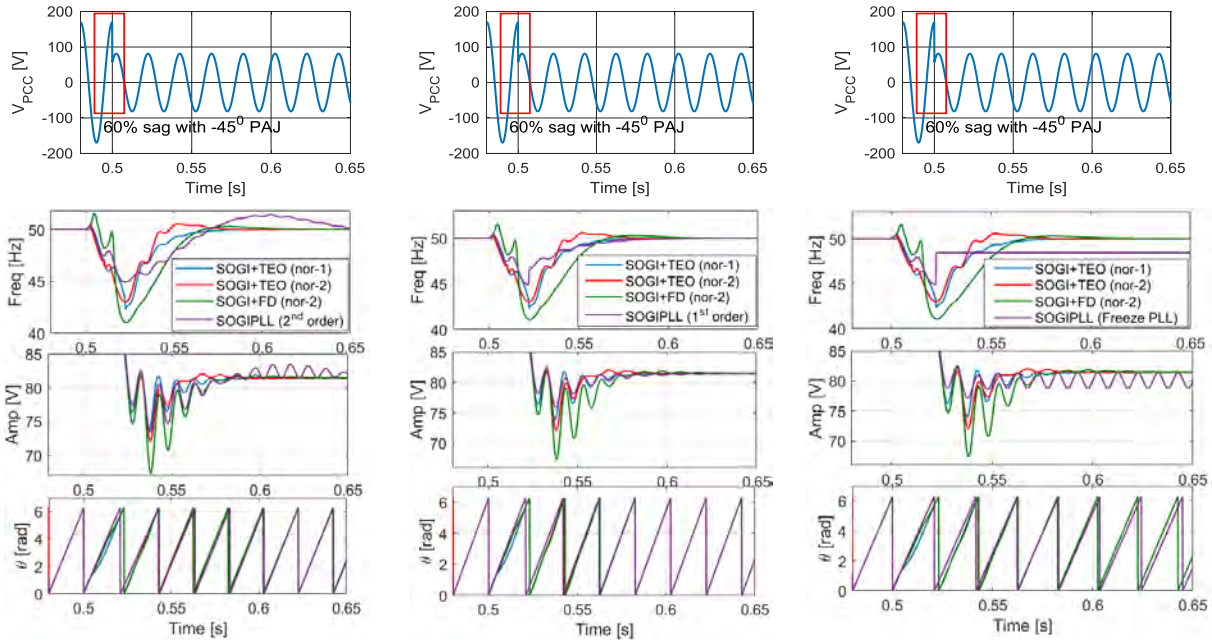
Figure 4.30: Single-phase grid synchronization performance comparisons by adding (a) transients (60% sag at t = 0.25 s, -45° PAJ at t = 0.5s and +1 Hz frequency variations at t = 0.8 s) (b) harmonics (lower-order with 10% THD) (c) 5% DC offset and (d) 5% DC offset with the use of DSC.

Similarly, with the addition of 5% DC offset in the measured voltage, the conventional SOGIPLL, SOGI+TEO (nor-2), and SOGI+FD (nor-2) are noticed to contain ripples in the estimated frequency (refer Figure 4.30 (c)). Moreover the estimated amplitudes by all the four techniques are equally affected by the presence of DC offset. With the use of ½ fundamental period delayed signal cancellations (DSC) filter at the SOGI output, the problem is mitigated as shown in Figure 4.30 (d). The DSC filter is made frequency-adaptive with the estimated frequency to avoid any phase-angle offset during off-nominal frequency variations.

This thesis is more focused on the impact of short-term grid faults (voltage sag with PAJ) on conventional SOGIPLL and improvement with hybrid grid synchronization. Hence, in the second part of performance benchmarking, the hybrid grid synchronization transition principle is investigated in single-phase systems. The adaptive techniques chosen are first-order SRFPLL with SOGI, and freeze PLL with SOGI. These techniques are compared with the conventional SOGIPLL and the proposed adaptive SOGI techniques during the occurrence of a fault having 60% voltage sag and -45° PAJ at t = 0.5s. During the PAJ associated fault, the frequency and phase-angle estimation for SOGIPLL is switched to the proposed adaptive frequency estimators (e.g., Teager Estimator and FD technique based estimator) and arctangent based phase-angle under the hybrid grid synchronization principle.

The comparison of conventional SOGIPLL with the proposed adaptive techniques (SOGI+TEO (nor-1), SOGI+TEO (nor-2) and SOGI+FD (nor-2)) is shown in Figure 4.31 (a). Similarly, the comparison of SOGI + first-order SRFPLL and SOGI + freeze PLL with the proposed technique are shown in Figure 4.31 (b) and (c) respectively. Out of all these comparisons, it is observed that adaption to first-order SRFPLL from second-order PLL with conventional SOGI performs almost equally as compared to SOGI+TEO (nor-1), and SOGI+TEO (nor-2) in terms of overshoot and settling time of the frequency estimation

during the fault occurrence. The SOGI+FD (nor-2) technique is observed to show a delayed response but it is faster than the conventional second-order SOGIPLL. As anticipated, for SOGI + freeze PLL there is a steady-state error observed in the estimated frequency due to PAJ and erroneous frequency when fed to SOGI BPF providing oscillatory behaviour in the estimated amplitude.



(a) (b) (c)

Figure 4.31: Grid synchronization performance comparison of the proposed frequency-adaptive SOGI during 60% symmetrical sag with -45° PAJ, with respect to (a) conventional second-order SRFPLL (b) first-order SRFPLL (c) Freeze PLL.

B. Selected Experimental Results

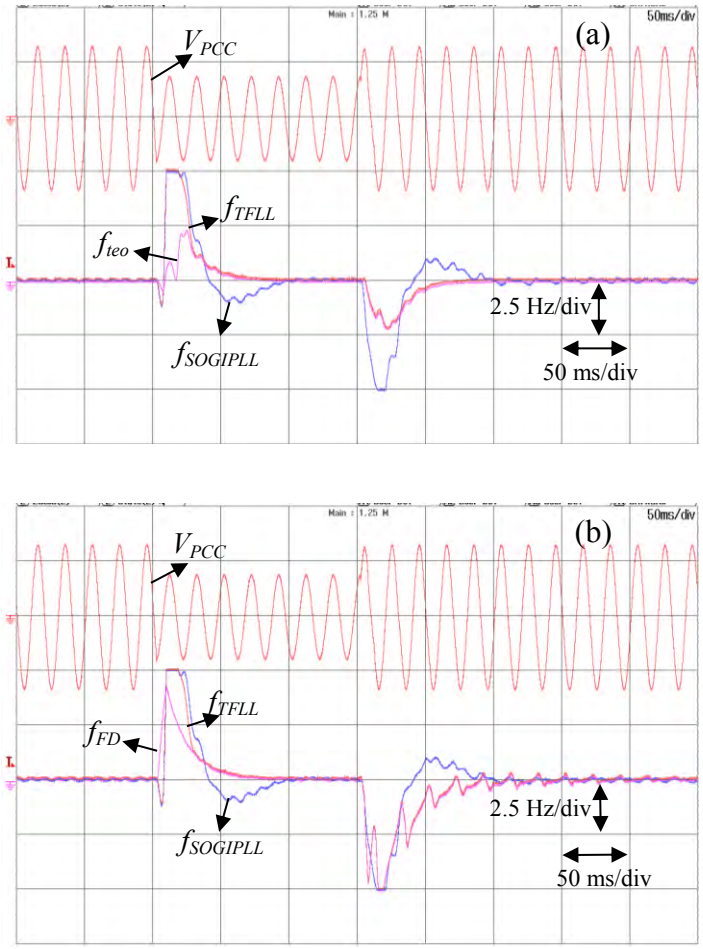


Figure 4.32: Experimental validation of frequency transition from conventional SOGIPLL to (a) Teager estimation and (b) FD technique based estimation using the proposed hybrid grid synchronization transition principle.

The experimental validation of the transition of the conventional SOGIPLL frequency estimation to teager frequency estimation and to Fixed Delay technique based estimation is shown in Figure 4.32(a) and Figure 4.32(b) respectively. The experiential set up is briefed in the appendix. The considered fault is 50% sag and 45° PAJ in the voltage for duration of 150 ms. The transition happens under the proposed hybrid grid synchronization principle explained for three-phase systems previously.

The FRT behaviour of single-phase grid connected converter using the proposed adaptive and hybrid single-phase grid synchronization techniques will be discussed in Chapter-6.

4.6 Chapter Summary

This chapter summarizes the adaptive and hybrid grid synchronization techniques applicable for three-phase and single-phase grid connected converter operation. It begins with the insight to various existing adaptive grid synchronization techniques for three-phase grid-connected converters. The adaptation is done by modifying the second-order SRFPLL depending upon the grid fault conditions. The objective of these techniques is to provide faster settling time and adequate damping during any PAJ associated severe grid fault that may create the loss of synchronization issue for the converters. The limitations of these techniques are highlighted as well.

In contrast, a hybrid grid synchronization transition technique is proposed which includes hybrid phase-angle and frequency estimation. The hybrid phase-angle estimator uses the arctangent based phase-angle estimation for grid synchronisation when the grid voltage faces a PAJ during either symmetrical or asymmetrical faults. The peculiarity of the proposed hybrid estimator is that it provides faster estimation by avoiding the design trade-off of SRFPLL loop gain. Upon the recovery of the fault; it switches back to the SRFPLL estimations to get advantageous features such as accurate frequency tracking and harmonic rejection capability.

Moreover, during asymmetrical fault and PAJ, the frequency adaptability of the DSOGIPLL is enhanced by the hybrid frequency estimator that uses the arctangent derived frequency instead of the SRFPLL estimation. On the recovery of the fault, the frequency estimation again switches back to the SRFPLL estimation. It is observed that such hybrid frequency estimators enhance the frequency adaptability of the conventional DSOGIPLL. They are controlled by a common phase-angle error based bump-less transition framework.

For single-phase grid-connected converter application, the frequency dependency of SOGI BPF on the SRFPLL estimation is replaced during the PAJ associated grid fault by proposing two frequency estimators excluding the arctangent derived frequency. The estimators are Teager Energy Operator and Fixed Delay method. These estimators take the SOGI BPF in-phase component of the single-phase voltage signal to estimate the frequency. Such implementation enhances the frequency adaptability of the SOGI by avoiding the dependency of PLL loop gains. The phase-angle is estimated using the arctangent function on the in-phase and quadrature phase signals of the improved frequency-adaptive SOGI BPF. Similar to the concept applied in three-phase system, such improved frequency and phase-angle estimators use the principle of the proposed hybrid grid synchronization transition.

In the final part of this chapter, a benchmarking of the proposed hybrid grid synchronization transition technique is carried by using both simulation and real time experiments. The comparisons are done separately for three-phase and single-phase techniques. For three-phase comparisons, other existing techniques such as first-order SRFPLL, freezing PLL are considered in addition to second-order SRFPLL. For single-phase comparison, the improved frequency-adaptive SOGI techniques are compared with the conventional SOGIPLL during various grid conditions. They include both transients (like voltage sag, PAJ and frequency variations) and steady-state disturbances (like DC offset and harmonics). The transition principle proposed for the hybrid grid synchronization of three-phase converter application is also tested for single-phase configuration.

It can be concluded that for either three-phase or single-phase configuration of the grid-connected converters, the proposed hybrid grid synchronization transition principle provides robust grid synchronization dynamics especially against the grid faults with PAJ. It is expected that this efficient grid synchronization performance will lead to the improved current controller dynamics during FRT of the converters. The FRT of three-phase and

single-phase power converters using the proposed hybrid grid synchronization transition technique will be detailed in Chapter-5 and Chapter-6 respectively.

Chapter 5

Fault Ride-Through of Three-Phase Power Converters

Loss of grid synchronization is one of the major causes for the failure of converters during grid faults. To overcome this issue and to make the converter's current controller robust during faults, this chapter proposes the hybrid grid synchronization transition technique. This transition method is already discussed in Chapter -4. In this Chapter, this transition technique is implemented with the current controller of a three-phase voltage source converter. The current controller using the hybrid grid synchronization is implemented both in the synchronous reference frame (*dq*-frame) and stationary reference frame (*αβ*-frame). The performance of the converter during both symmetrical and asymmetrical grid faults along with the fault ride-through strategies is tested by both simulations and experiments.

5.1 Introduction

Due to the increasing price and environmental pollution issues, fossil fuel based power generation are gaining less importance in recent years. Hence, many countries are switching towards the renewable energy sources (RESs) based power generation. In such cases, the conventional synchronous generators are getting replaced by solar PV and wind energy systems. The RESs use power electronic converters for grid integration purpose. These power

converters poses several risk on the existing power systems due to the lack of inertia. Thus stringent grid codes are being imposed on them by several countries such as provision of the fault ride-through (FRT) during grid fault, and maintaining the power quality of the grid current during normal operating conditions. This chapter focuses on the FRT capability of the power converters.

During FRT, the converters are expected not to trip (stay connected) for a specific pre-defined time duration. The connection/disconnection duration of these converters depends on the amount of voltage drop as a result of faults, which is decided by the low voltage ride-through (LVRT) curve of a specific country. Additionally, the converters supply active and reactive current to the grid during the fault depending upon the grid voltage sag depth. During severe fault, i.e., for sag depths more than 50%, only reactive current is injected by the converters making the active current injection zero.

Large scale solar PV or wind energy systems use three-phase converters (inverters) to inject grid current. During grid faults, current controllers of these converters need to be designed properly to provide enhanced FRT. Most of the industrial converters use either proportional plus integral (PI) current controller in the *dq*-frame or proportional plus resonant (PR) current controller in the $\alpha\beta$-frame. Both these types require either the phase-angle or the frequency information of the grid voltage. Additionally, to provide reactive current, fast and accurate grid voltage amplitude (sag depth) estimation is necessary. All these information are provided by a dedicated synchronization unit for these grid-connected and grid following converters. Inefficient grid synchronization performance may result in poor FRT of the converter due to loss of synchronization (LOS). Recently grid fault as a result of LOS is reported by the North American Electric Reliability Corporation (NERC). According to the report, the LOS of the PLL with the grid during a fault triggered the trip of a 900 MW solar PV plant in Southern California [89]. Other records from industries illustrate that voltage sags of 20-100 ms

duration contribute to 46% of all types of other voltage transients [145]. During such adverse grid scenarios, it has always been a challenge to design an immune, fast, simple and yet robust PLL for the purpose of grid synchronization.

In Chapter-4, the commonly used synchronous reference frame phase-locked loop (SRFPLL) [131], [132] and its variants [53]-[59] are discussed regarding their synchronization performance, when subjected to various grid faults. It is shown there that the PLL based grid synchronization techniques are not suitable for the grid faults with phase-angle jumps (PAJs). Its insufficient damping and higher settling time degrade its synchronization performance during PAJs. Additionally, Chapter-4 detailed the proposed hybrid grid synchronization concept and its synchronization improvements are proven in comparison to PLL based techniques. This chapter will not repeat the synchronization schemes. However, it will use them to design the current controllers.

Apart from the synchronization improvement, adding voltage (at PCC) feedforward compensation terms to the output of the current controller (in case of PI controller in the *dq*-frame) can overcome the negative impact of the PLL dynamics during grid faults. Nevertheless, such feedforward compensation acts as a positive feedback to the closed-loop control of the converters. Hence, it decreases the system stability margin, especially in a weak grid where the grid impedance is of utmost concern [148]-[150]. It also adds harmonics to the current to be injected to the grid as a result of large grid impedance seen at the PCC [151].

5.1.1 Contribution and Organization of this Chapter

This chapter explores the PI and PR current controller design and investigate the FRT performance of the converter during the grid faults. Here, the conventional grid synchronization using PLL is replaced by the proposed hybrid grid synchronization technique. Section 5.2 outlines the reduced order model of the three-phase converter. Section 5.3 provides the insight to the impact of voltage feedforward compensation on the current controller especially in a weak grid during grid faults. In Section 5.4, the model of current controller including grid synchronization dynamics (PLL) is explained. Section 5.5 investigates the Fault Ride-through (FRT) of the power converter during symmetrical and severe symmetrical grid faults having both voltage sag and PAJs. The reactive current injection requirement to meet the grid code is presented. Section 5.6 provides detailed simulation analysis and experimental validations of the proposed hybrid grid synchronised power converter's enhanced FRT operation. Additionally, comparisons with other adaptive grid synchronization techniques are performed based on the dynamics of current controller, DC-link voltage, power profiles (active and reactive) and current injection angle. The adaptability of voltage feedforward compensation in the current controller is tested during the faults as well.

In Section 5.7 special attention is given to the FRT operation during asymmetrical grid faults having PAJs. During the asymmetrical faults, two types of current controllers are implemented such as Proportional plus Integral plus Resonant$_2$ (PIR$_2$) and only Proportional plus Resonant (PR) along with the proposed hybrid grid synchronization technique. The performance comparisons are done in Section 5.8. Lastly, Section 5.9 provides the chapter summary.

5.2 System Description

The overall system description of the grid integration of the DERs is shown in Figure 5.1.

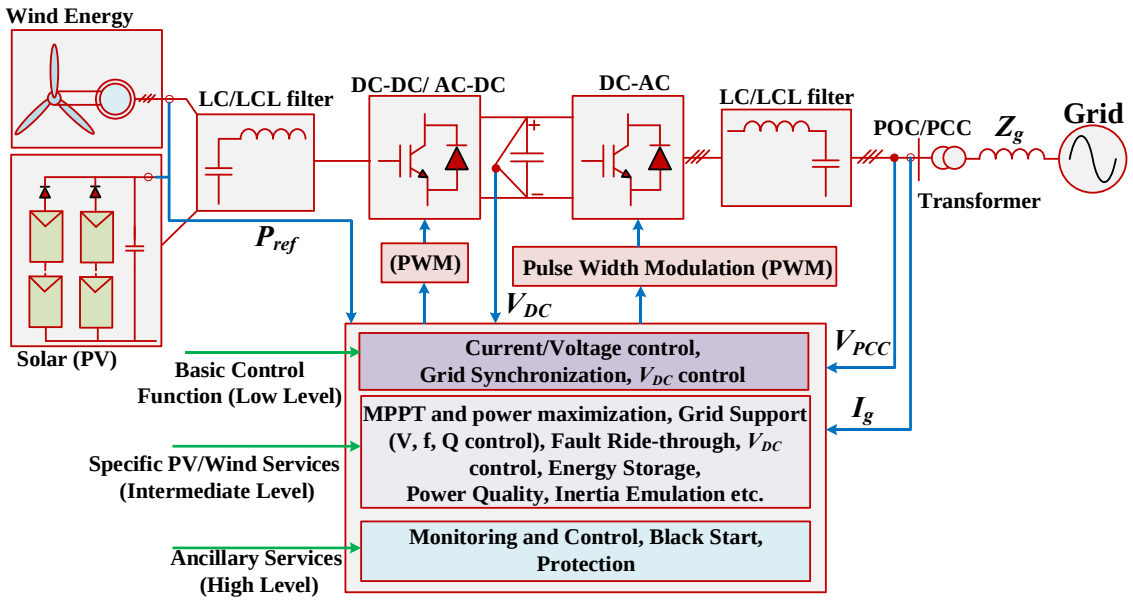


Figure 5.1: Overview of grid integration of distributed energy resources (DERs) and control layers for interfacing power converters.

The DERs shown are wind energy and solar (PV) systems. The power electronic converters are observed to act as the interface between the DERs and the grid. The converters are used as rectifiers (DC/DC) and/or inverters (DC/AC). Inverters are responsible for the grid connections. There are three control layers used during such grid-connected operation such as: (a) basic control as lower level controller, (b) specific control actions required by the solar/wind energy systems as intermediate level controller and (c) ancillary services as the higher level control. The lower level controller includes grid synchronization, inner current control and outer voltage control. The purpose is to inject grid current synchronized with grid voltage. The basic function of intermediate level controller is to extract maximum energy from the large penetration of DERs using MPPT or other power maximization technique. Apart from this, it provides the necessary Fault ride-through capability for power converters

by injecting reactive power following grid codes during grid faults. The outermost or the high level control layer takes care of generation-demand balance, protection schemes and black start functionalities.

In the present study, the detailed model shown in Figure 5.1 is reduced to the Figure 5.2 based on the following assumptions.

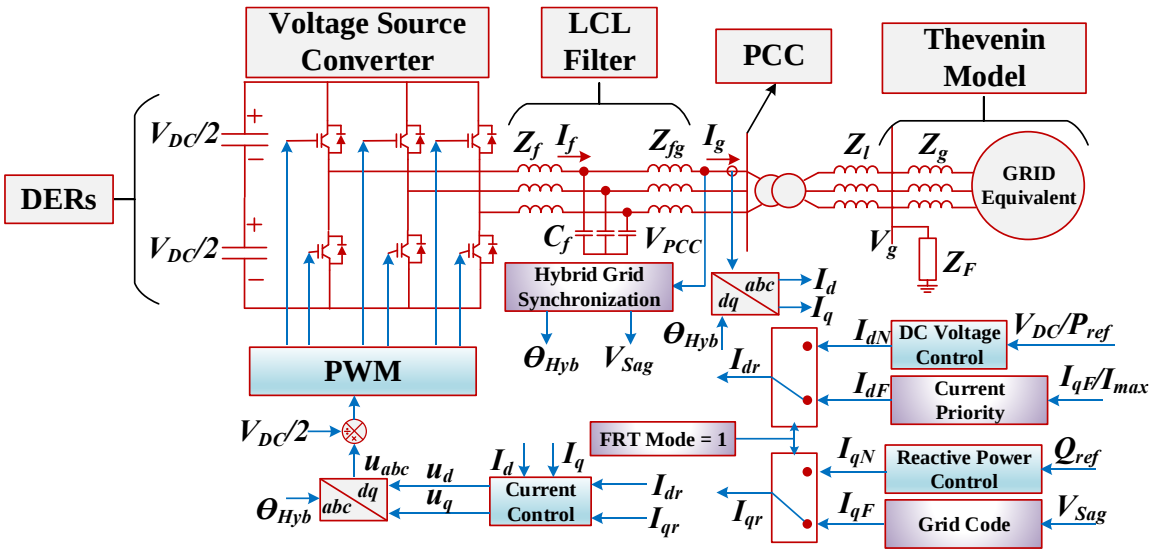


Figure 5.2: Reduced-order model of the grid-connected three-phase power converter.

(a) The interaction between the generator side and grid side converter is replaced by the constant DC-link voltage source. This is done by properly maintaining the DC voltage using the outer loop control.

(b) During any fault, only grid side converter controller dynamics are studied. For instance, current controller as the inner control layer and DC voltage control and/or grid synchronization control as the outer loop control layer.

(c) During the FRT, the reference current generation is decided by the grid code requirement and thus outer control layer is deactivated.

(d) During fault, the power imbalance between the DC side and AC side (active power) is assumed to be dissipated using a chopper circuit (equivalent resistance is interfaced in the DC link) to avoid DC-link overvoltage.

(e) The actual grid is assumed to be a Thevenin equivalent voltage source and the fault is created at the bus connected to the grid voltage. The PCC for the converter is at an electrical distance (line length) from the fault point assuming a radial system.

The schematic of system configuration of a grid-connected three-phase VSC along with its local controller is shown in Figure 5.2. It consists of the plant (LCL filter), grid model (grid voltage with series impedance), grid synchronization unit, DC voltage controller, reactive power controller, the current controller, and the pulse width modulation (PWM) unit. Each controller layer implementation is explained in the following sub-sections.

5.2.1 *LCL* Filter Plant Model

During the integration of DERs to the grid, the interfacing power electronic converters (inverters) use passive filters in order to mitigate the switching harmonics at their output terminal. The harmonics are generated during the PWM control of such inverters. The passive filter can be configured as a simple inductor (*L*) filter (first-order plant model), combination of inductor-capacitor (*LC*) filter (second-order plant model) or combination of inductor-capacitor-inductor (*LCL*) filter (third-order plant model). Compared to *L* and *LC*, *LCL* filter plant model has the superior harmonic attenuation characteristics in the high frequency range [152]. Thus it is mostly preferred for practical grid-connected applications which aim to maintain the total harmonic distortion (THD) below 5% as per IEEE-519 standard [153]. In this work, *LCL* filter is used as the plant model. A typical structure of the plant is given in Figure 5.3.

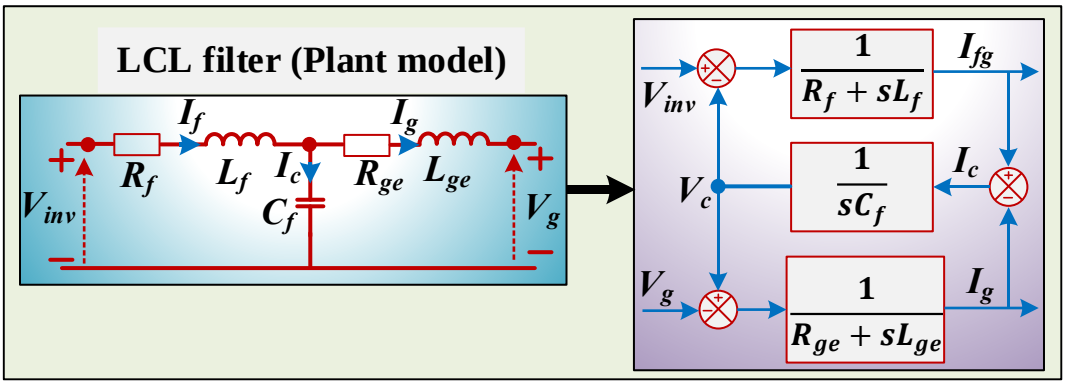


Figure 5.3: LCL filter Plant model for grid-connected inverter application.

The transfer function of the *LCL* filter in the Laplace domain can be derived as the ratio of the superposition of the ratios of grid current (I_g) (a) to the inverter input voltage (V_{inv}) by making the grid side voltage (V_g) as zero and (b) to the grid voltage by making inverter voltage zero as given by

$$I_g = \frac{V_{inv} + V_g(1 + s^2 C_f L_f + sC_f R_f)}{s^3 C_f L_f L_{ge} + s^2 C_f (L_{ge} R_f + L_f R_{ge}) + s(C_f R_f R_{ge} + L_f + L_{ge}) + (R_f + R_{ge})} \quad (5.1)$$

By neglecting the internal resistance of inductor (5.1) can be further simplified as

$$I_g = \frac{V_{inv} + V_g(1 + s^2 C_f L_f)}{s^3 C_f L_f L_{ge} + s(L_f + L_{ge})} \quad (5.2)$$

The resonance frequency (f_{res}) for the *LCL* filter is expressed by

$$f_{res} = \frac{1}{2\pi}\left(\frac{L_f + L_{ge}}{C_f L_f L_{ge}}\right) \quad (5.3)$$

For grid-connected inverter operation, while taking the grid current as feedback control, the resonance frequency is selected as per the thumb rule [154] as $f_b \leq f_{res} \leq \frac{f_{sw}}{2}$, where f_b is the current controller bandwidth ($\cong$ 1 kHz) and f_{sw} is the switching

frequency for the inverter (10 kHz used in this work). In this work, f_{res} is chosen to be 3.7 kHz to avoid any resonance with that of the current controller.

5.2.2 DC-link Voltage Control Loop

The DC-link voltage control is considered as the outer loop control based on control time scale [155]. Its response is slower as compared to the inner current control. This control layer maintains the DC-link voltage (V_{DC}) to its reference value ($V_{DC}{}^{ref}$). Based on the power balance between the DC side and the AC side, the reference current (d-axis) for the current controller is extracted from the output of the DC-link voltage controller. The closed-loop control of DC-link voltage along with the plant model is shown in Figure 5.4. The current controller gain is given by $G_i(s)$).

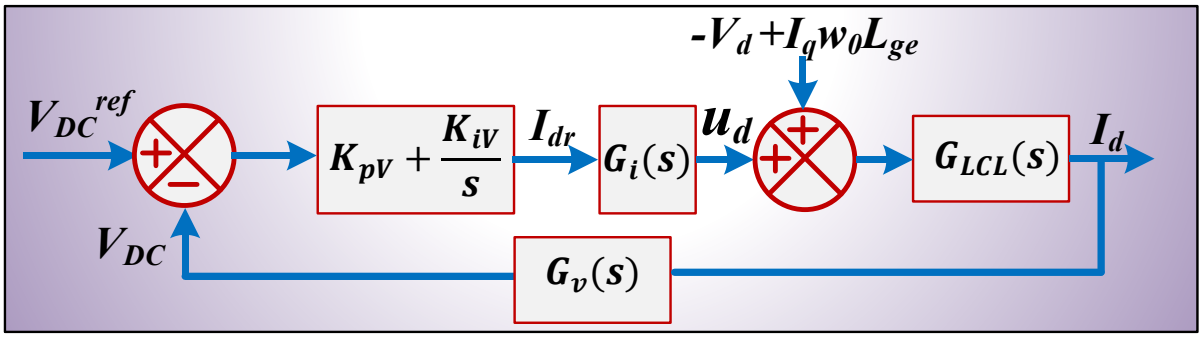


Figure 5.4: DC-link voltage control Loop.

The gain function ($G_v(s)$) shown in the feedback path of the d-axis current is given by

$$G_v(s) = \left(\frac{3V_d}{2V_{DC}{}^{ref} C_{DC} s}\right) \tag{5.4}$$

where V_d is the d-axis voltage component of the PCC voltage and C_{DC} is the DC-link capacitance. The control action is mainly performed using the proportional and integral (PI) controller as given by

$$I_{dr}(s) = \left(K_{pV} + \frac{K_{iV}}{s}\right)({V_{DC}}^{ref} - V_{DC}) \tag{5.5}$$

5.2.3 AC Current Control Loop (ACC)

The grid current is measured using analog to digital converter (ADC) for AC current control purpose. It can be controlled either in the natural reference frame (*abc*-frame), the synchronous reference frame (*dq*-frame) or in the stationary reference frame (αβ-frame). For current control either in αβ-frame or *dq*-frame, the sensed three-phase grid current is frame transferred using either frequency or phase-angle information from the grid synchronization unit (PLL). The *dq*-frame current control using the PI controller is shown in Figure 5.5. Adequate decoupling term and voltage feedforward in *dq*-axes are added at the output of the current control action. The expression for reference voltages for inverter is given by

$$u_{dqr}(s) = \left(K_{pi} + \frac{K_{ii}}{s}\right)(I_{dqr} - I_{dq}) \tag{5.6}$$

The bandwidth of the current control loop is kept much closer to the inverter switching frequency and accordingly the gain parameters are designed. The effect of voltage feedforward terms on the current controller in a weak grid will be discussed later. The reference for the *dq*-axes ACC is provided by the outer loop control. For instance, I_{dr} is generated using the outer DC-link voltage control loop and I_{qr} is generated by the reactive power control loop. Usually I_{qr} is set as zero in the normal operating condition to maintain unity power factor (UPF) operation. On the contrary, the reference current generation is decided by the grid code of a particular country during FRT operation as a result of grid faults. Firstly, the reactive current injection limit is decided based on the grid voltage sag and then active current reference is decided by the maximum current injection limit during fault.

In this chapter, more focus is given during the FRT operation and thus outer loop will not be discussed further.

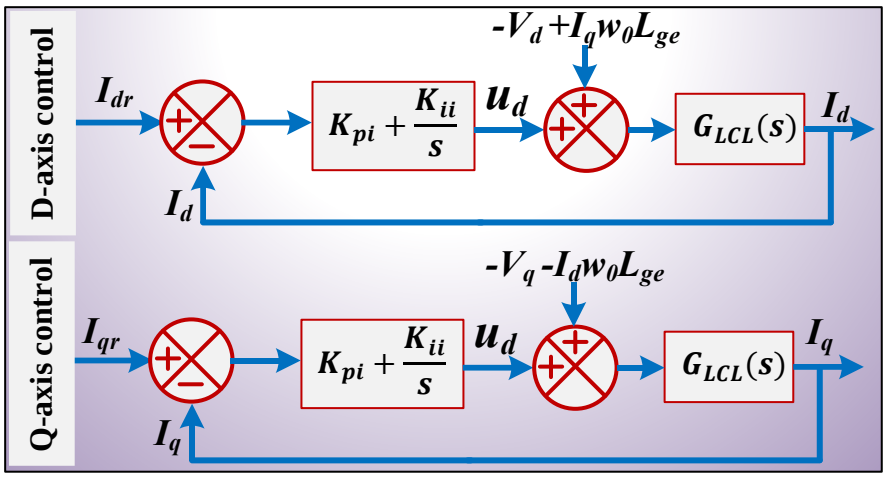


Figure 5.5: AC current control Loop in synchronous reference frame.

5.2.4 Grid Model

The performance of the grid-connected inverters is highly depended on the characteristics of the power grid. The strength of the grid is measured by its sensitivity to any disturbances either load changes, harmonic current injections or any transients for instance grid faults. On the basis of this, grid can be a stiff grid or a weak grid. Topology wise grid model can be represented as radial, looped or mesh type. Out of these, radial presentation of the grid is common in rural regions having low power, long transmission lines with fewer consumers. In this work, radial configuration is used. In fact, in the analysis, the grid model is replaced by its Thevenin equivalent (a voltage source in series with grid impedance).

The tolerance of the grid towards a fault is characterized by the short circuit power that is required to be injected to the fault point. Based on the rating of the power apparatus (nominal

power), such power transfer is related by the short-circuit ratio (SCR). It is defined as the ratio between the short circuit power level (S_{sc}) to the nominal power (S_n) and given by

$$\text{SCR} = \frac{S_{sc}}{S_n} = \frac{{V_g}^2/Z_g}{S_n} \tag{5.7}$$

It can be seen that, the grid impedance (Z_g) is inversely proportional to SCR. Higher Z_g results in lower SCR and vice versa. The SCR for a stiff grid is above 20-25 while for a weak grid is 2-10 [156]. The impact of low SCR (weak grid) on current controller during FRT will be analysed in this chapter. The grid is mainly resistive for low voltage level and inductive for medium/high voltage applications [157]. The inductance to resistance value (X/R) of the grid also affects the dynamics of the current controller through the grid synchronization which will be discussed in the later sections.

5.2.5 Pulse Width Modulation

The sinusoidal input voltage reference to the inverter generated from the output of the current controller is used for the Pulse Width Modulation (PWM) process. The PWM strategy can be of natural sampling (sine wave and triangular carrier wave) or regular sampling. Natural sampling provides complexity for the digital implementation, while regular sampling provides sample delay which is suitable for digital implementations. Regular sampling can be either symmetrical or asymmetrical based on the mode of sampling of the carrier wave's positive and negative peak. In this work, asymmetric regular PWM technique is implemented [158].

5.2.6 Grid Synchronization

The grid parameter estimation at the PCC is essential for grid synchronization and current control for inverters during both normal and FRT modes of operation. It is done by SRFPLL. The basic modelling of the SRFPLL and other state-of-the-art modified SRFPLL suitable for FRT are already discussed in detail in Chapter 4. In this chapter, their impact on the converter's current controller during grid fault is included in this chapter. The comparative improvement in the FRT of the three-phase converter using the proposed hybrid grid synchronization will be discussed in the subsequent sections.

Apart from the adaptive and hybrid grid synchronization proposed in Chapter 4, there are other methods, namely, grid voltage feedforward compensation and SRFPLL with faster settling time, which can improve the transient disturbance (FRT) performance of the converter. However, these methods have negative consequences in case of the weak grid connection of the converter. In the next two sections, the details of these consequences will be discussed.

5.3 DQ Current Control Model with Voltage Feedforward Compensation

In this section, the impact of PCC voltage feedforward compensation on the *dq*-frame current controller is explained in relation to the grid strength such as stiff grid and weak grid. In grid-connected applications, voltage feedforward compensation at the output of the current controller is conducive for inverter operation and control during various transient events. These include inverter starting process, load switch on and off, etc. Such compensation is also feasible to provide improved FRT of converter during a grid fault. Apart from the transient disturbance rejection, this feedforward compensation has certain disadvantages especially when the grid is not stiff (weak grid). In weak grids, the PCC and grid point are not the same. They are separated by the grid impedance. In stiff grid, this impedance is negligible. On the other hand, in weak grid due to low SCR values, this grid impedance is of significant magnitude to influence the feedforward compensation process. The current control loop with and without voltage feedforward compensation considering the weak grid is shown in Figure 5.6. With the addition of PCC voltage, the necessary changes in the current controller are shown in black colour arrows. It can be observed that, the grid current feedback adds extra feedforward compensation to the current controller. This feedforward gain is dependent on the impedance value seen from the PCC (line plus grid impedance - refer Figure 5.2). Therefore, it has the tendency to destabilize the current controller during varying grid impedance values (as in a weak grid) [150].

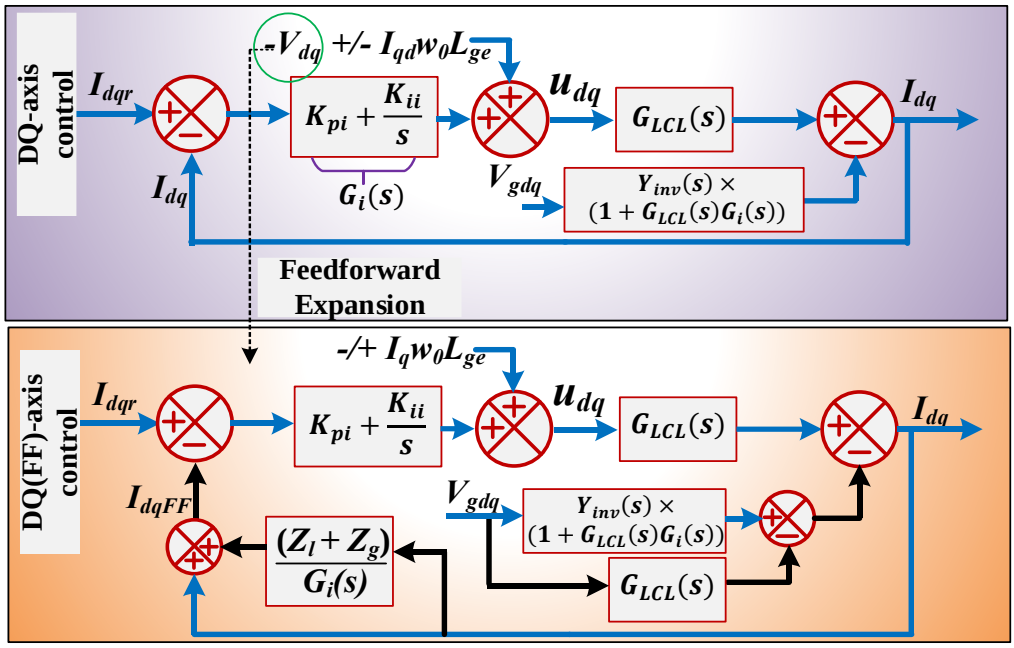


Figure 5.6: AC current control Loop in synchronous reference frame with and without PCC voltage feedforward compensation.

The mathematical expressions to show the impact of the grid impedance dependent feedforward compensation in the current controller gain is as follows:

Equation (5.2) yields the transfer function of grid current in relation to inverter voltage ($G_1(s)$) and grid voltage ($G_2(s)$) as given by

$$G_1(s) = G_{LCL}(s) = \frac{I_{dq}(s)}{V_{dq}(s)} = \frac{1}{s^3 C_f L_f L_{ge} + s(L_f + L_{ge})} \tag{5.8}$$

$$G_2(s) = Y_{inv}(s)\left(1 + G_{LCL}(s)G_i(s)\right) = \frac{I_{dq}(s)}{V_{gdq}(s)} = \frac{1 + s^2 C_f L_f}{s^3 C_f L_f L_{ge} + s(L_f + L_{ge})} \tag{5.9}$$

The PCC voltage expression with respect to the grid voltage is given by

$$V_{dq}(s) = V_{gdq}(s) + I_{dq}(s)\underbrace{(Z_l(s) + Z_g(s))}_{Z_{gn}(s)} \tag{5.10}$$

The current controller loop gain without the consideration of voltage feedforward compensation can be obtained as (the control delay is assumed to be unity):

$$G_{iOpenloop}(s) = G_i(s)G_{LCL}(s) \tag{5.11}$$

The closed loop current controller gain is given by

$$G_{iCloseloop}(s) = \frac{G_i(s)G_{LCL}(s)}{1 + G_i(s)G_{LCL}(s)} \tag{5.12}$$

While considering the PCC voltage feedforward compensation in the current control loop, (5.11) and (5.12) can be modified as

$$G_{iOpenloopFF}(s) = \frac{G_i(s)G_{LCL}(s)}{1 - Z_{gn}(s)G_{LCL}(s)} \tag{5.13}$$

$$G_{iCloseloopFF}(s) = \frac{G_i(s)G_{LCL}(s)}{1 + (G_i(s) - Z_{gn}(s))G_{LCL}(s)} \tag{5.14}$$

It is observed from (5.14), that when the grid impedance is of non-negligible magnitude, it will certainly impact the closed-loop stability of the current controller. As studied in [148], with the high magnitude of net grid impedance ($Z_{gn}(s)$), the closed loop poles will shift towards the positive real axis. This is not the case in stiff grid as the grid impedance is of minimum magnitude and thus can be neglected ($Z_{gn}(s) \approx 0$) while performing the stability analysis. Even without this voltage feedforward compensation, the plant transfer functions have a great coupling with the grid impedance. So in any case, in weak grid, such large grid impedance will bring the resonant frequency and phase margin of the current controller much below than that in the case of a stiff grid.

Direct voltage feedforward compensation to the current controller could enhance the harmonics in the injected grid current in weak grid [150]. This is because, the assumption of the control delay to be unity as in (5.11), overlooks the introduction of the negative resistance in the low and middle frequency band of the current controller and thus degrades its lower order harmonic rejection capability.

The impact of PCC voltage feedforward compensation on the current controller is usually studied for weak grids having grid impedance variations. Nevertheless, it is also interesting to see this impact on the current controller dynamics during FRT of inverters in case of grid faults having PAJs. This is investigated in the simulations and experiments sections of this chapter.

5.4 DQ Current Control Model with SRFPLL

The interaction between the grid side current controller and the SRFPLL happens during the frame transformation (*abc*-*dq*) of the instantaneous three-phase grid current. The phase-angle information required for such transformation is provided by the SRFPLL. Unlike the case in stiff grid, in weak grid the actual phase-angle observed at the PCC (θ_g) differs from that estimated by the SRFPLL (θ_{PLL}). This results in a phase-angle deviation of ($\Delta\theta = \Delta\theta_{PLL}$) between the actual *dq*-frame and the estimated *dq*-frame by the SRFPLL. This $\Delta\theta$ is highly dependent on the tuning of the SRFPLL control loop (discussed in Chapter 4). Accordingly, the *dq*-components of the PCC voltage and the grid currents are affected in relation to this $\Delta\theta$ during the frame transformation. This dependency can be well understood from the small-signal modelling of *dq*-frame current controller including the SRFPLL controller [159]. The controller loop including the SRFPLL along with *d*- and *q*- axes control is shown in Figure 5.7.

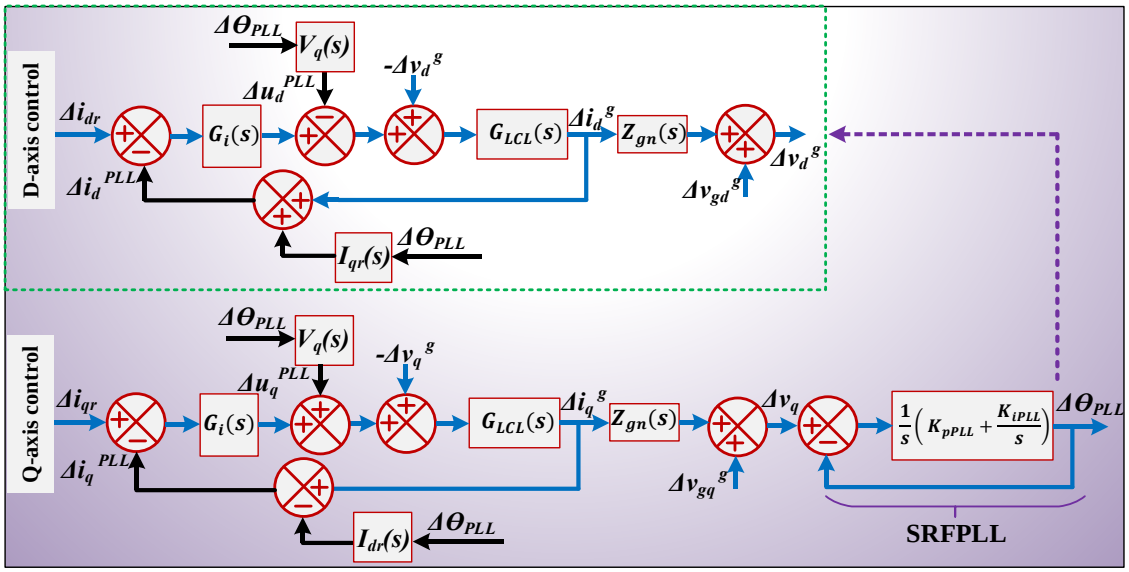


Figure 5.7: AC current control Loop in synchronous reference frame with SRFPLL.

The small-signal modelling is as follows. The variables estimated by SRFPLL is denoted by superscript "PLL" and those in the actual (grid side) frame are denoted "g" in the derivations. The mathematical relationship between these two frames with respect to $\Delta\theta$ is given by

$$\Delta v_{dq}{}^{PLL}/\Delta i_{dq}{}^{PLL} = \Delta v_{dq}{}^{g}/\Delta i_{dq}{}^{g}[1 - j\Delta\theta] \tag{5.15}$$

The relation of $\Delta\theta$ to the q-axis of the PCC voltage ($\Delta v_q{}^{g}$) can be expressed by the closed-loop gain of the SRFPLL as given by

$$G_{PLL}(s) = \frac{\Delta\theta}{\Delta v_q{}^{g}} = \frac{G_{PIPLL}(s)}{s + V_d G_{PIPLL}(s)} \tag{5.16}$$

where

$$G_{PIPLL}(s) = K_{PPLL} + \frac{K_{IPLL}}{s}$$

The expression for transformed dq-components of voltage ($\Delta v_{dq}{}^{PLL}$) and those for currents can be given by

$$\begin{aligned}\Delta {v_d}^{PLL} &= \Delta {v_d}^{g} + \Delta\theta V_q \\ \Delta {v_q}^{PLL} &= \Delta {v_q}^{g} + \Delta\theta V_d\end{aligned} \tag{5.17a}$$

$$\begin{aligned}\Delta {i_d}^{PLL} &= \Delta {i_d}^{g} + \Delta\theta I_{qr} \\ \Delta {i_q}^{PLL} &= \Delta {i_q}^{g} + \Delta\theta I_{dr}\end{aligned} \tag{5.17b}$$

Accordingly, the small signal net grid current as per Norton's equivalent can be given by

$$\Delta {i_{dq}}^{g} = G_{iCloseloop}(s)\Delta i_{dqr} - Y_{inv}(s)\Delta {v_{dq}}^{g} - Y_{PLLdq}(s)\Delta {v_{dq}}^{g} \tag{5.18}$$

It can be seen that an extra admittance term ($Y_{PLL}(s)$) is fed forward to the current controller. The expression for $Y_{PLL}(s)$ is given by

$$Y_{PLL}(s) = G_{iOpenloop}(s)G_{iPLL}(s) + G_{LCL}(s)G_{vPLL}(s) = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{5.19}$$

and current gain terms ($G_{iPLL}(s)$) as given by

$$G_{vPLL}(s) = \begin{bmatrix} 0 & V_q G_{PLL}(s) \\ 0 & -V_d G_{PLL}(s) \end{bmatrix}, \text{and } G_{iPLL}(s) = \begin{bmatrix} 0 & I_q G_{PLL}(s) \\ 0 & -I_d G_{PLL}(s) \end{bmatrix} \tag{5.20}$$

In a weak grid, the dq-axes PCC voltage and grid voltage are related as

$$\begin{bmatrix} \Delta {v_d}^{g} \\ \Delta {v_q}^{g} \end{bmatrix} = \begin{bmatrix} \Delta {v_{gd}}^{g} \\ \Delta {v_{gq}}^{g} \end{bmatrix} + \begin{bmatrix} Z_g(s) & 0 \\ 0 & Z_g(s) \end{bmatrix} \begin{bmatrix} \Delta {i_d}^{g} \\ \Delta {i_q}^{g} \end{bmatrix} \tag{5.21}$$

On solving, (5.18), (5.19), (5.20) and (5.21), the net Y bus matrix for grid-connected inverter and expression for q-axis current is given by

$$Y_{11}(s) = Y_{inv}(s), Y_{12}(s) = Y_{21}(s) = 0, Y_{22}(s) \\ = Y_{inv}(s) - (I_{dr} G_{iCloseloop}(s) + V_d Y_{inv}(s)) G_{PLL}(s) \quad (5.22)$$

$$\Delta {i_q}^g = \frac{G_{iCloseloop}(s)}{1 + Y_{22}(s) Z_g(s)} \Delta i_{qr} \quad (5.23)$$

The expression is given assuming V_q= 0 and unit power factor (UPF) operation.

It can be observed from (5.22) and (5.23) that the SRFPLL parameter tuning affects q-axis $Y_{22}(s) \Delta {i_q}^g Y_{22}(s) Y_{22}(s) Z_g(s)$

Sections 5.3 and 5.4 revealed that, either voltage feedforward compensation or SRFPLL with faster settling time can improve the FRT of the converter by compromising with its closed-loop control stability. Thus in this chapter, the settling time of the SRFPLL is kept high (120 ms) to not disturb the stability as part of the hybrid grid synchronization. A test case with and without voltage feedforward compensation during the FRT is provided in the simulation section 5.6. Other investigations are carried out without adding the voltage feedforward compensation.

The following sections will explain the FRT setting of the converter controller for various grid faults (both symmetrical and asymmetrical). Both simulation and experimental analysis are performed.

5.5 Fault Ride-Through during Symmetrical Grid Faults

This section explains the FRT strategy embedded in the converter's current control, which is the main theme of the thesis. Under normal grid operating conditions, the *d*-axis reference current (I_{dr}) is decided by the outer DC-link voltage control loop as explained in 5.2.2. Similarly, *q*-axis reference current (I_{qr}) is kept zero to maintain unit power factor (UPF) operation. These references switch from the outer loop control to FRT mode on the occurrence of any grid fault. The control structure used during the FRT using the proposed hybrid grid synchronization for the VSC is shown in Figure 5.8. In the FRT mode, the I_{qr} is chosen based on the voltage sag depth seen at the PCC. The sag is calculated by the hybrid grid synchronization unit.

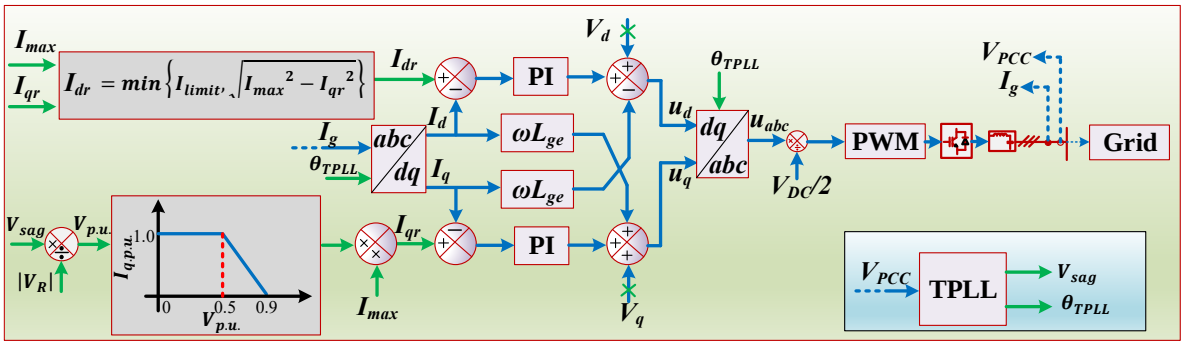


Figure 5.8: Grid current control loop using the proportional plus integral (PI) during symmetrical grid faults.

Based on the sag depth, different countries follow different grid codes to decide the reactive current injection support to the grid as given by

$$\left|\frac{I_{qr}}{I_{max}}\right| = \begin{Bmatrix} 0, & if\ \ 0.9 < V_{pu} \le 1.0, & Zone-3 \\ (k=2)(1-V_{pu}), & if\ \ 0.5 < V_{pu} \le 0.9, & Zone-2 \\ 1.0, & if\ \ 0.0 \le V_{pu} \le 0.5, & Zone-1 \end{Bmatrix} \tag{5.24}$$

The value of "*k*" can be chosen from 2 to 10. Higher values of "*k*" drive the PCC voltage to dead zone (0.9 pu -1.1 pu) as per the grid code. This in turn results in undamped oscillations

in the injected active and reactive power. Due to these oscillations, the converter may fail to provide robust FRT support during faults. Hence, the optimal value of "*k*" is chosen to be 2 in this chapter. Once the I_{qr} is decided, it is fed to the current priority unit to decide I_{dr}. The current priority unit also contains the previously set $I_{max.}$ I_{dr} is chosen as given by

$$I_{dr} = \min\left\{I_{limit}, \sqrt{{I_{max}}^2 - {I_{qr}}^2}\right\} \tag{5.25}$$

The voltage profile along with reactive current injection pattern followed during fault is shown in Figure 5.9.

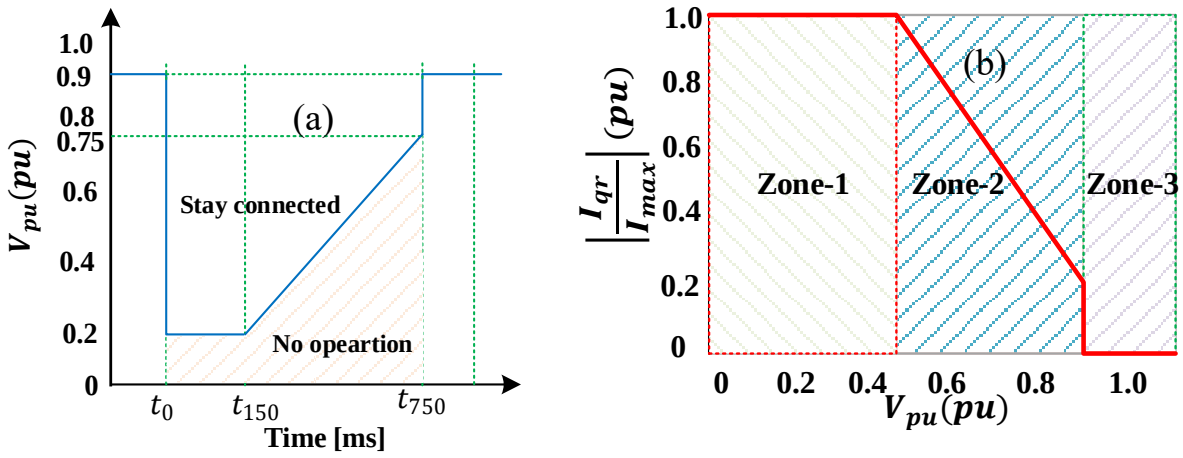


Figure 5.9: (a) Voltage profile and (b) reactive current injection following fault ride-through operation.

5.6 Simulation and Experimental Results

The FRT operation of the grid-connected three-phase voltage source converter (VSC) is simulated using the switching model as given in Figure 5.2. The model is built in the MATLAB/SIMULINK and PLECS Blockset software environment. The converter and controller parameters used for modelling are given in TABLE 5.1. The fault at the grid side is a three-phase symmetrical fault of 60% voltage sag depth at t = 0.35s which is cleared at t = 0.55s. The PAJs are chosen to be both +45° and -45° along the fault inception and recovery.

The reasons for selecting these two PAJs (+45° and -45°) are:

1) During balanced faults, the PAJ seen by the grid-connected converter at PCC varies between +10° and -60° [68]. On the other hand, during the unbalanced faults, the voltage sag observed at the high voltage (HV) side of the transformer is propagated to the low voltage (LV) side depending on the transformer connection type. Accordingly, the PAJ observed by the converter connected at the LV side can vary between +45° and -45° for different sag magnitudes.
2) At this higher angle, the linearity assumed by the SRFPLL control loop during grid synchronization becomes invalid, which leads to the poor FRT of the converter. To improve the converter's FRT during such PAJs using hybrid grid synchronization is the objective of this thesis.

The results obtained by simulation for various test scenarios are discussed below.

TABLE 5.1: THREE-PHASE CONVERTER AND CONTROLLER PARAMETERS

Parameters and Symbols	Values
Rated Power (P_{rated})	2.2 kW
DC voltage (V_{DC})	400 V
Grid voltage (Secondary side) (V_g)	240 V_{rms}
PCC voltage (Primary side) (V_{PCC})	120 V_{rms}
Nominal current (Primary side) (I_N)	8.65 A_{peak}
Grid Frequency (f_g)	50 Hz
Proportional gain of the voltage control (K_{pV})	8
Integral gain of the voltage control (K_{iV})	7000
Proportional gain of the current control (K_{pi})	12
Integral/Resonant gain of the current control (K_{ii}/K_{ir})	7000
Settling time of the SRFPLL (t_{set})	120 ms
Transition time for TPLL (t_{tr})	2 ms
Grid side filter inductance (L_{fg})	1.8 mH
Converter side filter inductance (L_f)	0.5 mH
Sampling frequency (f_{sam}) and Switching frequency (f_{sw})	10 kHz

5.6.1 Comparison with and without PAJ during Symmetrical Fault

Initially, the FRT operation of VSC synchronised with the classical second-order SRFPLL is simulated during the symmetrical fault without the addition of any PAJ.

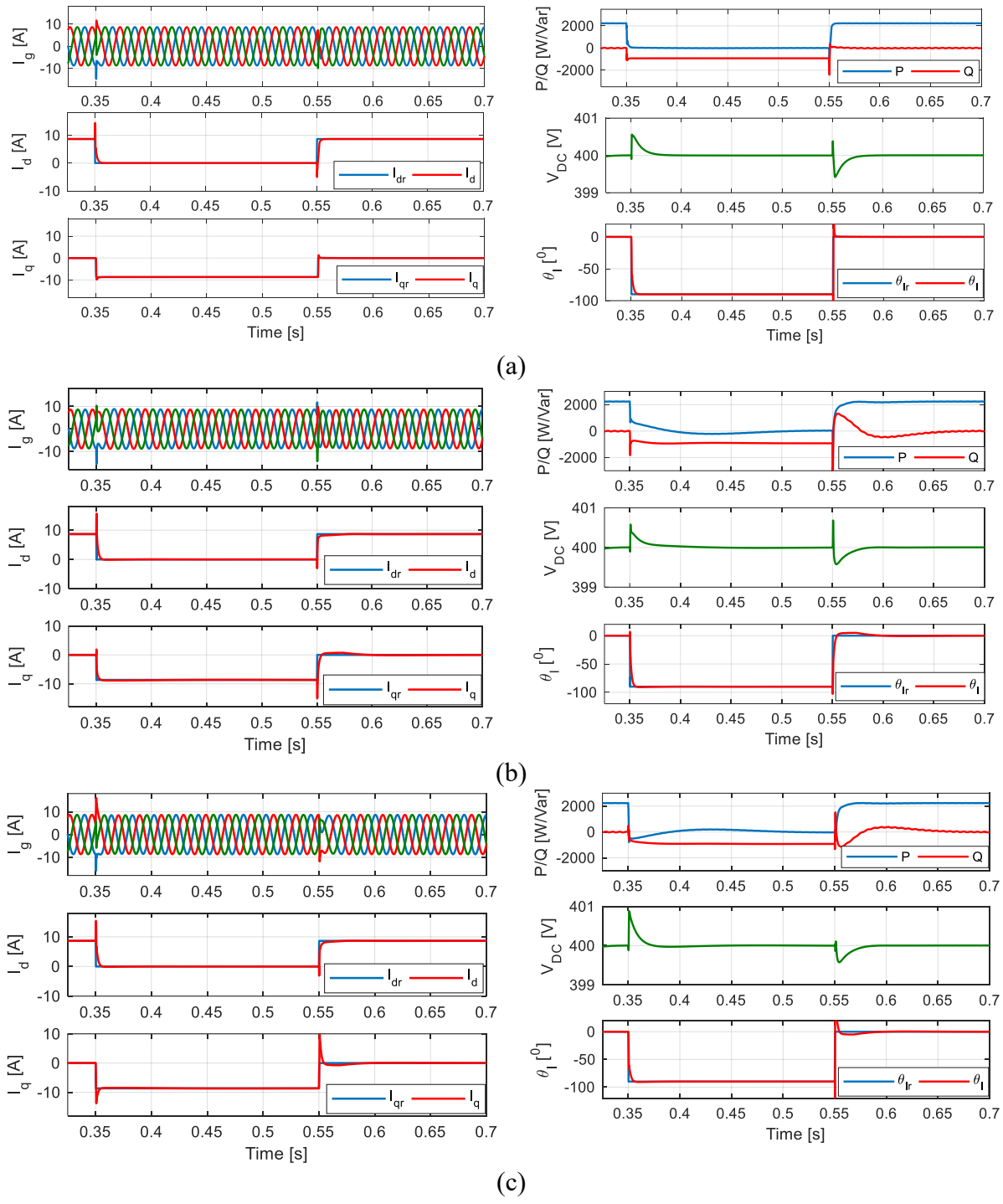


Figure 5.10: FRT of Three-phase VSC synchronized with second-order SRFPLL during 60% sag: with (a) no PAJ, (b) -45° PAJ and (c) 45° PAJ.

The plots for grid current (I_g), dq-axes components of grid currents (I_{dq}), active and reactive power (P/Q), DC-link voltage (V_{DC}) and the fault current angle (θ_I) are shown in Figure 5.10(a). It is observed that there is a smooth tracking of the grid current to inject the rated reactive current as per the grid code requirement. The injection of the full reactive current and null active current is noted with the active power injection of 0 W and the reactive power injection of 925 Var. The pure reactive current injection can also be viewed from the grid current injection angle which is of 90° lagging PF.

With the addition of PAJ during fault inception, it is observed that, I_q dynamics is affected and due to the dq-axes coupling behaviour, settling time for I_d is increased as shown in Figure 5.10(b) and Figure 5.10(c). The dynamics of I_q can be well understood as a result of the delayed response of the SRFPLL while estimating the V_q. I_q gets affected due to the SRFPLL dynamics during a PAJ in relation to V_q through the q-axis self-admittance (Y_{22} (s)) as shown in (5.22) and (5.23).

It is observed that with the change in the sign of the PAJ, the dynamics of the grid currents, power profiles, and DC-link voltage are complementary to each other. During +45° PAJ, the overshoots observed in the grid current is higher as compared to that in the case of -45° PAJ. The settling time for I_q during both the sign of PAJs are observed to be 70 ms while the settling time for P and Q are around 120 ms due to delayed estimation of dq-axes voltage components by the SRFPLL.

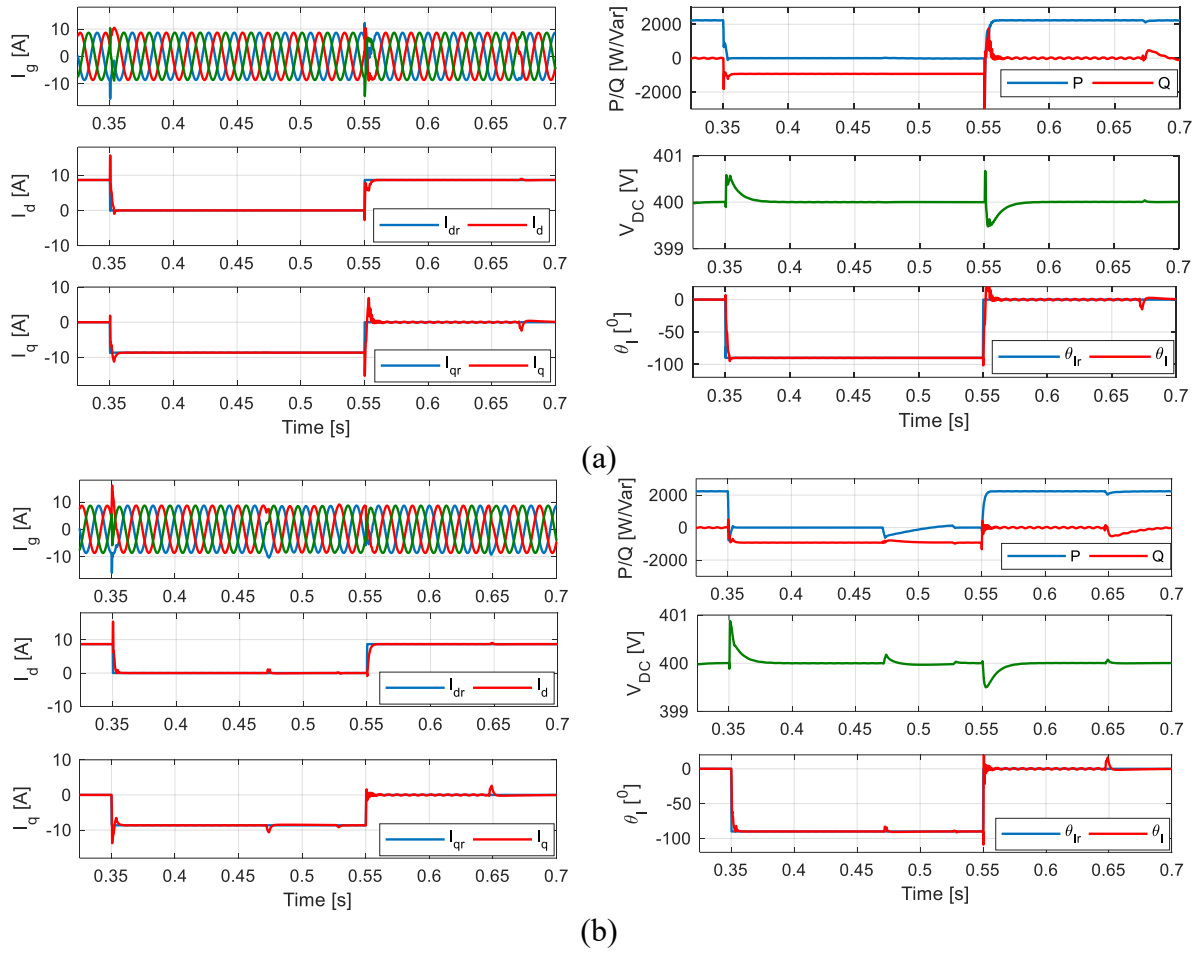


Figure 5.11: FRT of Three-phase VSC synchronized with proposed TPLL during 60% sag: with, (a) -45° PAJ, and (b) +45° PAJ.

The performance of the proposed transition phase-angle (TPLL) based hybrid grid synchronized VSC is tested during the symmetrical voltage sag with both -45° and +45° PAJs as shown in Figure 5.11(a) and Figure 5.11(b) respectively. The settling time for I_q is greatly improved for the proposed technique during both fault inception and recovery point. It is observed to be 8 ms in both the cases. The faster settling of I_q helps in improving power profiles (P/Q) during fault and post-fault time. The transition is enabled until the time the SRFPLL takes to settle to the steady-state equilibrium point (which is the settling time for the SRFPLL i.e. 120 ms in this work). Assuming the phase-angle error to be negligible between the SRFPLL estimation and arctangent estimation after 120 ms, both the estimators swap

among themselves and accordingly the VSC uses the phase-angle for current controller. The transition time is kept 2 ms. The transition scheme is observed to be smoother for -45° PAJ as compared to +45° PAJ during the FRT period. In power systems during grid faults, positive PAJs are less realistic as compared to the negative PAJs [68].

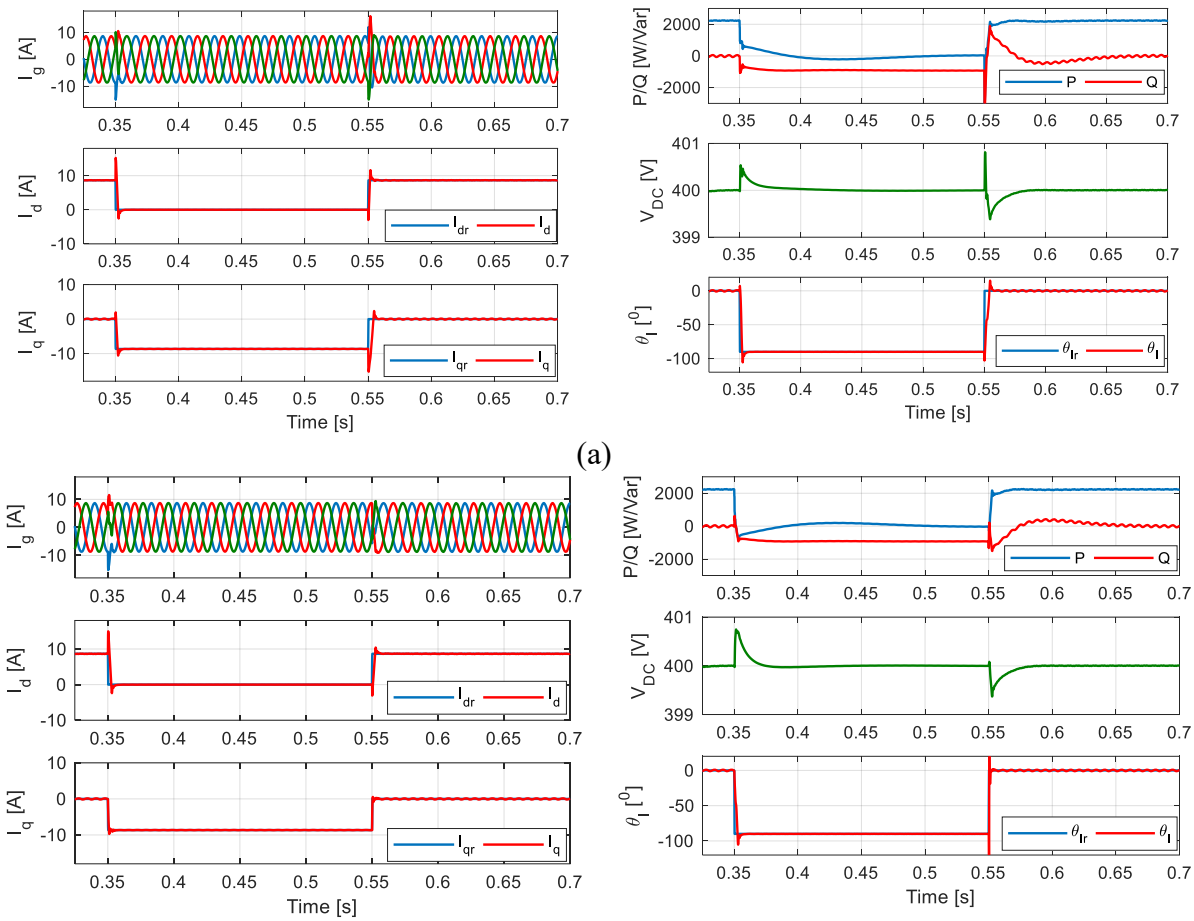


Figure 5.12: FRT of Three-phase VSC synchronized with second-order SRFPLL with PCC voltage feedforward compensation during 60% sag: with, (a) -45° PAJ, and (b) +45° PAJ.

As studied in the Section 5.3, the addition of PCC voltage feedforward compensation can also minimize the disturbance in the current controller caused due to PAJ in SRFPLL synchronised VSC (settling time). Thus, FRT with the addition of voltage feedforward compensation is compared with the proposed TPLL synchronization in terms the transient dynamics of current controller during fault inception and recovery as shown in Figures 5.12 (a) and (b). It can be noticed that the current controller tracking is greatly improved with the voltage feedforward addition as compared to without compensation in SRFPLL synchronized VSC. The power profile dynamics on the other hand (P/Q) is not improved in comparison to the proposed technique. The settling time I_q during -45° PAJ is observed to be slightly higher than the proposed TPLL. On the other hand, the response time during +45° PAJ is almost identical.

5.6.2 Comparison in a Weak Grid

The addition of direct PCC voltage feedforward compensation in SRFPLL grid synchronised VSC improves the disturbance rejection capability as shown in 5.6.1. On the other hand, such addition adds harmonics in the injected grid current due to high line impedance. On the same note, the proposed TPLL uses the arctangent phase-angle estimation during fault which suffers in such weak grid due to the lack of inherent filtering. However, the TPLL improves the grid current distortions in weak grid using SRFPLL filtering during normal operating condition. The total harmonic distortion (THD) measurements of the grid current for the SRFPLL with voltage feedforward compensation and the proposed TPLL technique are shown in Figures 5.13 (a) (b) respectively. The measurements are done after the fault recovery. The THD improvement with TPLL can be observed when it switches back to SRFPLL at t = 0.67 s (Transition point). The SRFPLL, in this case does not include the

voltage feedforward terms. To improve the filtering capability of the proposed TPLL during FRT during grid unbalance and harmonics, dual second-order generalized integrator (DSOGI) is used as the pre-filter which is discussed in Chapter 4.

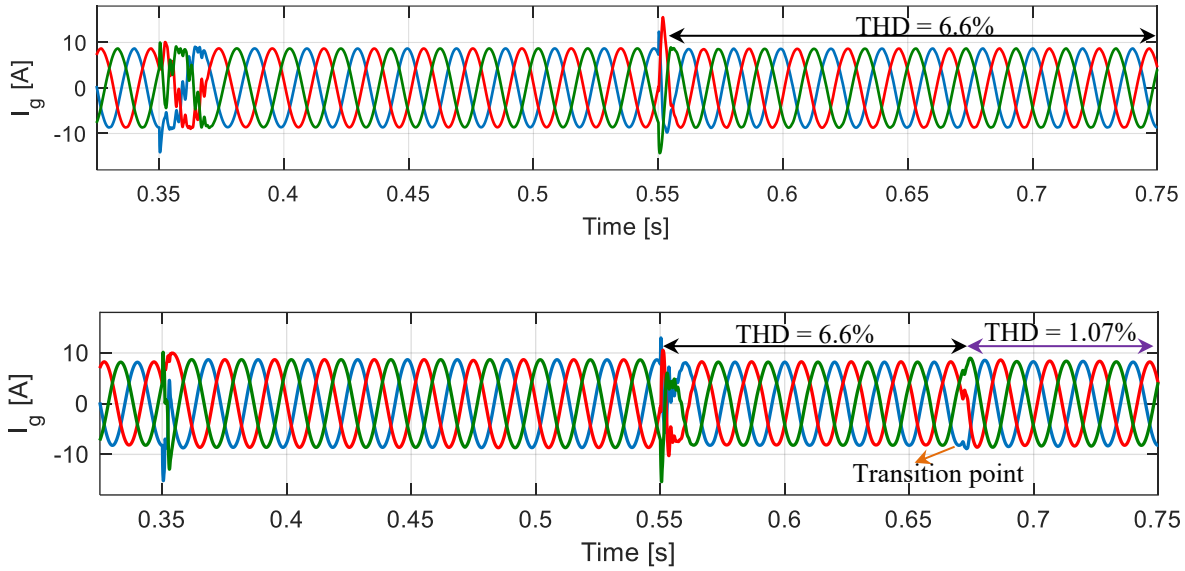


Figure 5.13: FRT of Three-phase VSC synchronized with (a) second-order SRFPLL with PCC voltage feedforward compensation and (b) proposes TPLL during 60% sag with -45° PAJ.

5.6.3 Comparison during loss of synchronization (LOS)

One of the common issues with the conventional SRFPLL based grid synchronization is the loss of synchronization (LOS) during severe symmetrical faults [49]. The details of the LOS phenomena and how this affects the FRT of VSC are explained in Chapter 3. It is understood that the LOS can be due to either the large signal or the small signal instability. Both the cases are simulated for SRFPLL by creating a symmetrical fault with 90% voltage sag depth. During this fault level, the rated reactive current is injected which is kept 8.65A_{pk} as decided by the grid resistance i.e. (0.09 pu). The steady-state current limit is ≥10 A_{pk}. In Figure 5.14(a), the VSC is able to inject the 8.65 A_{pk} during the 90% symmetrical sag with no PAJ. In Figure 5.14(b), it is shown that while trying to inject current =10 A_{pk}, which is the

violation for steady-state current limit, grid current destabilizes during FRT period. In Figure 5.14(c), the current magnitude is maintained $8.65A_{pk}$ to ensure large-signal stability. The addition of -45° PAJ to the 90% voltage sag triggers the small-signal instability of SRFPLL due to less damping and high settling time. Under such conditions, the adaptability of the proposed TPLL is compared and the response is shown Figure 5.14(d). It is observed that, it provides a robust current controller dynamics from fault inception to the end of FRT. The transition back to SRFPLL during the post fault recovery is not smooth as during that time the frequency estimated by SRFPLL is out of synchronism that creates a huge and unregulated phase error for the proposed TPLL to malfunction.

The LOS discussed above is under the assumption that the estimated frequency by SRFPLL is not bandlimited. Further the LOS is tested with the lower and upper limit for the frequency estimations set as 45 Hz and 55 Hz respectively. With this frequency band limit the test cases and responses shown in Figure 5.14 (c) and Figure 5.14 (d) are reinvestigated. It is observed from Figure 5.14 (e) and Figure 5.14 (f), that both the SRFPLL and the proposed technique provide improved FRT during the fault. The resynchronization process is noticed to be poor for SRFPLL resulting in huge oscillations in I_g, P, Q and V_{DC}. In contrast, the proposed technique takes around 60-70 ms to resynchronize during the post-fault condition.

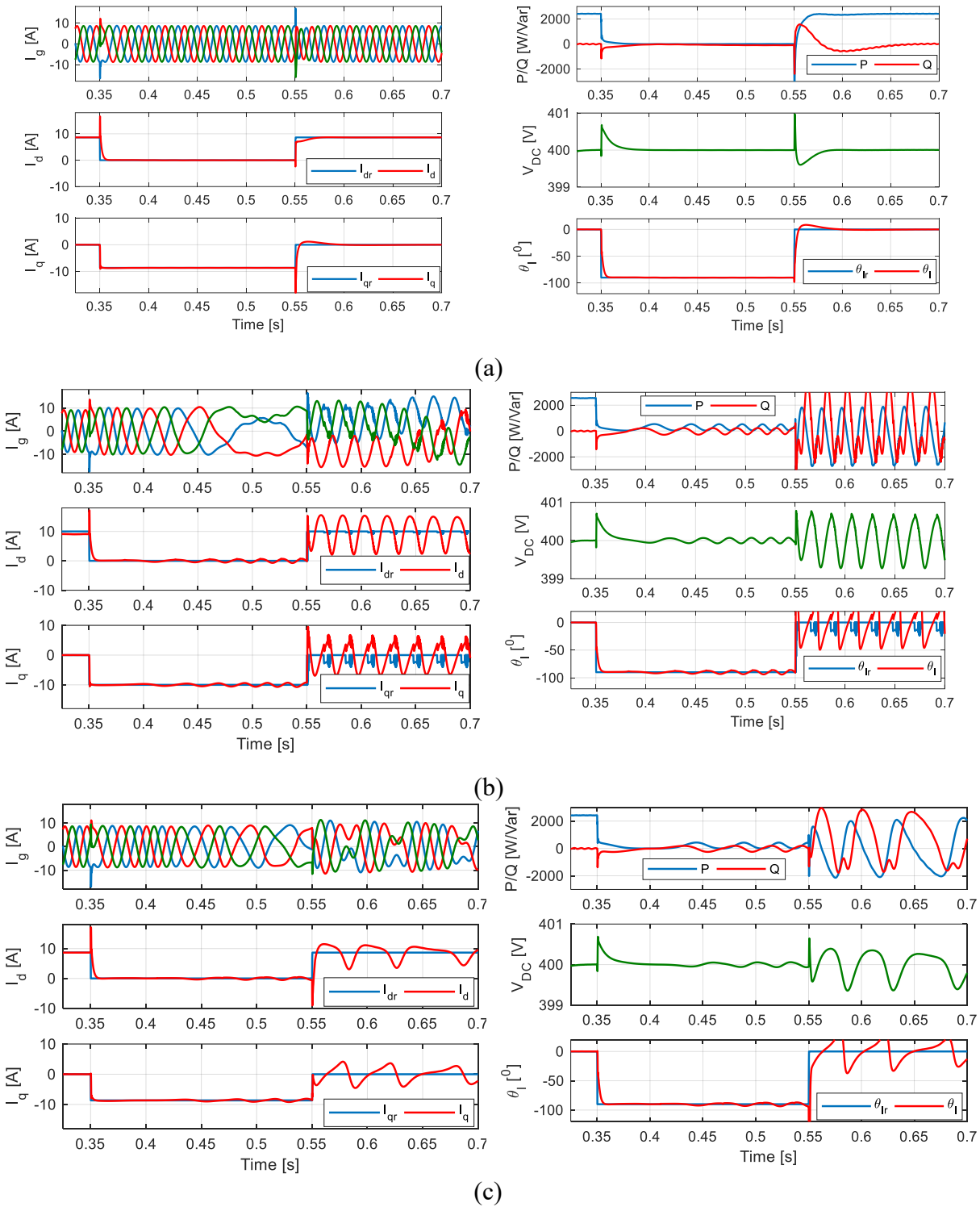
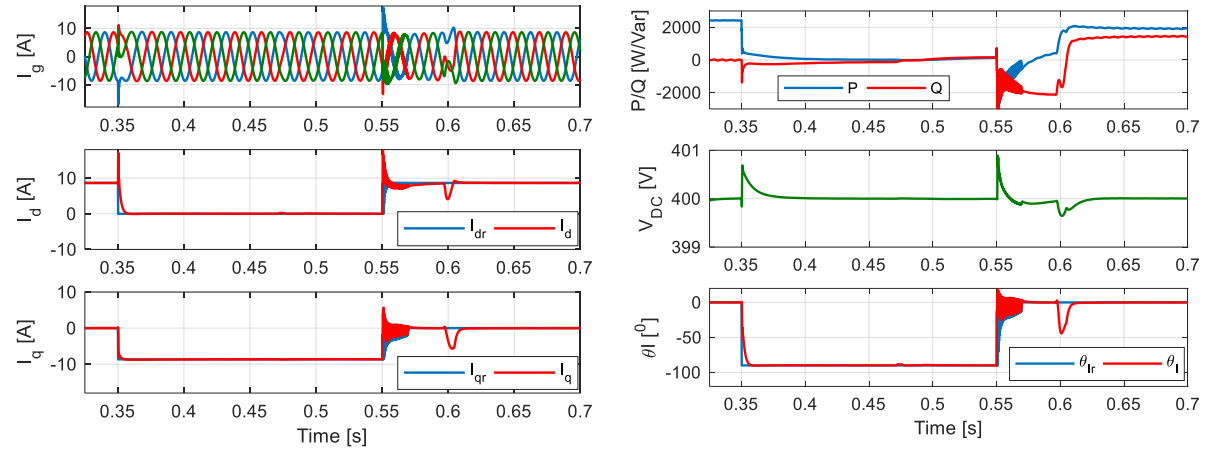
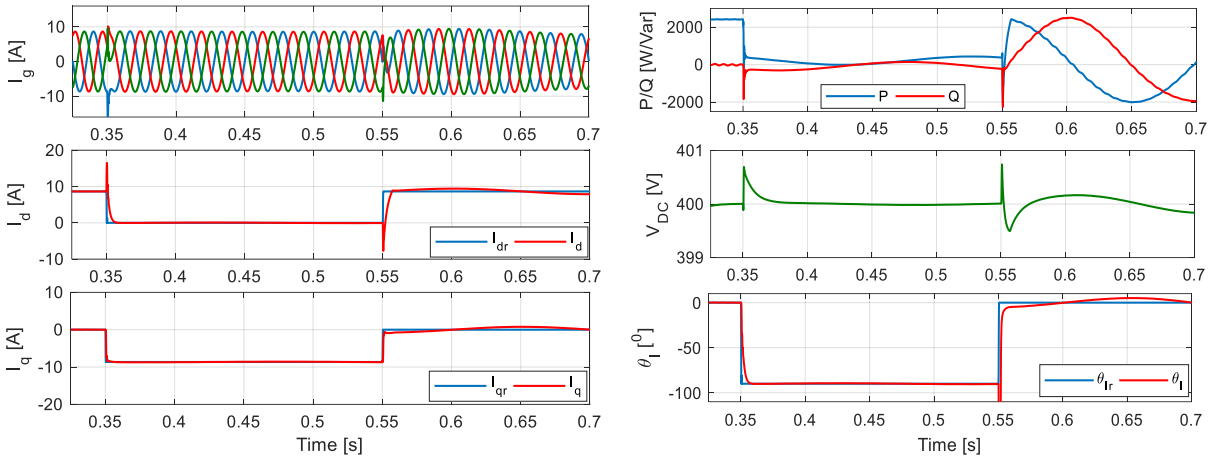


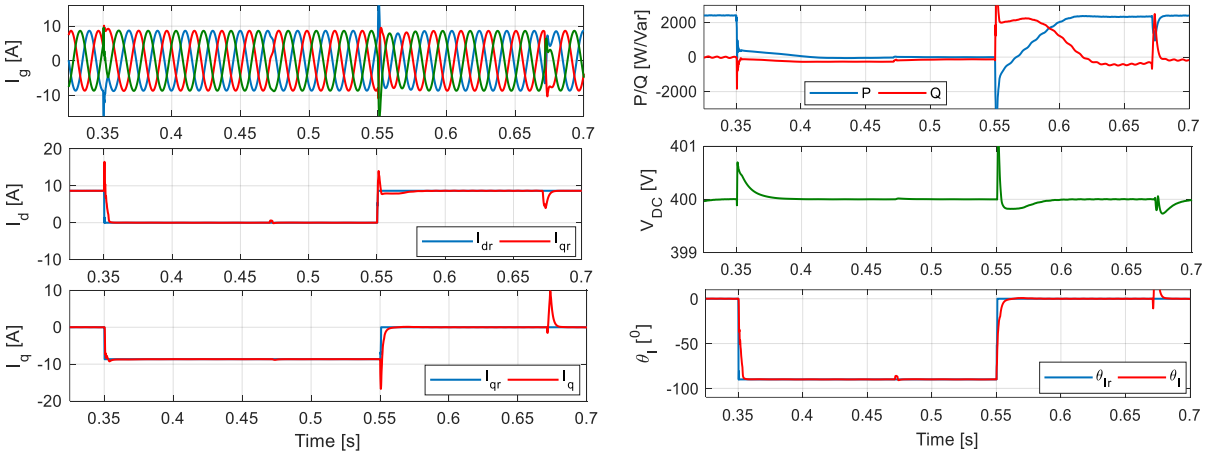
Figure 5.14: FRT of Three-phase VSC during 90% sag with second-order SRFPLL: (a) within steady-state current limit (8.65 A_{pk}), (b) LOS due to violating steady-state current limit (10 A_{pk}), (c) LOS within steady-state current limit (8.65 A_{pk}) but with -45° PAJ,



(d)



(e)

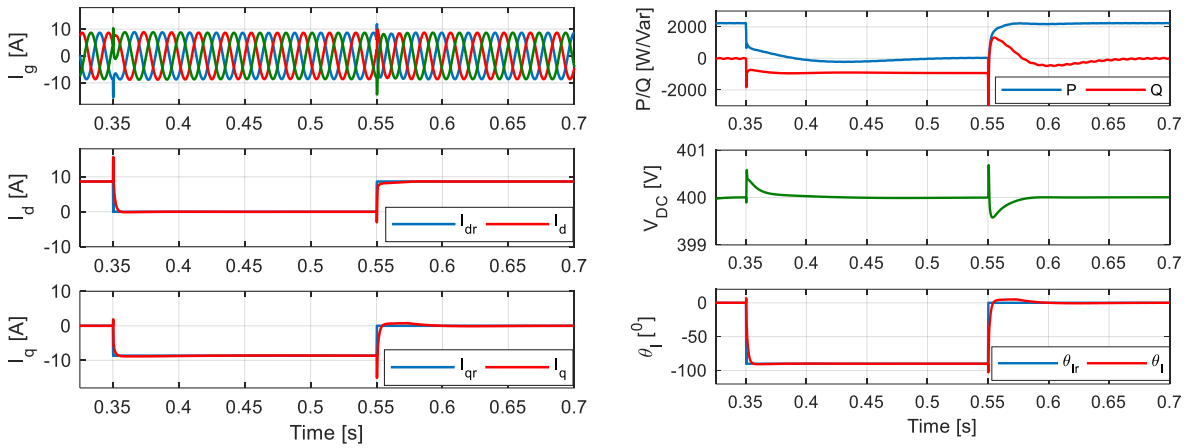


(f)

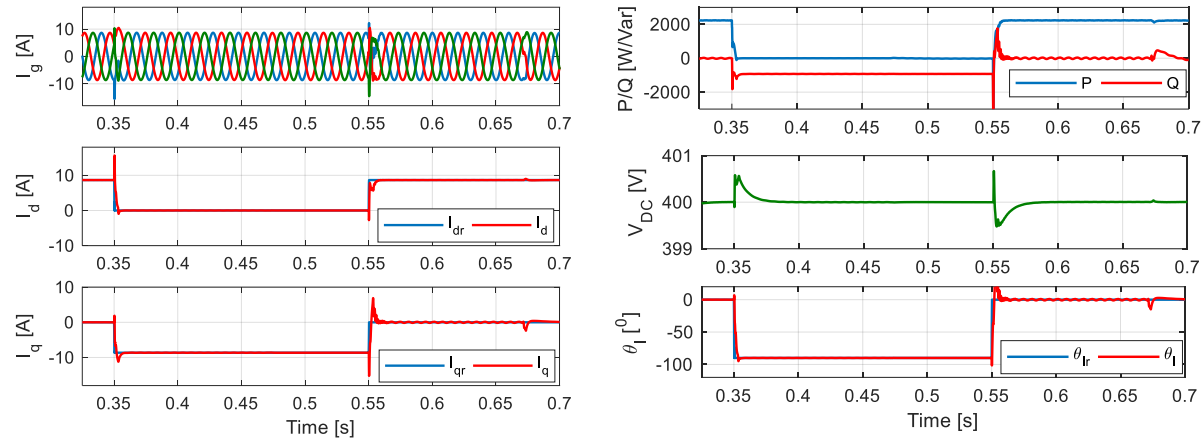
Figure 5.14: FRT of Three-phase VSC during 90% sag with, (d) improvement to LOS with proposed technique (TPLL) due to -45° PAJ and within steady-state current limit (8.65 A_{pk}), (e) Reinvestigation of (c) with frequency band limit (45 Hz-55 Hz), and (f) Reinvestigation of (d) with frequency band limit (45 Hz-55 Hz).

5.6.4 Comparison with other adaptive synchronization techniques

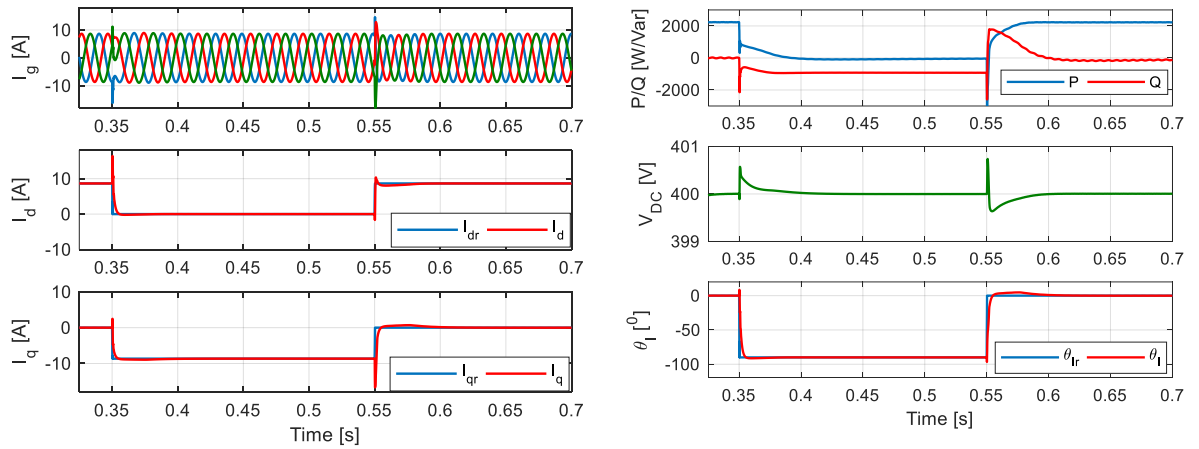
The FRT performance of the VSC synchronised with other adaptive synchronization techniques are shown in Figure 5.15 (a) to Figure 5.15 (e). For comparison purpose, 60% symmetrical voltage sag along with -45° PAJ is chosen. Figure 5.15(a) and Figure 5.15(b) show the dynamics for the second-order SRFPLL and the proposed TPLL. The comparison with the second-order SRFPLL with higher ζ (=1.5), and first-order SRFPLL (K_{iPLL}=0), is done in Figure 5.15(c) and Figure 5.15(d) respectively. It is observed that with both the schemes, the tracking time for I_q is reduced to around 30 ms. This is more than the proposed TPLL and less than the second-order SRFPLL. The settling time for P and Q during fault and post-fault is reduced to 50 ms. On the other hand, with the Freeze PLL ($V_{qp.u.} = 0$), the dynamics is observed to be much faster as the proposed TPLL than all the other adaptive techniques as shown in Figure 5.15(e). Nevertheless, by freezing the PLL during fault, the converter is unable to track the -45° PAJ in the grid voltage correctly. As a result, it fails to inject the exact amount of P and Q as required by the grid code. This can be observed from the error present in the injected power profiles during FRT (refer Figure 5.15(e)). Thus this technique is not suitable for robust FRT of the converter especially when the grid faults include PAJs.



(a)

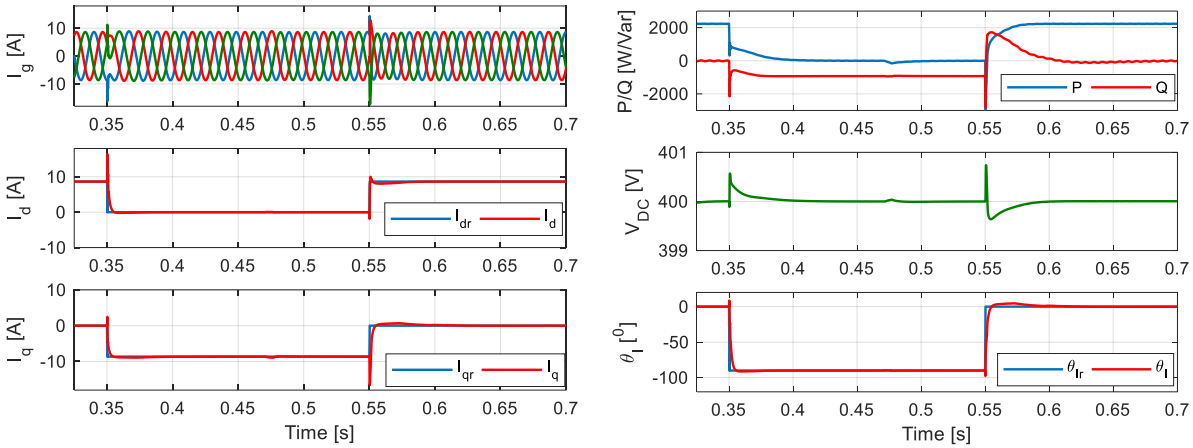


(b)

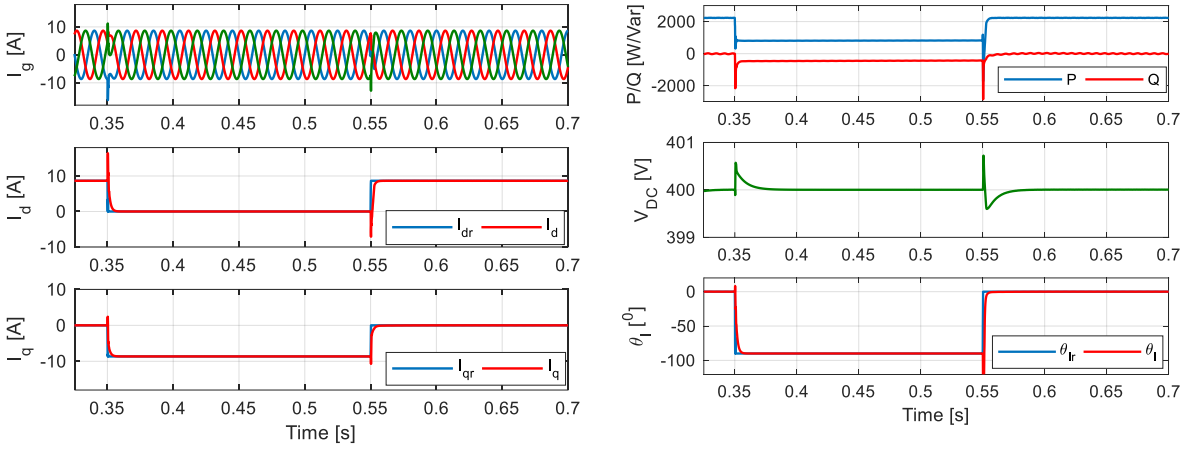


(c)

Figure 5.15: FRT of Three-phase VSC synchronized during 60% sag and -45° PAJ, with (a) second-order SRFPLL, (b) Proposed TPLL, (c) second-order SRFPLL with ζ = 1.5,



(d)



(e)

Figure 5.15: FRT of Three-phase VSC synchronized during 60% sag and -45° PAJ, with (d) first-order SRFPLL ($K_{iPLL} = 0$) and (e) Freeze SRFPLL ($V_{qp.u.} = 0$).

5.6.5 Experimental Validation

The performance of the proposed technique is also validated using laboratory experiments (refer Section C of Appendix) and compared with the other adaptive synchronization techniques as shown in Figure 5.16. The fault at the grid side is chosen similar to that of the simulation analysis i.e. 60% sag and -45° PAJ. The fault duration is kept for 150 ms. The nominal power for the inverter is kept ≅1 kW, which injects $2A_{pk}$ grid current in the secondary of the transformer having 1:2 turns ratio. The inverter is connected to the low voltage side ($120V_{rms}$) which injects $4A_{pk}$ current during fault. The parameters compared are

the grid current (I_g), dq-axes components of grid currents (I_{dq}), and active and reactive power (P/Q). Thee dynamics in terms of tracking time of I_{dq}, P and Q matches with those of the simulation findings.

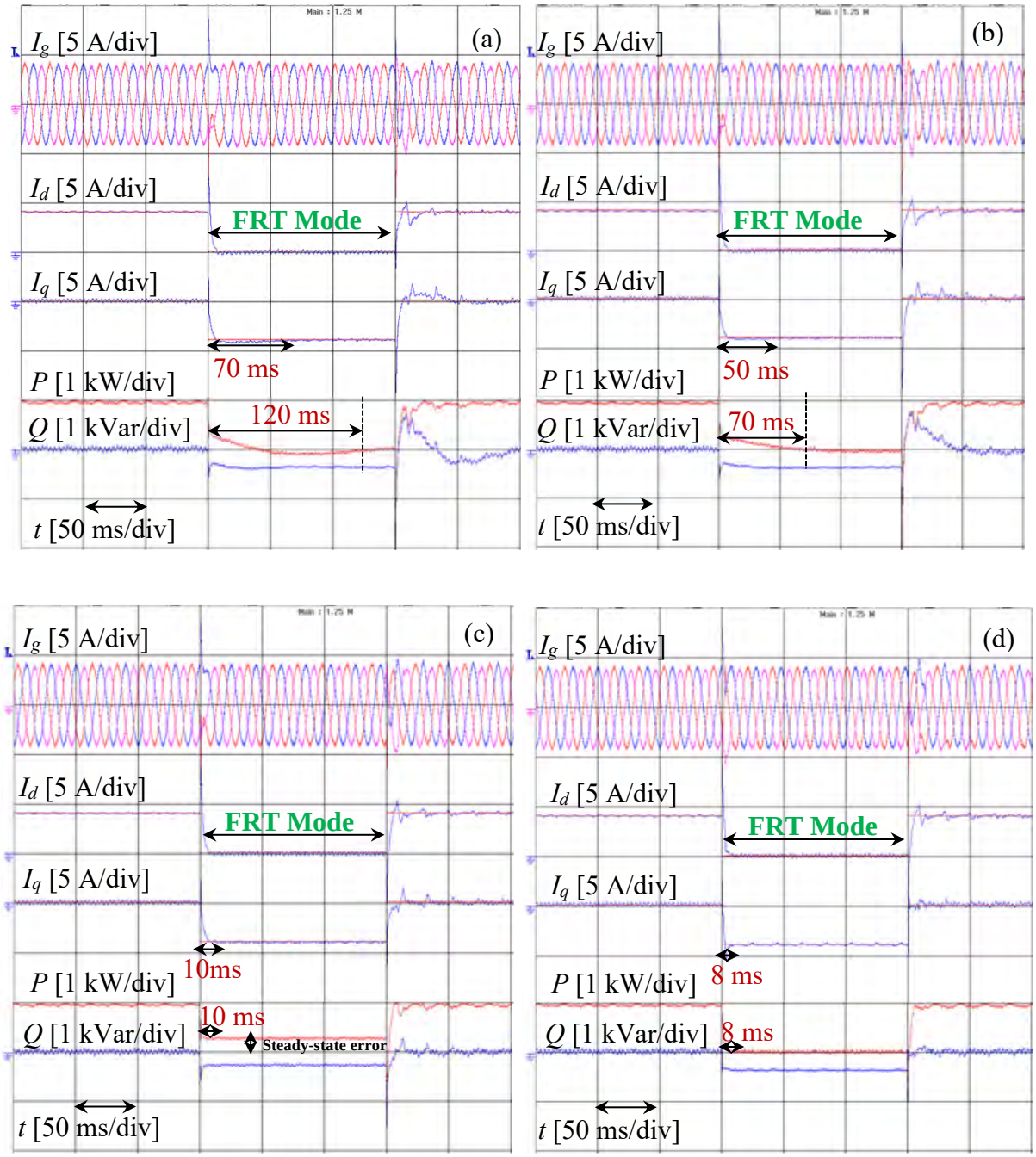


Figure 5.16: Experimental Validation of FRT of Three-phase VSC synchronized during 60% sag and -45° PAJ, with (a) second-order SRFPLL, (b) first-order SRFPLL ($K_{iPLL} = 0$), (c) Freeze SRFPLL ($V_{qp.u.} = 0$), and (d) Proposed TPLL.

5.7 Fault Ride-Through during Asymmetrical Grid Faults

During asymmetrical grid faults, the grid voltage contains positive, negative and zero sequence components. Various types of asymmetrical grid faults are discussed in Chapter 3. Accordingly, the grid current gets unbalanced. The phase-angle estimated by either SRFPLL or arctangent method gets distorted due to the presence of double frequency component in the estimated grid frequency. To avoid this issue, DSOGI pre-filter is used for the PCC voltage to extract the positive sequence components and fed to the phase estimator. Details of the implementation and performance of the DSOGI with the proposed hybrid grid synchronization during asymmetrical grid voltage is provided in Chapter 4. In this Chapter, the proposed hybrid grid synchronization technique is implemented in two types of current controllers. Positive sequence grid currents in proportion to the positive sequence voltage are injected during asymmetrical grid faults. The current controllers selected are: (a) Proportional plus Integral plus second Resonant (PIR_2) and (b) Proportional plus Resonant (PR). The dynamics of both the types' current controller with the proposed hybrid grid synchronization principle during the faults will be tested and compare with that of conventional technique. More precisely, evaluations will be performed on the basis of frequency adaptability of the resonant controller. The conventional way of feeding the resonant controller is with the SRFPLL estimated frequency. On the contrary, the proposed hybrid grid synchronization will enable hybrid frequency estimator (refer Chapter 4) to feed the resonant controller.

The asymmetry considered for the fault is of Type-C which corresponds to a phase-phase faults [68] to evaluate the FRT. The sag depth is created as 90% in phase B and phase C with a PAJ of -45°. Details of the controller implementations along with the simulation and experimental results are discussed below.

5.7.1 Current control with PIR$_2$ controller

The control loop for the grid current using the PIR$_2$ controller during the FRT of VSC for the asymmetrical grid fault is shown in Figure 5.17. Unlike the dual *dq*-frame PI controller, this type of current controller does not require any sequence component extraction of the grid current during the grid voltage unbalance. Hence, in this case, extra time delay involving the sequence component extraction of the grid current is avoided. Using the PIR$_2$ controller no compromise to the transient stability of the grid current is done. Use of the resonant controller in the stationary reference frame in parallel to the PI controller has gained popularity as the R pole can exactly provide a zero error (infinite gain) at R frequency. In this chapter, the value of R is set at twice the grid frequency ($2f_g$) to eliminate the double frequency ripple in grid current. Hence, the converter will supply balanced positive sequence grid current during the fault. The current controller expression for PIR$_2$ is given by (5.26); where K_{ir} and w_r are the gain and frequency of the resonant controller.

$$G_i(s) = K_{pi} + \frac{K_{ii}}{s} + \frac{K_{ir}}{s^2 + (2w_r)^2} \tag{5.26}$$

The PIR$_2$ is designed in the positive *dq*-frame which ensures voltage and current values are DC values and are taken care of by the PI regulator. The negative sequence components are controlled by the R$_2$ regulator.

One of the issues with the resonant controller is that it is sensitive to grid frequency variations. For instance, during the off-nominal grid frequency, there is huge drop in the gain values at the cross over frequency. If the resonator is not fed with the updated frequency information, it results in poor tracking of the intended grid current. Thus, the frequency information is fed from the SRFPLL estimations during normal grid conditions. During the grid faults having PAJs the frequency oscillations increases which directly impacts such

frequency-adaptive resonant current controller. To avoid such issues, in addition to the proposed phase-angle transition, the frequency is also transited from the SRFPLL to the arctangent derived frequency during fault. The details of this hybrid frequency transition are discussed in Chapter 4.

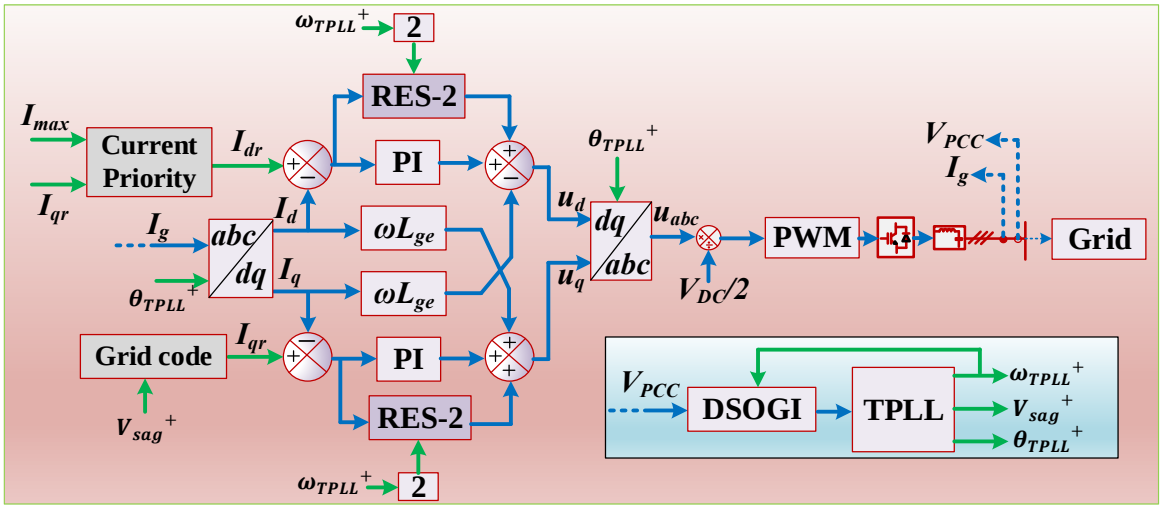


Figure 5.17: Grid current control loop using the proportional plus integral plus resonant (PIR_2) during asymmetrical grid faults.

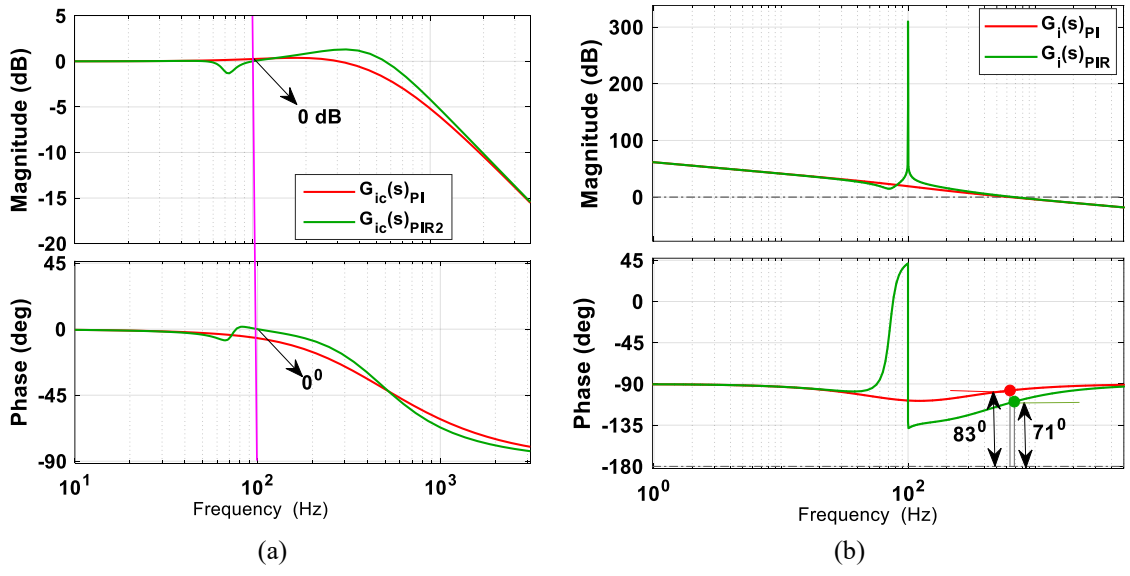


Figure 5.18: Comparison of PI and PIR_2 current controller using (a) Closed-loop bode plot and (b) open-loop bode plot.

A comparison of bode plot for PIR_2 based current controller to the PI base current controller is shown in Figure 5.18. From the closed-loop current controller bode plot as in Figure 5.18 (a), it can be observed that the resonant current controller provides 0 dB gain and 0° phase-angle error at exactly 100 Hz frequency, without having a profound effect on the PI bandwidth. On the other hand, from the open loop bode plot as shown in Figure 5.18(b), there is no significant phase margin difference observed between the two types of current controllers. Hence the PIR_2 does not affect the current controller stability as compared to the PI. Additionally, the sensitivity of the PIR_2 current controller during frequency variations is shown in Figure 5.19. There is a sharp decrease in the magnitude when the frequency changes by ±1 Hz. Thus, the resonant controller is fed with the estimated frequency rather than fixed frequency in the proposed control.

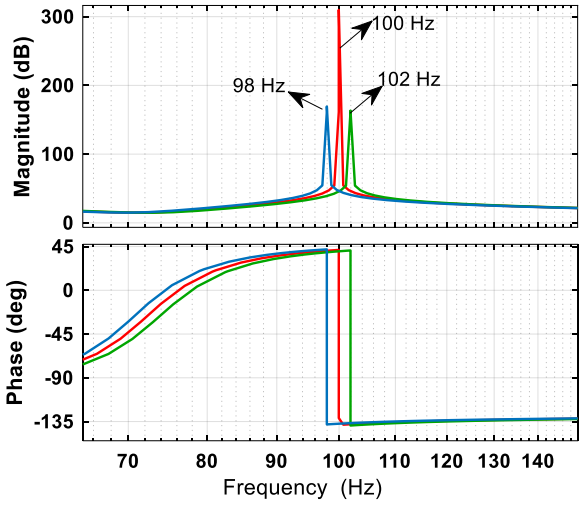


Figure 5.19: Response of PIR_2 current controller to grid frequency variations of 50±1 Hz.

As shown in Figure 5.17, using the hybrid frequency-adaptive DSOGI, the positive sequence voltage sag magnitude (V_{sag}^{+}) is calculated. It is fed to the grid code requirement based positive sequence reactive current reference (I_{qr}^{+}) calculator. The calculated I_{qr}^{+} and I_{max} decides the magnitude of I_{dr}^{+} as described for symmetrical grid faults. The grid current (I_g) is

decomposed to produce *dq*-axes components (I_{dq}) using the positive sequence hybrid phase-angle (θ_{TPLL}^{+}). The current error in *dq*-axes is fed to the proposed frequency adaptive PIR$_2$ current controller. The double frequency ripples present in both *dq*-axes components of currents are eliminated by the R$_2$ controller (fed by ω_{TPLL}^{+}). The reference negative current of the *dq*-axes components (I_{dqr}^{-}) are set to zero and only positive sequence balanced grid current is injected during the FRT.

5.7.2 Current control with PR controller

As compared to the PI or PIR$_2$ current controller PR controller has more flexibility to control the grid current during asymmetrical grid fault scenarios. In this control, the grid current undergoes only Clarke transform. It does not need the phase-angle information. The current tracking happens in the form of sinusoids as PR controller is itself a sinusoidal regulator. It can regulate the positive and negative sequence currents simultaneously unlike the dual *dq*-frame based PI current controller. In fact, PR controller is the combination of the PI controller both in positive and negative *dq*-frames.

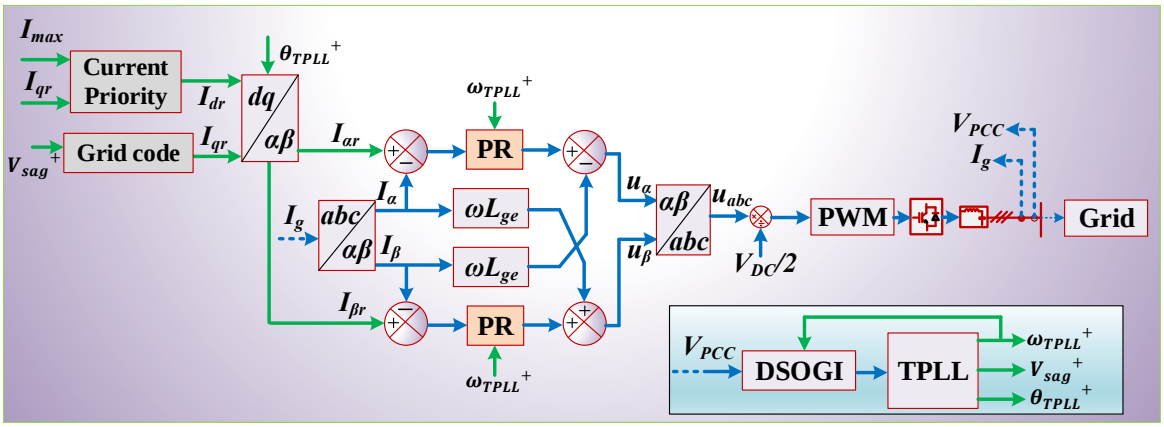


Figure 5.20: Grid current control loop using the proportional plus resonant (PR) controller during asymmetrical grid faults.

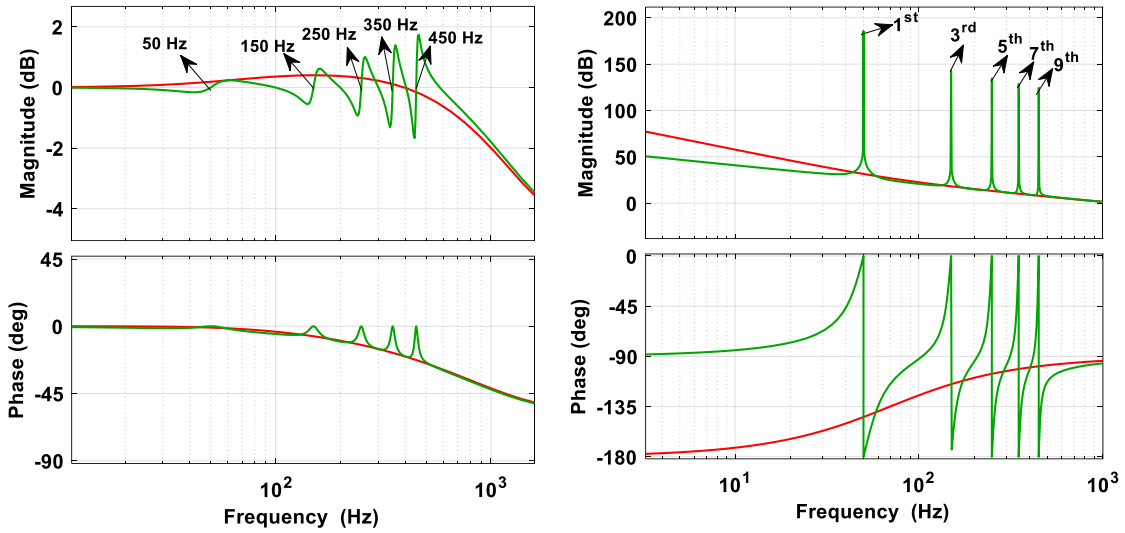
As discussed in PIR_2, PR current controller is also sensitive to grid frequency variations. Usually the frequency is fed from the SRFPLL to make the PR current controller frequency-adaptive. As explained previously, during the PAJ, such frequency feedback degrades the response speed of the current controller and hence the FRT of the VSC.

To avoid this issue, the hybrid frequency estimator is used for the frequency-adaptive PR current controller during the FRT. The control system for the proposed technique is shown in Figure 5.20. The frequency and phase-angle information required for the current controller is replaced by the proposed hybrid grid synchronization estimated frequency ($\omega_{TPLL}{}^{+}$) and phase-angle ($\theta_{TPLL}{}^{+}$) respectively. The PR current controller implemented here is chosen only at 50 Hz crossover frequency. One of the issues of such PR current controllers centred at the fundamental frequency is the sensitivity to the grid harmonics. Hence, parallel harmonic compensators (HCs) are implemented and centred at particular harmonic frequencies. The bode plot comparison of PI and PR+HCs current controllers having the same bandwidth is shown in Figure 5.21. It can be seen that unlike PI, the PR+HCs selectively controls the grid frequency components such as fundamental (1st), 3rd, 5th, 7th and 9th harmonic. The current controller expression for PR is given by (5.27); where K_{ir} and w_r are the gain and frequency of the resonant controller for fundamental component, while K_{irh} and $w_{rh} = hw_r$ are the gain and frequency for various harmonic components.

$$G_i(s) = K_{pi} + \frac{K_{ir}}{s^2 + (2w_r)^2} + \sum_{h=3,5,7,9} \frac{K_{ih}}{s^2 + (w_{rh})^2} \tag{5.27}$$

The sensitivity of the PR current controller to grid frequency variations is shown in Figure 5.22. It can be seen that with the change in fundamental frequency from 50 to 51 Hz, the gain reduces from 186 dB to 167 dB. This shows that the grid current tracking with PR current

controller at fundamental frequency is not robust. This chapter only considers the short time duration grid faults and thus the HCs are not shown in the control diagram (refer Figure 5.20). The FRT strategy in terms of generation of *dq*-axes reference currents as per the grid code is followed the same way as discussed for PIR_2 during the asymmetrical grid faults with PAJs.



(a) (b)

Figure 5.21: Comparison of PI and PR current controller using (a) Closed-loop bode plot and (b) open-loop bode plot.

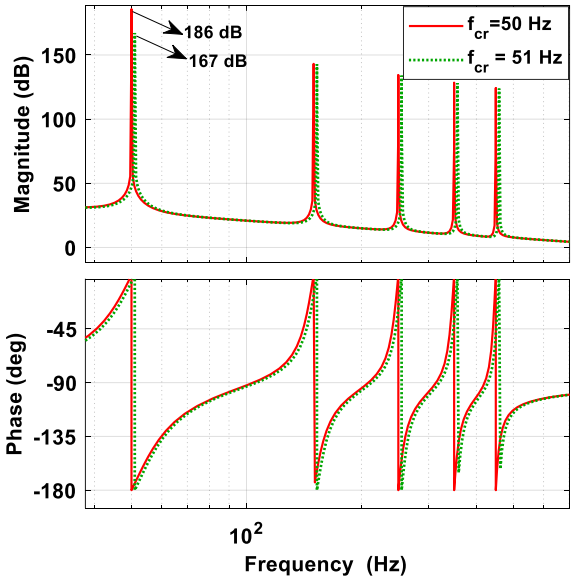


Figure 5.22: Response of PR current controller to grid frequency variations of 50+1 Hz.

5.8 Simulation and Experimental Results

The dynamic performance of the adaptive current controller with the proposed hybrid grid synchronization transition during the asymmetrical fault having voltage sag and PAJ is simulated using MATLAB/SIMULINK and PLECS Blockset. The converter and controller parameters are chosen to be the same as in case of symmetrical fault which is given in Table 5.1. As mentioned earlier, the asymmetry considered is the 90% voltage sag in Phase B and Phase C. The PAJ is chosen to be -45°.

At first, the simulation results are presented without using the R_2 controller in PIR_2 based inner current controller. The response with the conventional SRFPLL synchronized current controller along with power profiles, DC-link voltage and fault current angle dynamics is shown in Figure 5.23. The positive sequence phase-angle for frame transformation of the grid current (*abc-dq*) is extracted using the DSOGI pre-filter. In Figure 5.23 (a), the centre frequency of DSOGI filter is tuned at the nominal grid frequency i.e., 50 Hz; instead the frequency feedback from the PLL assuming the grid voltage frequency is unaltered during fault. This is conducive to the smooth FRT of the VSC during both fault inception and fault recovery using DSOGIPLL based grid synchronization. On the other hand, during the FRT period, the grid current is observed to be unbalanced as it contains both positive and negative sequence components. The steady-state ripples in the I_d and I_q are observed to be $8A_{p\text{-}p}$. These unbalanced grid currents induce a ripple of 0.3V in the DC link voltage around its constant magnitude i.e., 400V. Due to the unbalanced grid currents, P and Q also contain steady-state ripples along with the fault current angle during the FRT period. It is noticed that the DSOGI is not influenced by the SRFPLL estimated frequency. However, the PLL in-loop delay can be observed in both current dynamics and power profiles especially during the post fault recovery instance.

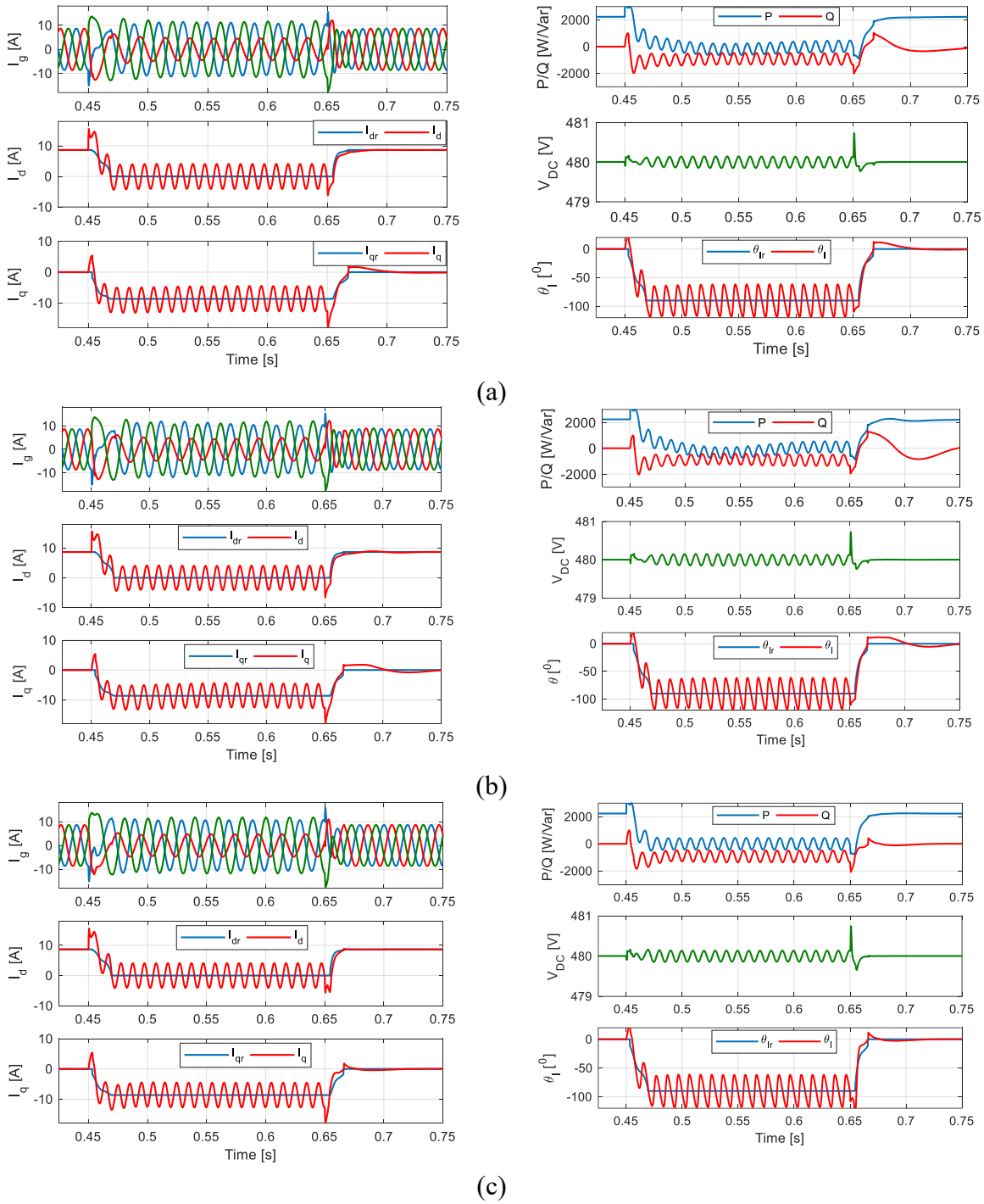
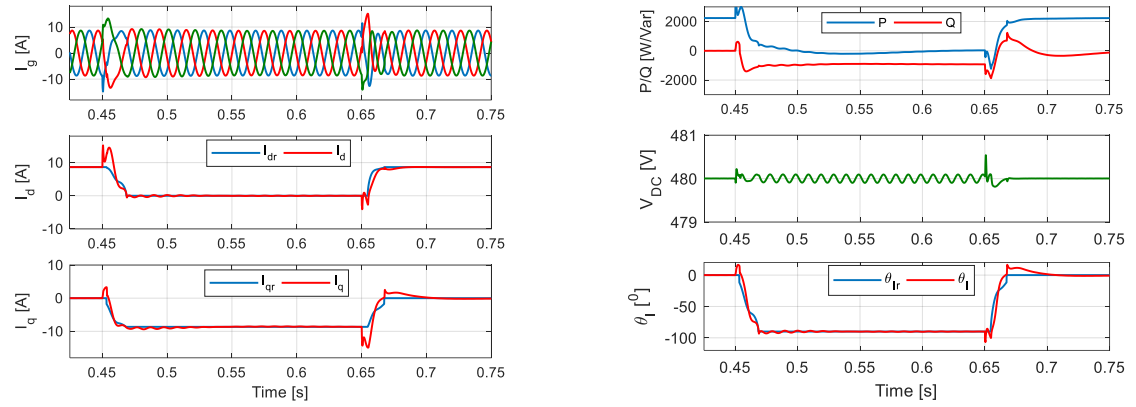


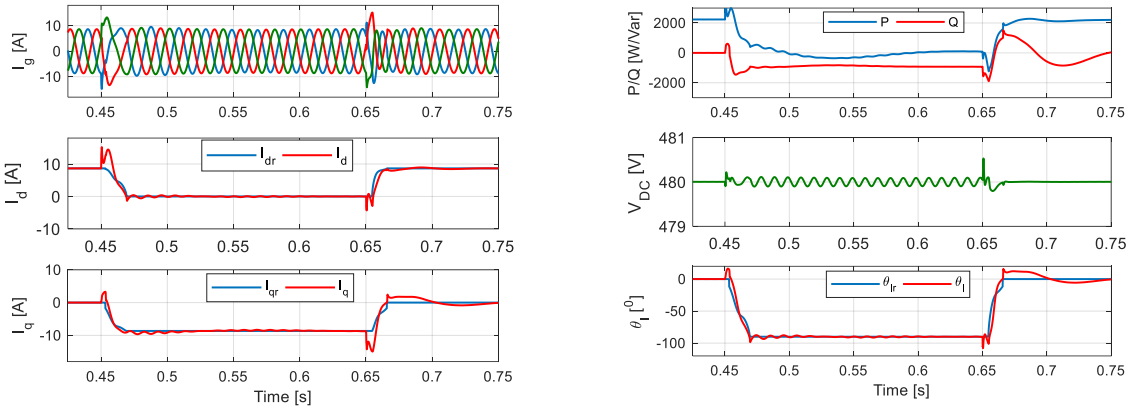
Figure 5.23: Response of PI current controller in positive dq-frame during asymmetrical grid fault (90% sag in Phase B and Phase C) with -45° PAJ using DSOGI pre-filter with centre frequency (a) tuned at 50 Hz, (b) estimated by second-order SRFPLL and (c) tuned with proposed hybrid frequency estimator.

The assumption of the grid voltage frequency to be 50 Hz as afore-mentioned may not be true always. It may fluctuate around the 50 Hz value. Hence, the tests are repeated using frequency-adaptive DSOGIPLL. The responses are shown in Figure 5.23 (b). The impact of PAJ is clearly visible during both fault inception and recovery. This slow dynamics and oscillating frequency add extra delay to the current controller. It can be seen that the I_q tracking time increases (more than 100ms) as compared to the case in Figure 5.23 (a). In Figure 5.23(c), the DSOGI is fed by the arctangent derived frequency under the hybrid grid synchronization principle. It helps in providing a better damping and thus reduces the tracking time (60 ms) for the current controller. The phase-angle also transits from the SRFPLL to the arctangent as a result of PAJ during the grid fault. The grid synchronization performance for this scenario is provided in Chapter 4.

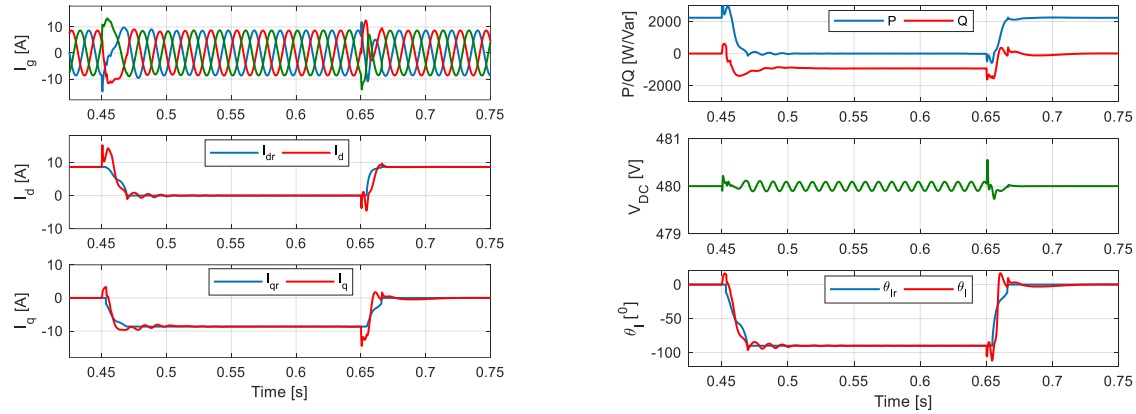
The proposed hybrid grid synchronization improved the current controller dynamics during the fault inception and recovery. It can be observed that in all the results presented in Figure 5.23 (a), (b) and (c), the steady state ripples in the current (I_g, I_{dq}, θ_l), DC-link voltage (V_{DC}) and injected P and Q could not be avoided. To mitigate this issue, only positive sequence currents need to be injected as a function of positive sequence voltage. This can be done using the sequence component extraction of the grid current to get positive sequence and negative sequence currents using the DSOGI filter. However, an extra delay is added in the current control loop. As a result, the bandwidth of the current controller is required to be compromised which is not feasible from the FRT aspect.



(a)



(b)



(c)

Figure 5.24: Response of PIR$_2$ current controller in positive dq-frame during asymmetrical grid fault (90% sag in Phase B and Phase C) with -45° PAJ, (a) frequency independent current controller, (b) frequency-adaptive with SRFPLL frequency estimation based current controller and (c) frequency-adaptive with the proposed hybrid grid synchronized current controller.

As in this chapter, only positive sequence current injection is discussed, one R_2 resonator is added in parallel to PI controller in the *dq*-frame (PIR_2) to eliminate the negative sequence component. Discussion on the implementation of the PIR_2 with the proposed hybrid synchronization is done previously. The frequency to the R_2 is initially fed with the nominal value (50 Hz) and the results are shown in Figure 5.24 (a). It provides a robust current controller performance during the FRT. During off-nominal frequency, such frequency fixed R_2 will not be able to provide the required gain to supress the double frequency ripples present in the grid current during asymmetrical grid faults. Therefore, the frequency adaptability of the resonant controller is investigated by feeding it from SRFPLL. As a consequence of PAJ, the frequency estimation from the classical second-order SRFPLL influences the current controller due to its inherent delay. The simulation results are shown in Figure 5.24 (b). The settling time of I_q is observed to increase from 50 ms to more than 100 ms during the fault inception and recovery time. Such delay is also reflected on the *P* and *Q* profiles. As observed in Figure 5.24(c), for the proposed technique, the delay time is around 60 ms. It maintains a trade-off between the frequency independent and adaptive (with SRFPLL frequency estimation) behaviour of PIR_2 current controller during the FRT. The ripple in the V_{DC} in all the three cases are observed to be 0.18V, which is lesser than those dynamics discussed in Figure 5.23 without the use of R_2 controller.

The performance of frequency-adaptive PIR_2 with SRFPLL frequency estimation is compared with proposed hybrid grid synchronization during asymmetrical FRT using an experiment setup. The results are presented in Figure 5.25. It can be observed from Figure 5.25 (b) that the frequency adaptability of PIR_2 inner current controller is enhanced with the proposed technique as compared to the SRFPLL (Figure 5.25 (a)). The tracking time observed during experiments matches with those obtained with the simulation analyses.

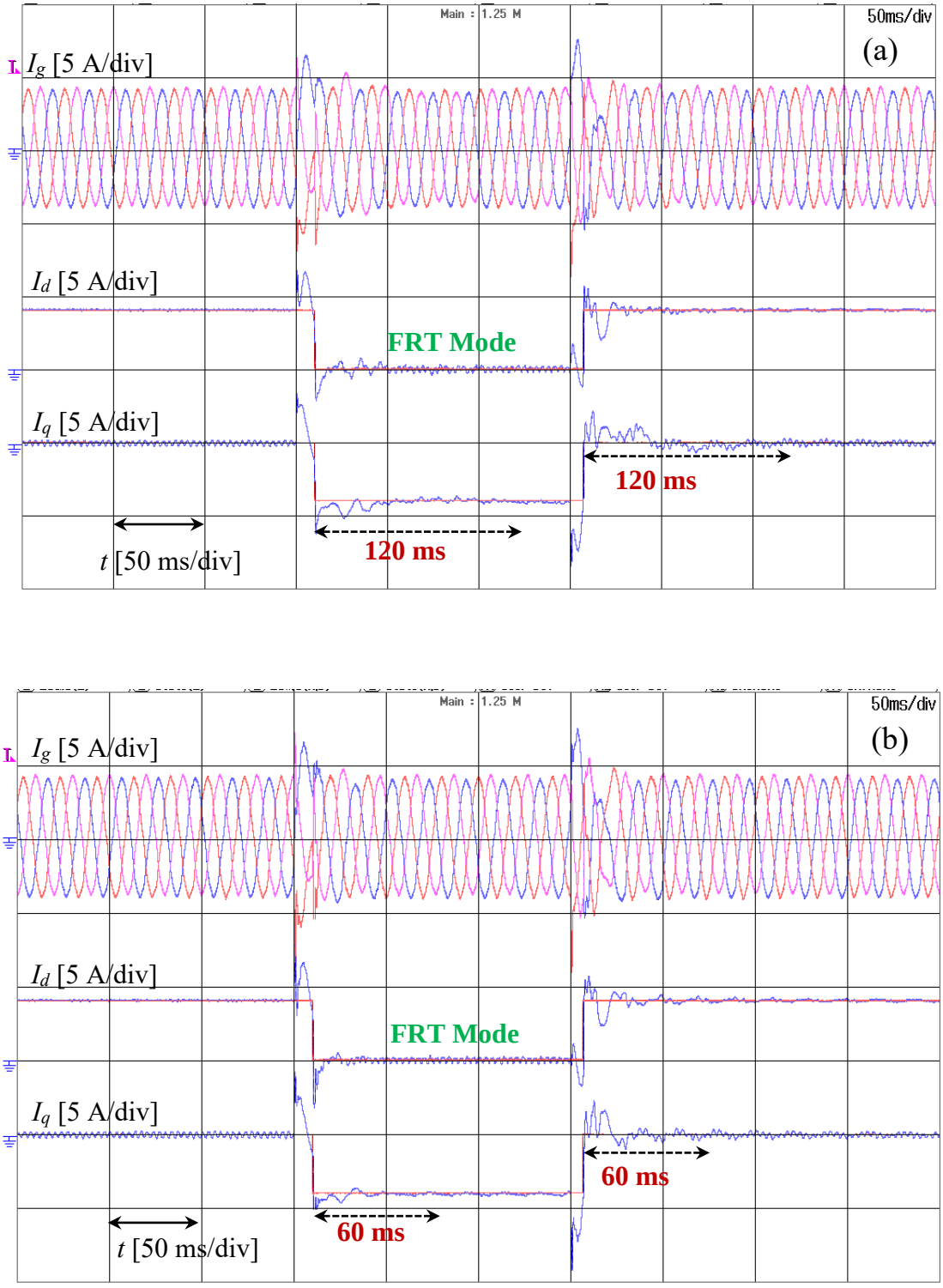
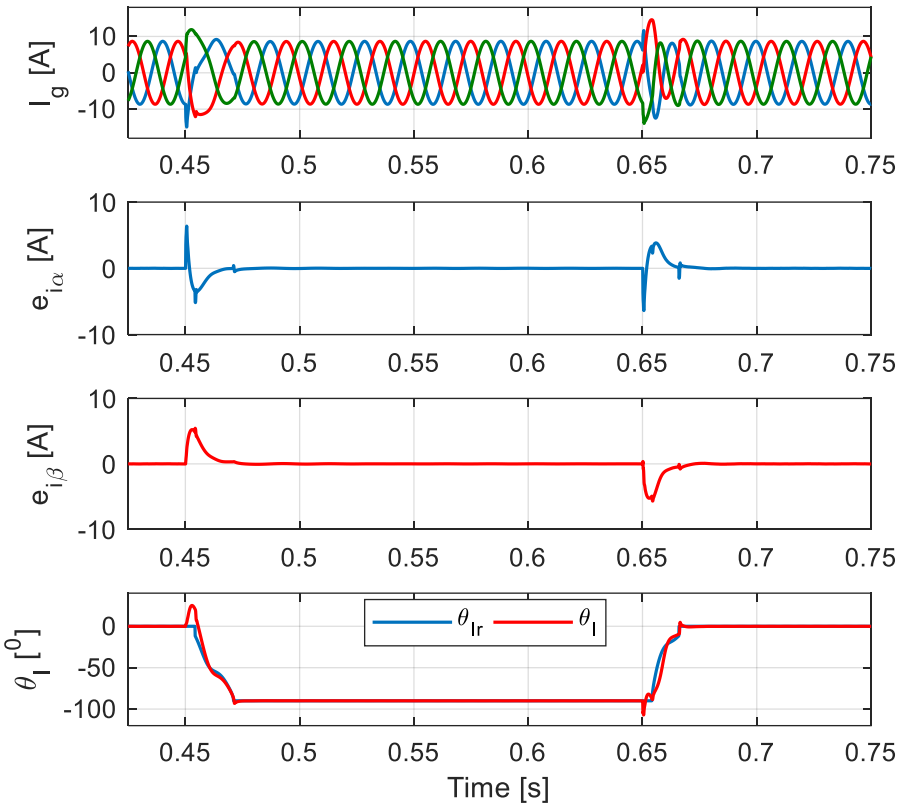
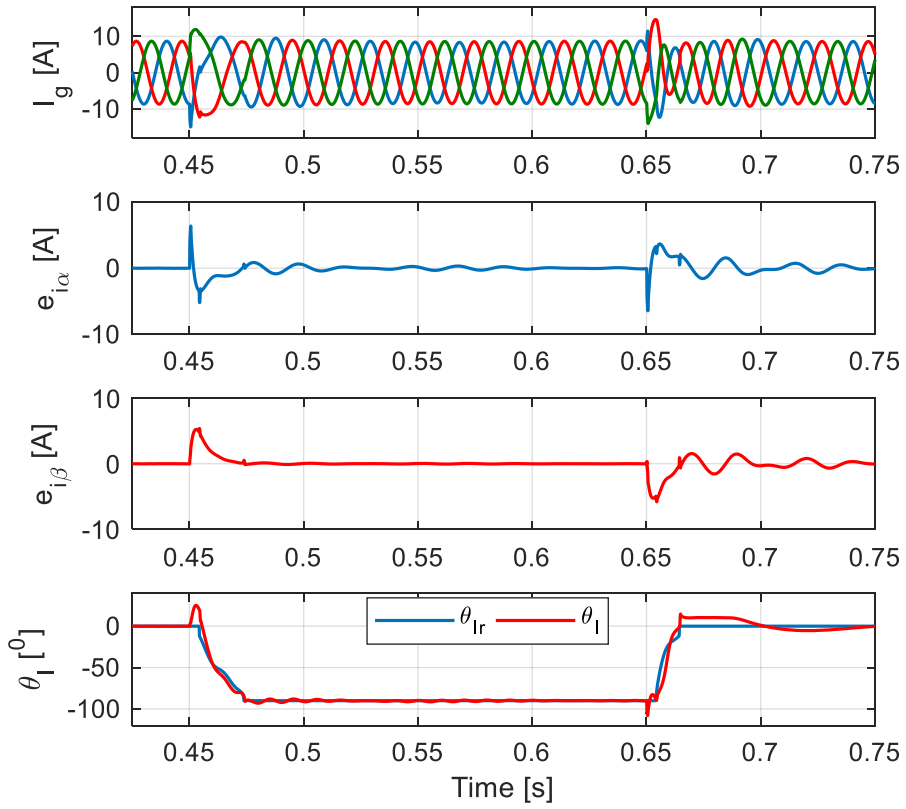


Figure 5.25: Experimental validation of response of PIR_2 current controller in positive dq-frame during asymmetrical grid fault (90% sag in Phase B and Phase C) with -45° PAJ, (a) frequency-adaptive with SRFPLL frequency estimations current controller and (b) frequency-adaptive with proposed hybrid grid synchronized current controller.

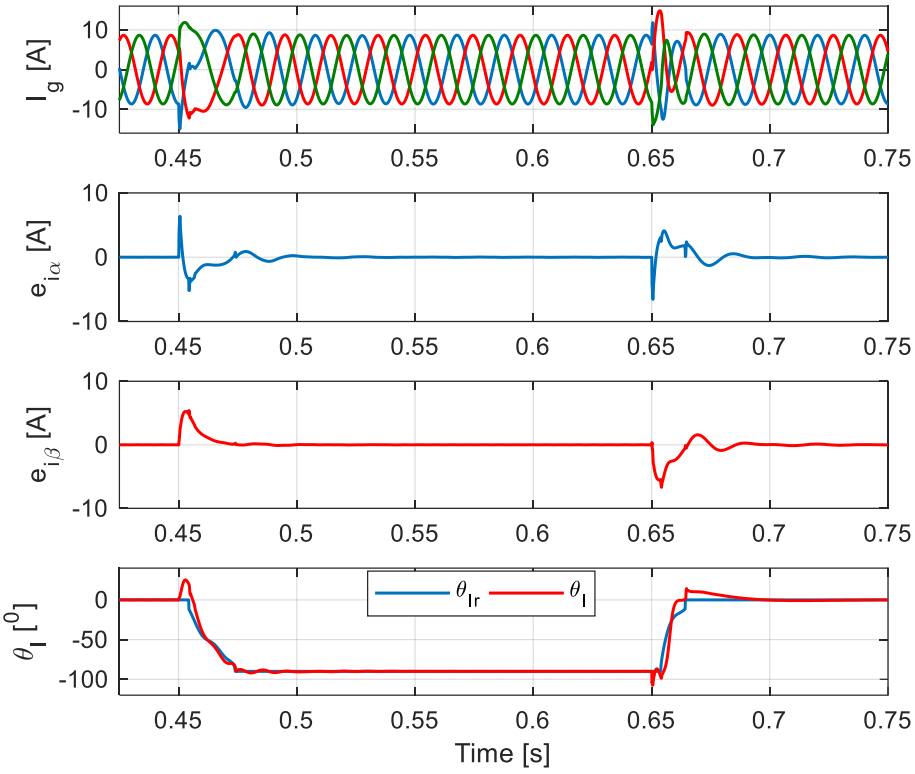
The dynamics of the grid current during the asymmetrical grid fault is tested using PR controller in the $\alpha\beta$-frame. The asymmetry considered is same for PIR_2 current controller. The current controller gain parameters are also kept unchanged for a fair comparison. In this case, the grid current is only frame transferred from *abc*-$\alpha\beta$. However, as discussed previously, these types of controllers selectively control the grid current frequency components and thus need to be frequency-adaptive in order to avoid steady-state tracking error. Three case scenarios are tested in regards to the frequency adaptability of the resonant controller. They are: a) frequency independent, b) frequency-adaptive with SRFPLL frequency estimation and c) frequency-adaptive with proposed hybrid grid synchronization. Grid current (I_g), tracking error in $\alpha\beta$-components of grid currents ($e_{i\alpha}$ (= $i_{\alpha r}$ - i_α), $e_{i\beta}$ (= $i_{\beta r}$ - i_β)) and the fault current angle (θ_I) are considered for comparisons. Initially, frequency independent PR current controller is tested during the FRT and response is shown in Figure 5.26 (a). It can be seen that the tracking time is least influenced by the estimated frequency dynamics by SRFPLL as a result of PAJ. It provides a tracking time of around 30ms for both $\alpha\beta$-axes current components. On the other hand, by making the PR current controller frequency-adaptive (estimated by SRFPLL) there are steady-state ripples observed during the FRT period. The tracking time is observed to be around 150ms as shown in Figure 5.26 (b). The total delay is the contribution of DSOGI filter and SRFPLL in loop delay. This delay is minimised by using the proposed hybrid grid synchronized based frequency-adaptive PR current controller as shown in Figure 5.26 (c). The tracking delay is found to be around 50 ms. This lies between the frequency independent and SRFPLL estimated frequency-adaptive PR current controller tracking time. Hence such adaptive current controller is observed to provide a faster FRT dynamics during grid faults having PAJ. It can also track the grid frequency and current error more robustly by switching back to the DSOGIPLL frequency estimation once the grid recovers the normal operating conditions.



(a)



(b)



(c)

Figure 5.26: Response of PR current controller in αβ-frame during asymmetrical grid fault (90% sag in Phase B and Phase C) with -45° PAJ (a) frequency independent current controller, (b) frequency-adaptive with SRFPLL frequency estimations current controller and (c) frequency-adaptive with proposed hybrid grid synchronized current controller.

The current controller dynamics using the PR regulator during the asymmetrical FRT is also validated using experimental results as shown in Figure 5.27. The grid current and error in the *αβ*-axes components are considered for comparison. The increased frequency oscillations by the SRFPLL estimation during the PAJ are observed in the current tracking error as in Figure 5.27 (a). The error tracking time is reduced using the hybrid frequency and phase-angle estimator based hybrid grid synchronization as shown in Figure 5.27 (b).

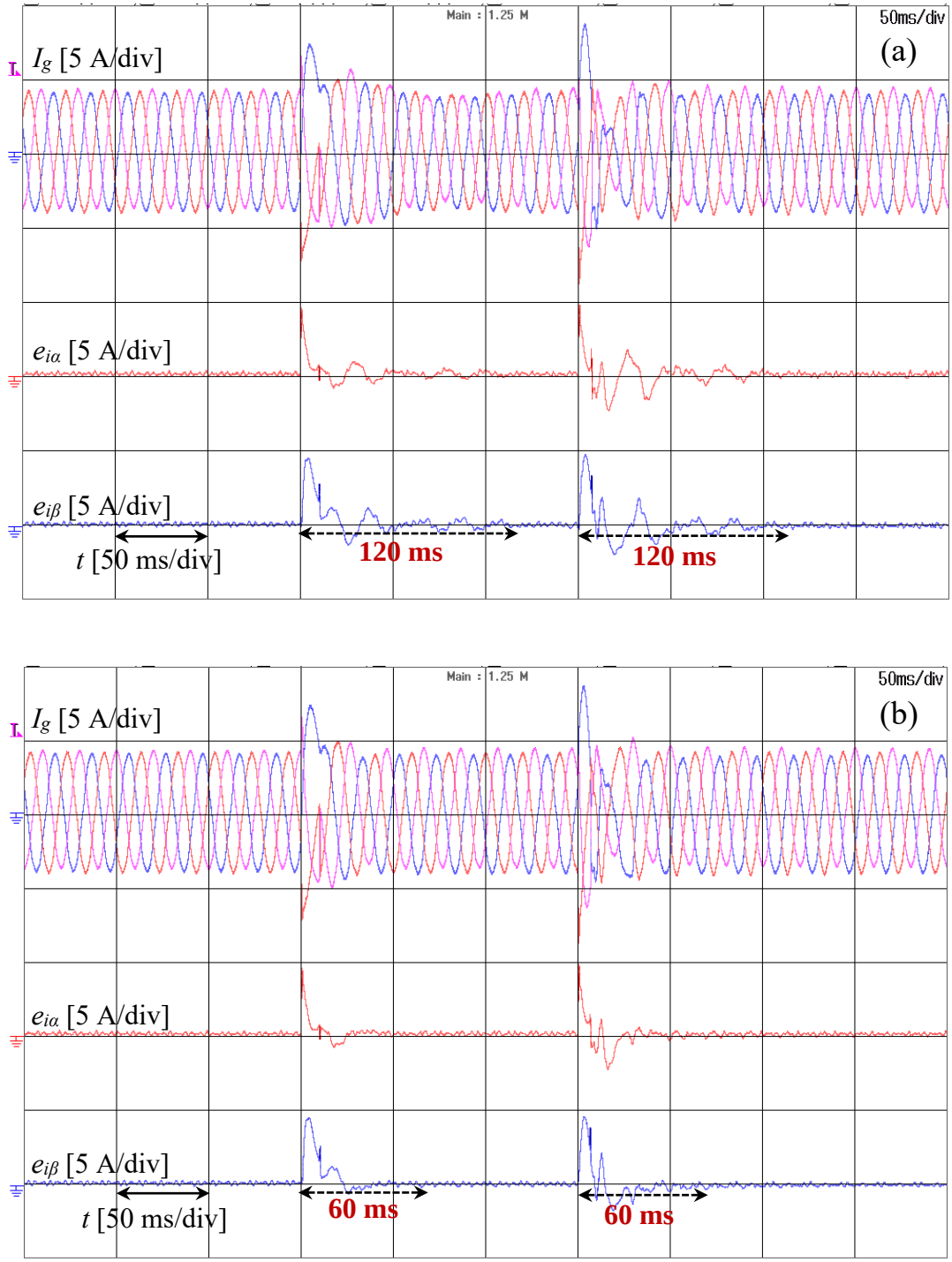


Figure 5.27: Experimental validation of response of PR current controller in αβ-frame during asymmetrical grid fault (90% sag in Phase B and Phase C) with -45° PAJ (a) frequency adaptive with SRFPLL frequency estimations current controller and (b) frequency adaptive with proposed hybrid grid synchronized current controller.

5.9 Chapter Summary

This chapter utilizes the concept of hybrid grid synchronization in designing different inner current controller for enhanced FRT of VSC during grid faults. The proposed adaptive current controllers are implemented with the FRT strategy during the fault. The grid faults considered for study are both symmetrical and asymmetrical types. In addition to the voltage sag, PAJ are also considered during the fault inception and recovery.

The above contributions are addressed by initially explaining the reduced order switching model of a three-phase grid-connected VSC under study. It includes grid synchronization, plant (*LCL* filter) model, Thevenin's equivalent grid model, pulse width modulation, outer DC link voltage control, and inner current control. Special attention is given to the impact of voltage feedforward compensation and SRFPLL based grid synchronisation dynamics on the inner current control loop. This impact is considered during the FRT, which includes the reactive current injection in relation to the grid voltage sag depth during the fault.

The FRT of the VSC synchronized with the classical second-order SRFPLL is tested and compared with the proposed hybrid grid synchronized VSC during symmetrical faults having PAJs. The comparisons are done with and without the addition of voltage feedforward compensation during FRT. Scenarios involving loss of grid synchronization due to the small-signal instability of SRFPLL as a result of PAJ is also considered. Adaptability of the proposed hybrid grid synchronisation in such a scenario is discussed. Comparisons are also made with other adaptive SRFPLL techniques. It is shown that the proposed hybrid grid synchronization improves the current controller dynamics in synchronous reference frame (*dq*-frame) during the FRT especially when the grid fault includes PAJ.

During asymmetrical FRT, PIR_2 and PR current controller are used to inject positive sequence grid currents by extracting positive sequence PCC voltage using the adaptive

DSOGI pre-filter. The frequency adaptability of the resonant controllers is enhanced during FRT by replacing the SRFPLL estimated frequency feedback with the proposed hybrid frequency estimations. The performance enhancement of the proposed adaptive current controller over the conventional techniques during the FRT is presented using both simulation analyses and experimental validations. A summary of the current controller performance during FRT with both the conventional and proposed grid synchronization when subjected to various grid faults is provided in TABLE 5.2. '✔' refers to the robust, '✔✔' refers to the robust and recommended and '✖' refers to the poor and not recommended.

TABLE 5.2: SUMMARY OF ADAPTIVE CURRENT CONTROLLER PERFORMANCE OF THREE-PHASE CONVERTER WITH THE HYBRID GRID SYNCHRONIZATION TECHNIQUE DURING FAULT RIDE-THROUGH.

	Grid Synchronization Technique				Current Controller for improved FRT		
Fault Type	SRFPLL	DSOGIPLL	TPLL	DSOGI+TFLL	PI	PIR_2	PR
Symmetrical (Voltage Sag)	✔	NC	NC	NC	✔	NC	NC
Symmetrical (Voltage Sag + PAJ)	✖	NC	✔	NC	✔	NC	NC
Asymmetrical (Voltage Sag)	✖	✔	NC	NC	NC	✔	✔✔
Asymmetrical (Voltage Sag + PAJ)	✖	*✔/✖	**✔	✔✔	NC	✔	✔✔

NC: Not Considered in this Study, **SRFPLL**: Synchronous Reference Frame Phase-Locked Loop, **DSOGIPLL**: Dual Second-order Generalized Integrator PLL, **TPLL**: Transition Phase-locked Loop, **DSOGI+TFLL**: DSOGI with Transition Frequency locked-Loop, **PI**: Proportional plus Integral, **PIR_2**: PI plus Second Resonant, **PR**: Proportional plus Resonant.

* DSOGIPLL can work well with either PIR_2 or PR current controller during asymmetrical grid fault with PAJ and FRT if the resonant controllers are made frequency independent.

** TPLL can provide robust FRT without the need of DSOGI+TFLL, with either PIR_2 or PR current controller during asymmetrical grid faults with PAJ, if the resonant controllers are made frequency independent.

Chapter 6

Fault Ride-Through of Single-Phase Power Converters

Grid frequency adaptability of the proportional and resonant (PR) current controller is essential to avoid any steady-state error during off-nominal frequency variations. Single-phase grid-connected converters use the estimated frequency from the second-order generalized integrator phase-locked loop (SOGIPLL), as feedback to the PR controller. Such frequency feedback degrades the current controller's performance when the converter is exposed to grid fault having phase-angle jumps (PAJs). This highly affects the fault ride-through (FRT) capability of the converter. To deal with this, enhanced frequency-adaptive PR current controller is proposed in this chapter. The objective of the proposed technique is to create a PLL independent frequency estimation technique for the PR controller during the grid faults involving PAJs. The frequency adaptability of the PR controller is governed by the hybrid grid synchronization principle. The dynamic performance of the grid current, controlled with the proposed technique, while providing FRT during the grid fault having PAJ is investigated. Its efficacy is determined using simulation analysis and by comparing it with a conventional technique.

6.1 Introduction

To meet the stringent modern grid code compliances imposed by various countries, the grid feeding converters are expected to serve two main purposes. They are: i) provision of fault/low voltage ride-through (FRT/LVRT) capability [160] and, ii) maintaining the power quality of the injected grid current [3]. Both the purposes can be met by improved grid synchronization strategies and robust current controller design. In case of single-phase converters, PR controller is chosen over PI to avoid any frame transformations of the measured grid current. The resonators in PR controllers are tuned at the centre frequency to track the sinusoidal reference accurately [161]. When the centre frequency is estimated by an additional frequency estimator, they are called as frequency-adaptive resonators. The frequency-adaptive PR current controllers are sensitive to the frequency fluctuations [162]. Any steady-state frequency error results in the poor tracking of the grid current. The frequency to be fed to the PR current controller is usually estimated by the grid synchronization unit.

Most widely used grid synchronization unit for the single-phase grid-connected converter is the second-order generalized integrator based phase-locked loop (SOGIPLL) [136]. It provides a good trade-off between the steady-state performance and harmonic rejection capability [137]. As explained in Chapter-4, it includes two feedback paths during grid synchronization. One is for the estimated frequency to feed the SOGI and the other is the estimated phase-angle for Park's transformation and current control. Presence of such feedback paths makes it a closed-loop control structure. Hence it is sensitive to grid voltage transients such as voltage sag, PAJs and frequency variations [142]. Further, the PLL gains are tuned under the assumption of the sine of the phase-angle error to the absolute value [131]. During a grid fault, mainly a large PAJ, such linearized approximation of the

trigonometric function becomes invalid. This greatly impacts the estimated grid frequency by PLL due to its coupling with the estimated phase-angle. This in turn drives the synchronised converter into the loss of synchronism (LOS) for a longer time. Such synchronization delays degrade the FRT/LVRT capability of the converters.

6.1.1 Contribution and Organization of this Chapter

This chapter explores the FRT of single-phase grid-connected power converters during grid faults having PAJs. Initially, a reduced-order converter model is presented in Section 6.2. The frequency adaptability of the PR current controller using SOGIPLL grid synchronization is explained in Section 6.3. A scenario of off-nominal grid frequency variation is presented to demonstrate the need for the frequency adaptability of the PR current controller to ensure robust performance. Additionally, the proposed enhanced frequency-adaptive PR current controller techniques under the hybrid grid synchronization principle are detailed. Section 6.4 investigates the dynamic performance of the conventional SRFPLL frequency-fed PR current controller during grid faults in the scope of FRT capability. This study reveals the necessity for the proposed enhanced frequency-adaptive PR current controller. The comparisons between the proposed and the conventional frequency-fed PR current controller responses during common grid fault are demonstrated with simulation analysis. Finally the results of this chapter are summarised in Section 6.5.

6.2 System Description

6.2.1 Single-phase Converter Model in Stationary Reference Frame

The schematic of the single-phase grid connected converter is shown in Figure 6.1. It consists of both power and control circuits. The single-phase converter is fed with a DC-link voltage. Usually, the DC-link voltage is controlled to the reference voltage set by the maximum power point tracking (MPPT) principle for solar (PV) applications. As discussed previously, the DC-link voltage control is performed using a proportional and integral controller. It is considered as the outer loop control. In this study, the DC-link voltage is represented by a constant DC voltage source assuming the reduced order model (different time-scale based control layer). The input DC power is converted to AC power with the help of single-phase voltage source converter (VSC). The switching harmonics at the output of the converter (inverter) is supressed by the use of *LCL*-filter. The resonant frequency and the gain for the *LCL*-filter are already explained in Chapter-5. The converter is connected to the Thevenin equivalent model of the grid through the equivalent grid impedance. The single-phase voltage and current is measured at the point of common coupling (PCC) which is separated from the grid point via grid impedance. For the fault ride-through study, the fault is assumed to occur at the grid voltage.

The measured grid voltage and the current at the PCC (V_{PCC} and I_g) are sampled using analog-to-digital (ADC) converter for control purposes. The control circuit is implemented in the discrete domain. The converter control under study consists of grid synchronization, sag detection, reference current generation and the FRT/LVRT unit. In this chapter, the conventional second-order generalized integrator phase-locked loop (SOGIPLL) is replaced by the proposed adaptative frequency-fed SOGI based techniques. The details of the proposed single-phase grid synchronization techniques are provided in Chapter-4. The hybrid

grid synchronization transition principle is embedded in the control of single-phase converter in this chapter. With the transition scheme, switching between the conventional SOGIPLL and the proposed technique is done for frequency and phase-angle estimation depending on the grid conditions.

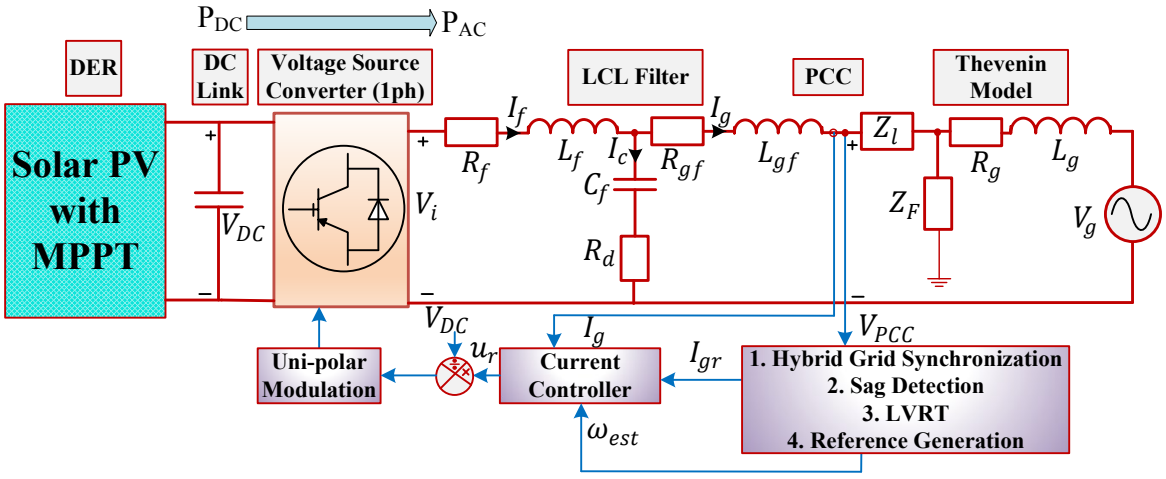


Figure 6.1 Schematic of a single-phase grid-connected converter.

The hybrid grid synchronization will also provide the sag information that will control the LVRT via reactive current injection. Voltage sag is the measure of the grid voltage fault level at the PCC. Another important aspect during the LVRT of a single-phase converter is the reference current generation. During fault, it is usually decided by the LVRT curve. The details of reference current generation strategy implemented will be demonstrated in the following sub-section. The reference current generated is fed to the inner current controller to generate the reference voltage. This will further be used for the generation of pulses for the converter switches. The current controller for single-phase converter can be implemented using proportional plus integral (PI) or proportional plus resonant controller (PR). Unlike the three-phase system, single-phase grid current requires an additional quadrature signal generator for Clarke's transform and then it needs the Park's transform as well to generate the

dq-components of grid current control for PI controller. In contrast the PR controller directly uses the measured and sampled sinusoidal grid currents without the need of any frame transformations. To avail this feature, this chapter discusses the FRT of single-phase converter using PR current controller. The advantages and disadvantages of frequency adaptability of the PR current controller will be explained in the following sub-section. The reference voltage from the output of the PR current controller is used for uni-polar modulation strategy to generate gate pulses [163].

6.2.2 Reference Current Generation

a) PQ-theory based

The instantaneous *PQ*-theory based reference current generation uses the Clarke's transformation of the measured voltage and current signals. This theory is generally implemented for three-phase systems [164]. In single-phase systems, the generation of *αβ*-components of both voltage and current signals require the implementation of additional quadrature signal generator (QSG). Thus, with the implementation of suitable QSG techniques, the *PQ*-theory is adapted for single-phase systems for reference current generation [165].

Based on the *PQ*-theory, for single-phase system, the active power (*P*) and reactive power (*Q*) expressions can be given by

$$P = \frac{1}{2}\left(V_\alpha I_\alpha + V_\beta I_\beta\right) \tag{6.1}$$

$$Q = \frac{1}{2}\left(V_\beta I_\alpha - V_\alpha I_\beta\right) \tag{6.2}$$

where $V_{\alpha\beta}$ and $I_{\alpha\beta}$ are the QSG output for measured voltage and current at the PCC. From (6.1) and (6.2), the expression for I_α can be deduced by performing inverse matrix operation and is given by

$$I_{gr} = I_\alpha = \frac{2}{{V_\alpha}^2 + {V_\beta}^2}\left(V_\alpha P + V_\beta Q\right) \tag{6.3}$$

It should be noted that as the measured grid current is a single-phase signal, the only control variable for current controller, I_α is considered as the reference current (I_{gr}). In (6.3), the values of P and Q during faults are decided by the FRT requirement as given by

$$Q = \begin{Bmatrix} 0, V_{sag} > 0.9 \\ k \times Q_{max}\left(1 - V_{sag}\right), 0.5 < V_{sag} < 0.9 \\ Q_{max}, V_{sag} < 0.5 \end{Bmatrix} \tag{6.4}$$

$$P = \sqrt{{S_{max}}^2 - Q^2} \tag{6.5}$$

where S_{max} is the maximum capacity of the power converter. The schematic of the reference current generation implementation based on *PQ*-based theory that follows (6.3) is given in Figure 6.2.

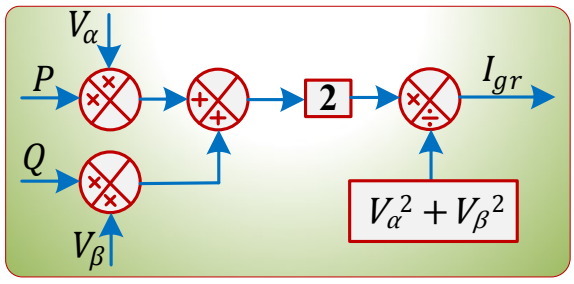


Figure 6.2 Schematic of reference current generation based on PQ-based theory.

b) Voltage-Current Phasor based

Another technique of reference current generation for single-phase converter's PR current controller, uses phasor relationship between the single-phase measured grid voltage and current. The basic understanding is the estimation and update of the phase-angle of the grid current to be injected to the grid depending on its operating conditions. Using the phasor analysis, the expression for the reference grid current is given by

$$I_{gr} = |I| \cos(\omega t + \theta + \theta_I) \tag{6.6}$$

$$|I| = \sqrt{{I_{dr}}^2 + {I_{qr}}^2} \tag{6.7}$$

$$\theta_I = \tan^{-1}\left(\frac{I_{qr}}{I_{dr}}\right) \tag{6.8}$$

Here $|I|$ is the magnitude of the maximum current capacity of the power converter ($|I|$=I_{max}). θ_I is the corresponding phase-angle between them. I_{dr} and I_{qr} are the reference currents in *dq*-axes which are mainly decided by the FRT based current injection strategies, as given by

$$I_{qr} = \begin{Bmatrix} 0, V_{sag} > 0.9 \\ k \times I_{qmax}(1 - V_{sag}), 0.5 < V_{sag} < 0.9 \\ I_{qmax}, V_{sag} < 0.5 \end{Bmatrix} \tag{6.9}$$

$$I_{dr} = \sqrt{{I_{max}}^2 - {I_{qr}}^2} \tag{6.10}$$

The schematic of the reference current generation using the phasor analysis is shown in Figure 6.3. In this chapter, the voltage-current phasor based reference current generation is

used during the FRT analysis. This technique does not require Park's transform of the measured grid current ($\alpha\beta$-dq).

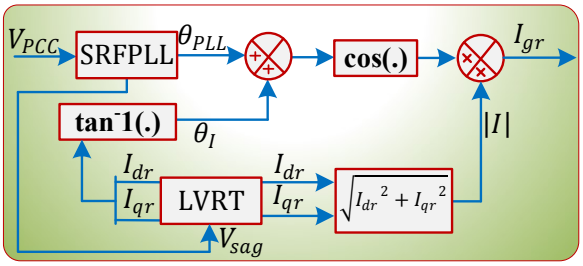


Figure 6.3 Schematic of reference current generation based on voltage-current phasor technique.

6.3 Frequency-Adaptive PR Current Controller and Fault Ride-through

As described previously, the generated reference current tracks the measured single-phase grid current using the PR controller. Unlike the PI controller, PR controller tracks the sinusoidal error. In PR current controllers the resonant frequency need to be tuned with the grid voltage frequency. A general structure of the PR current controller used in this work is shown in Figure 6.4. It uses two third-order integrators to implement its resonant structure. The schematic of the third-order integrator is shown in Figure 6.5. This integrator provides accurate tracking as compared to Euler (Backward or Forward) method of integration. It can be seen that PR current controller can be tuned at fixed grid voltage frequency (refer Figure 6.4a) or the frequency estimated by the SRFPLL (refer Figure 6.4b). The later method of implementation avoids any current tracking error during off-nominal grid frequency variations and thus makes the PR controller frequency-adaptive.

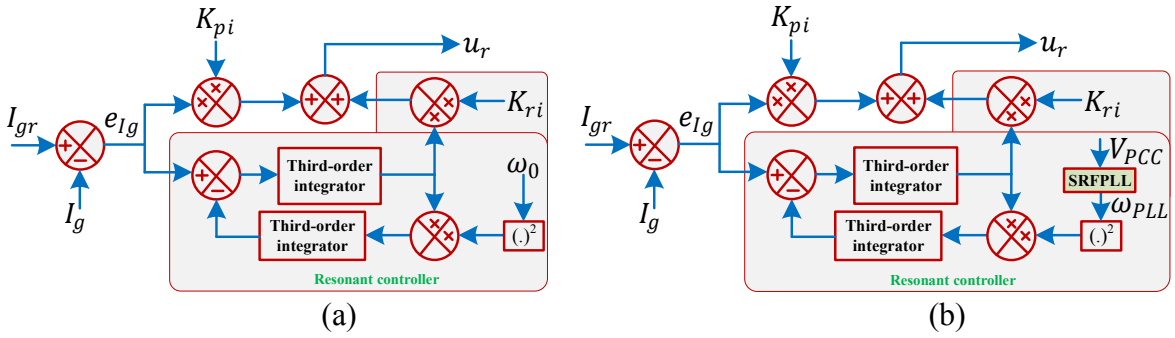


Figure 6.4 Schematic of a PR current controller: (a) frequency independent and (b) frequency-adaptive.

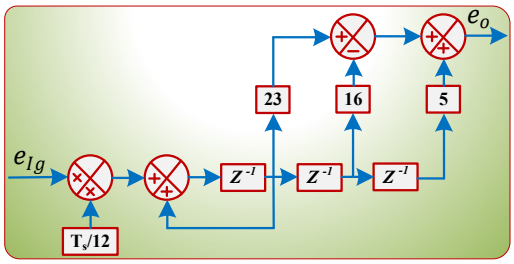


Figure 6.5 Schematic of a typical third-order integrator [136].

6.3.1 Mathematical Analysis

The expression for the PR current controller is given by

$$G_{PR}(s) = K_{pi} + \frac{K_{ri}s}{s^2 + {\omega_0}^2} \tag{6.11}$$

where K_{pi} and K_{ri} are the proportional and resonant gain respectively. Using this PR current controller, the simplified closed-loop transfer function can be expressed by

$$G_i(s) = \frac{I_g(s)}{I_{gr}(s)} = \frac{G_{PR}(s)G_{LCL}(s)}{1 + G_{PR}(s)G_{LCL}(s)} \tag{6.12}$$

The expression for error function is given by

$$G_{ie}(s) = 1 - \frac{I_g(s)}{I_{gr}(s)} = \frac{1}{1 + G_{PR}(s)G_{LCL}(s)} \tag{6.13}$$

The magnitude response of the $G_{PR}(s)$ is calculated as

$$|G_{PR}(j(\omega_0 + \Delta\omega)| = \sqrt{{K_{pi}}^2 + \frac{{K_{ri}}^2(j(\omega_0 + \Delta\omega))^2}{({\omega_0}^2 - (\omega_0 + \Delta\omega)^2)^2}} \tag{6.14}$$

From (6.14), the dependency of resonant part of the PR current controller can be deduced and simplified which can be given as

$$|G_R(j(\omega_0 + \Delta\omega)| = \frac{K_{ri}}{\omega_0}\left|\frac{1 + G_{\Delta\omega}}{{G_{\Delta\omega}}^2 + 2G_{\Delta\omega}}\right| \tag{6.15}$$

where $G_{\Delta\omega}$ is the relative frequency variation with respect to the actual grid frequency, i.e., $G_{\Delta\omega}$= $\frac{\Delta\omega}{\omega_0}$. It can be observed from (6.15) that, in case the grid voltage undergoes a frequency change ($\Delta\omega$), the frequency independent PR current controller suffers from a steady-state error proportional to $G_{\Delta\omega}$. The frequency-adaptive nature of a PR current controller can overcome this issue. This is illustrated with an example as shown in Figure 6.6. The grid frequency is changed from 50 Hz to 52 Hz at t = 0.35 s. The steady-state error in the grid current tracking is clearly visible in Figure 6.6(a) as it is controlled with fixed frequency tuned PR current control. In contrast, there is no steady-state error noticed in Figure 6.6(b). This is because, the resonant frequency of the PR controller is tuned at the frequency estimated by the SRFPLL.

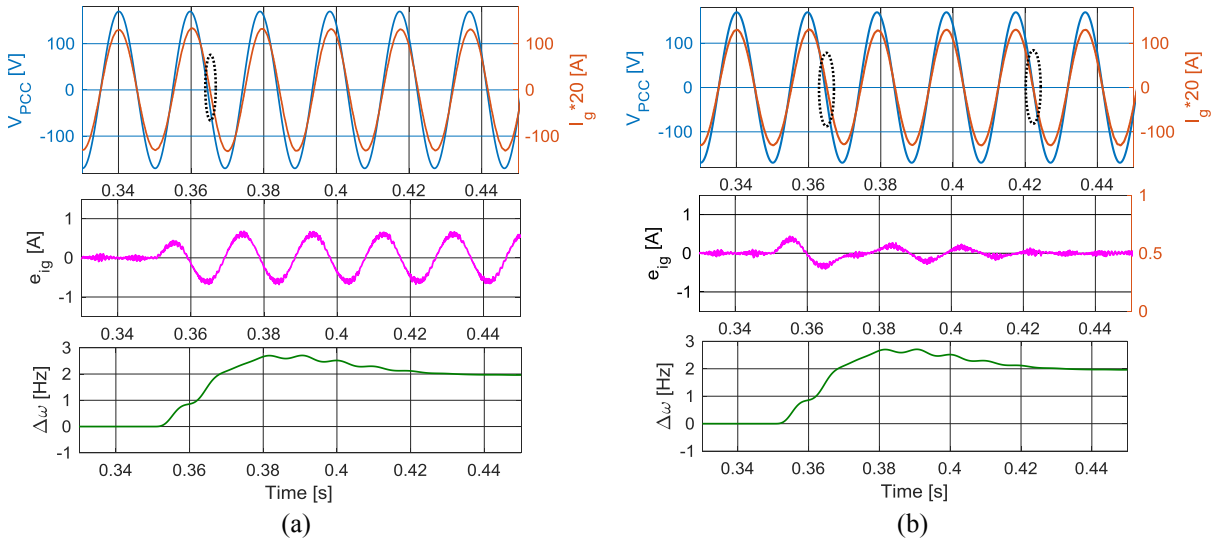


Figure 6.6 PR current controller response during grid frequency changes from 50 to 52 Hz (a) frequency independent and (b) frequency-adaptive PR controller with SRFPLL estimation.

Figure 6.6(b) shows that there is a delay in the estimation of frequency and current tracking. The delay is due to the settling time provided by the SOGIPLL used for the grid synchronization. For grid faults (which is the main objective of this thesis work), the grid voltage experiences a PAJ in addition to voltage sag. In such cases, as studied in Chapter-4, SOGIPLL estimated frequency undergoes abrupt and large oscillations. These highly impact the performance of frequency-adaptive PR current controllers. To deal with this issue, several enhanced frequency-adaptive SOGI based grid synchronization techniques replace the SOGIPLL technique. Such techniques are proposed in this thesis and have been detailed in Chapter-4. In this chapter, these techniques will be used to implement an enhanced frequency-adaptive PR current controller.

6.3.2 Proposed Frequency-Adaptive PR Current Controller

The frequency adaptability of the PR current controller fed by the conventional SRFPLL estimation (as in SOGIPLL) is enhanced by proposing three new frequency estimators for SOGI. The complete control structure showing the frequency-adaptive PR current controller along with the grid integration of the single-phase converter is shown in Figure 6.7.

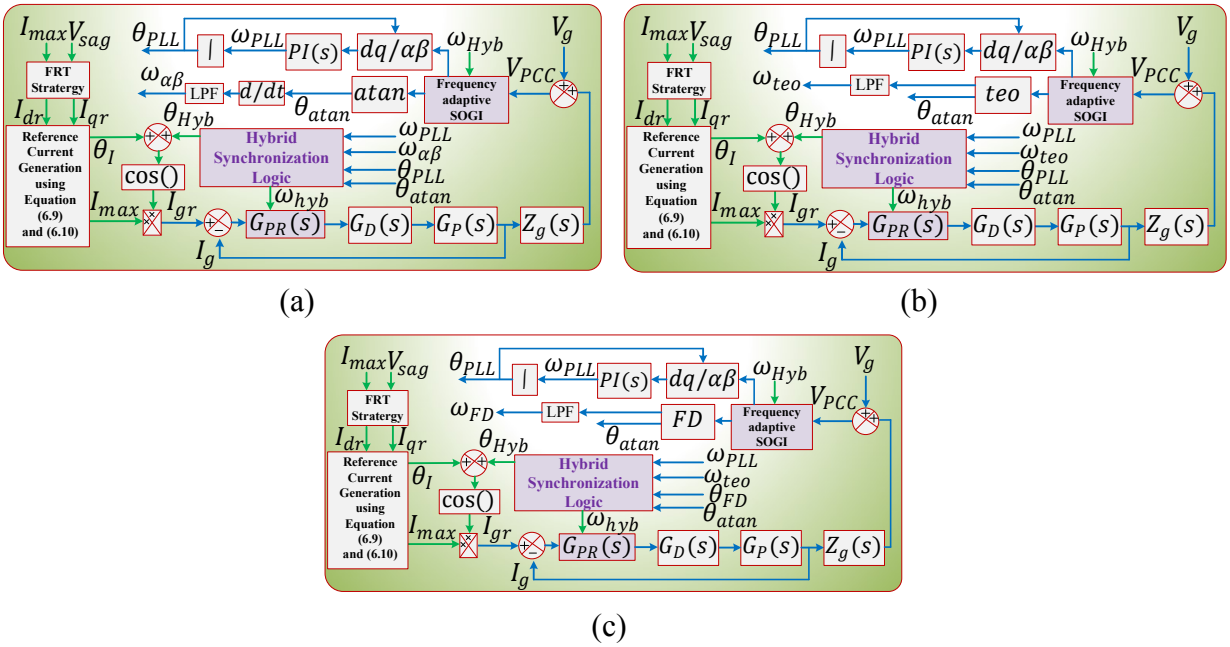


Figure 6.7 Schematic of proposed frequency-adaptive PR current controller of single-phase grid-connected power converter along with proposed hybrid grid synchronization principle: (a) Hybrid frequency estimation using the combination ω_{PLL} and $\omega_{\alpha\beta}$ [166], (b) Hybrid frequency estimation using the combination ω_{PLL} and ω_{teo} and (c) Hybrid frequency estimation using the combination ω_{PLL} and ω_{FD}.

The frequency estimation with a combination of SRFPLL and arctangent derived frequency is shown in Figure 6.7(a). This technique is already explained for the three-phase converter's FRT application in Chapter-5. It is investigated for single-phase FRT in this chapter. Additionally, two other frequency estimators in combination with SRFPLL, namely, teager energy operator (*teo*) (refer Figure 6.7(b) and fixed-delay (*FD*) (refer Figure 6.7(c)) methods are presented in this chapter for the enhanced FRT of the single-phase power converter. The

proposed frequency estimators will be used to feed the PR current controller during the occurrence of grid faults having PAJs.

The details of the proposed three enhanced frequency-adaptive SOGI based grid synchronization techniques have been discussed in Chapter-4. However, their implementation in feeding the frequency-adaptive PR current controller of single-phase converter for the FRT purpose is not included in the scope of Chapter-4 and hence explored in this chapter. All the modified control structures shown in Figure 6.7(a), Figure 6.7(b), and Figure 6.7(c), use the proposed hybrid grid synchronization principle (discussed in Chapter-4) during their transition to and from the SRFPLL frequency estimation depending on the grid operating conditions.

The proposed hybrid frequency-adaptive PR current controller performance of the single-phase converter during FRT will be tested in the following section using simulation analysis. The performance will be compared with the conventional SOGIPLL estimated frequency-adaptive current controller in case of grid faults having both voltage sag and PAJs.

6.4 Simulation Results

The converter and the controller parameters used for the simulation analysis and comparison between the conventional and proposed techniques are shown in TABLE 6.1. The FRT response is investigated by considering a fault having 70% grid voltage sag. Initially, the frequency adaptability of the PR current controller is explored without and with the addition of PAJ during the grid fault. The response without PAJ is shown in Figure 6.8. The frequency independent PR current controller response is shown in Figure 6.8 (i), while the frequency-adaptive response with SRFPLL estimation is shown in Figure 6.8 (ii). There is not much difference observed between the two FRT responses during fault having no PAJ.

TABLE 6.1: SINGLE-PHASE CONVERTER AND CONTROLLER PARAMETERS

Parameters and Symbols	Values
Nominal Power (P_N)	610 W
DC voltage (V_{DC})	200 V
Grid voltage (Secondary side) (V_g)	120 V_{rms}
Nominal current (Primary side) (I_N)	6.5 A_{peak}
Grid Frequency (f_g)	50 Hz
Proportional gain of the voltage control (K_{pV})	8
Integral gain of the voltage control (K_{iV})	7000
Proportional gain of the current control (K_{pi})	16
Resonant gain of the current control (K_{ri})	7000
Settling time of the SRFPLL (t_{set})	120 ms
Gain of SOGI	1.414
Transition time for TPLL (t_{tr})	2 ms
Grid side filter inductance (L_{fg})	1.8 mH
Converter side filter inductance (L_f)	0.5 mH
Sampling frequency (f_{sam}) and Switching frequency (f_{sw})	10 kHz

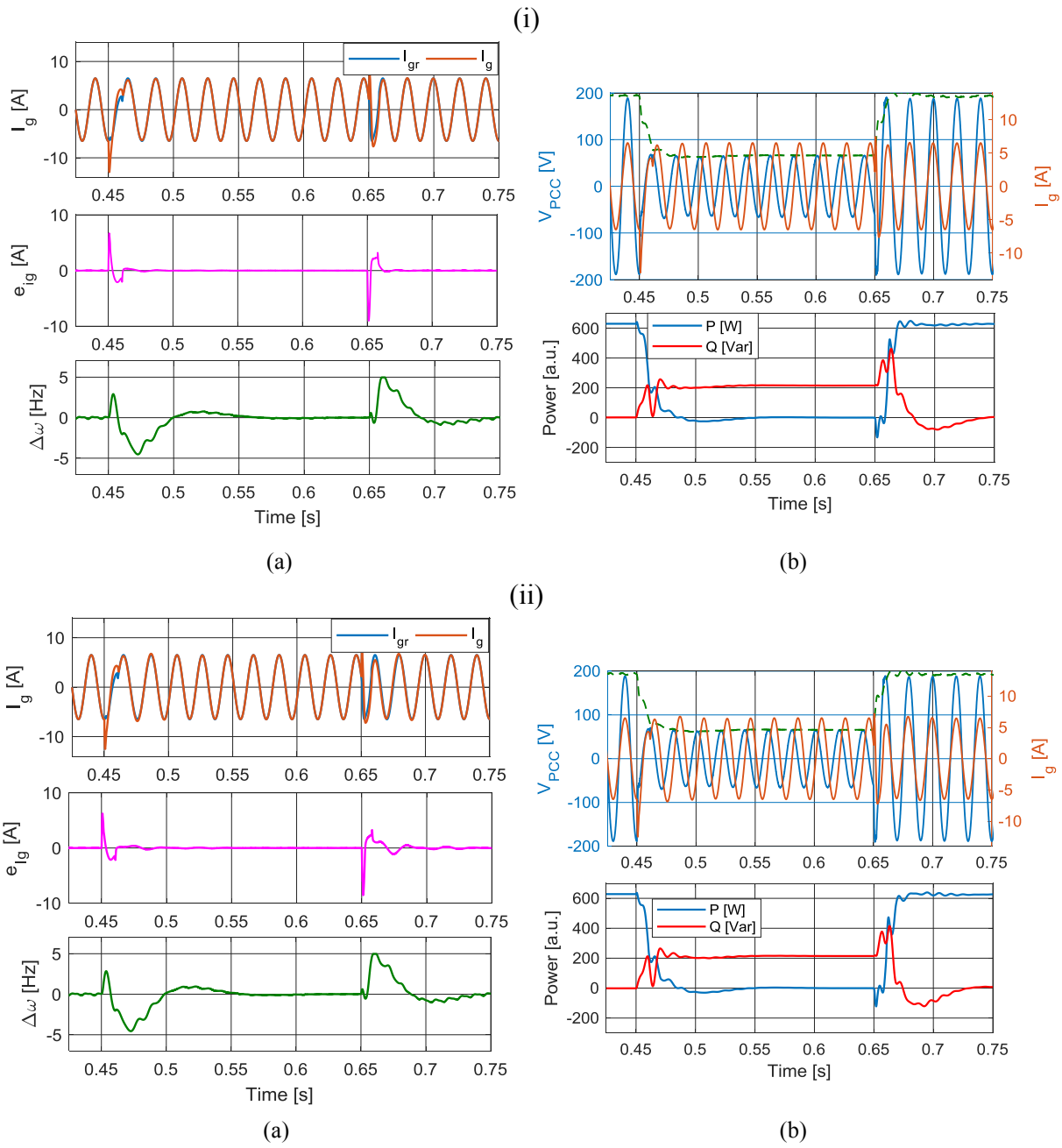


Figure 6.8 FRT response of single-phase grid-connected power converter during 70% sag in the grid voltage (V_g) with (i) frequency independent and (ii) frequency-adaptive (with SRFPLL estimation) PR current controller,: plot for (a) grid current (I_{gr} and I_g), error in grid current (e_{Ig}), error in SRFPLL estimated frequency ($e_{\Delta\omega}$), and plot for (b) voltage and current measured at PCC point (V_{PCC} and I_g), injected active (P) and reactive power (Q).

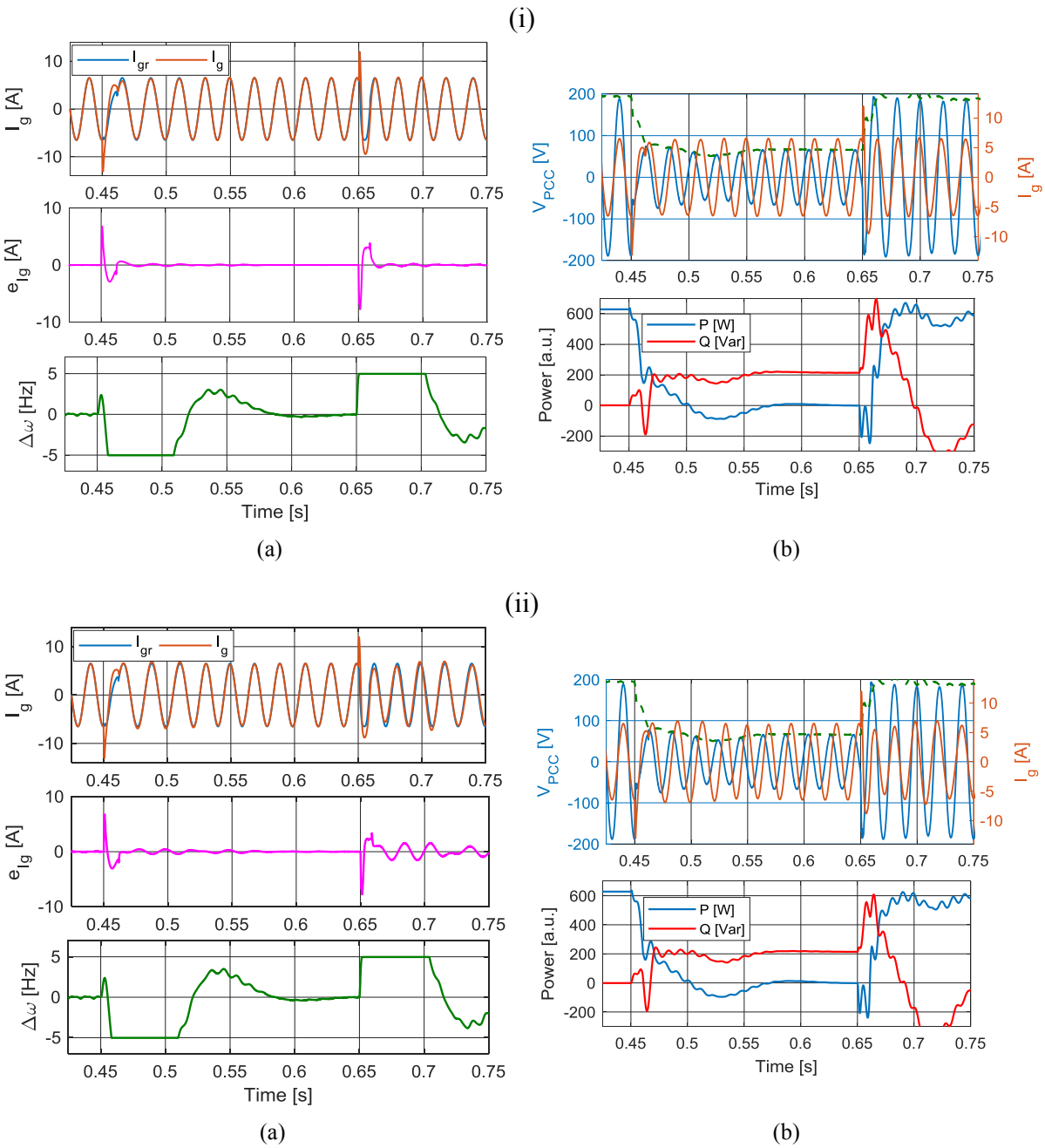


Figure 6.9 FRT response of single-phase grid-connected power converter during 70% sag and -45° PAJ in the grid voltage (V_g) with (i) frequency independent and (ii) frequency-adaptive (with SRFPLL estimation) PR current controller,: plot for (a) grid current (I_{gr} and I_g), error in grid current (e_{Ig}), error in SRFPLL estimated frequency ($e_{\Delta\omega}$), and plot for (b) plot for voltage and current measured at PCC point (V_{PCC} and I_g), injected active (P) and reactive power (Q).

The same test is carried out by adding -45° PAJ to the grid voltage having 70% sag. The responses without and with frequency-adaptive PR current controller are shown in Figure 6.9 (i) and Figure 6.9 (ii) respectively. As anticipated, with the PAJ the frequency estimation by

SRFPLL (in SOGIPLL) undergoes an abrupt oscillation during the fault inception and recovery. It also deteriorates the dynamics of the frequency-adaptive PR current controller (refer 6.9 (ii)). Consequently both the injected active and reactive powers seem to be highly impacted by the frequency-adaptive nature of the PR current controller.

Though such frequency-adaptive nature of the PR current controller improves the steady-state performance during off-nominal frequency variations, it is highly vulnerable to the notorious PAJ associated with the grid fault. Such poor FRT dynamics of the converter with SRFPLL estimated frequency-fed PR current controller is improved with the proposed enhanced frequency-adaptive PR current controller as shown below.

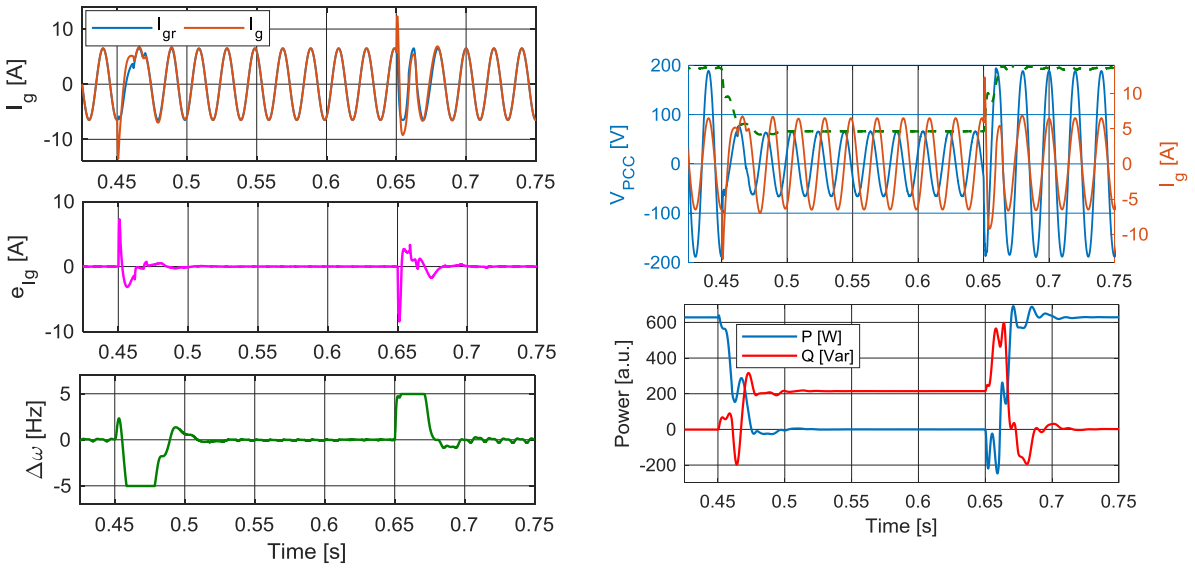


Figure 6.10 FRT response of single-phase grid-connected power converter during 70% sag and -45° PAJ in the grid voltage (V_g) with (i) frequency independent and (ii) frequency-adaptive (with arctangent derived frequency estimation during the fault inception and recovery) PR current controller,: plot for (a) grid current (I_{gr} and I_g), error in grid current (e_{Ig}), error in SRFPLL estimated frequency ($e_{\Delta\omega}$), and plot for (b) plot for voltage and current measured at PCC point (V_{PCC} and I_g), injected active (P) and reactive power (Q),

The adaptation of the proposed hybrid frequency estimator (under the hybrid grid synchronization principle) is shown in Figure 6.10. Here, the frequency estimation is

switched from SRFPLL to the arctangent derived frequency at the occurrence of PAJ. It can be observed that the proposed technique is able to provide a smooth FRT response by reducing oscillations in the frequency, grid current and power. The response time is observed to be around 60 ms which was around 120 ms for the conventional SRFPLL based technique.

Similarly, in the second proposition of enhanced frequency-adaptive PR current controller, the frequency to be fed at the occurrence and recovery of fault is estimated using the teager energy operator. The response is shown in Figure 6.11. The dynamic performance is observed to be improved as it gives a response time similar to that of the first proposition (using arctangent derived frequency) i.e., 60 ms. Unlike the conventional SRFPLL technique, it does not require any gain tuning for the frequency estimation. It also provides a phase-angle decoupled frequency estimation which makes it robust during the PAJ related grid faults.

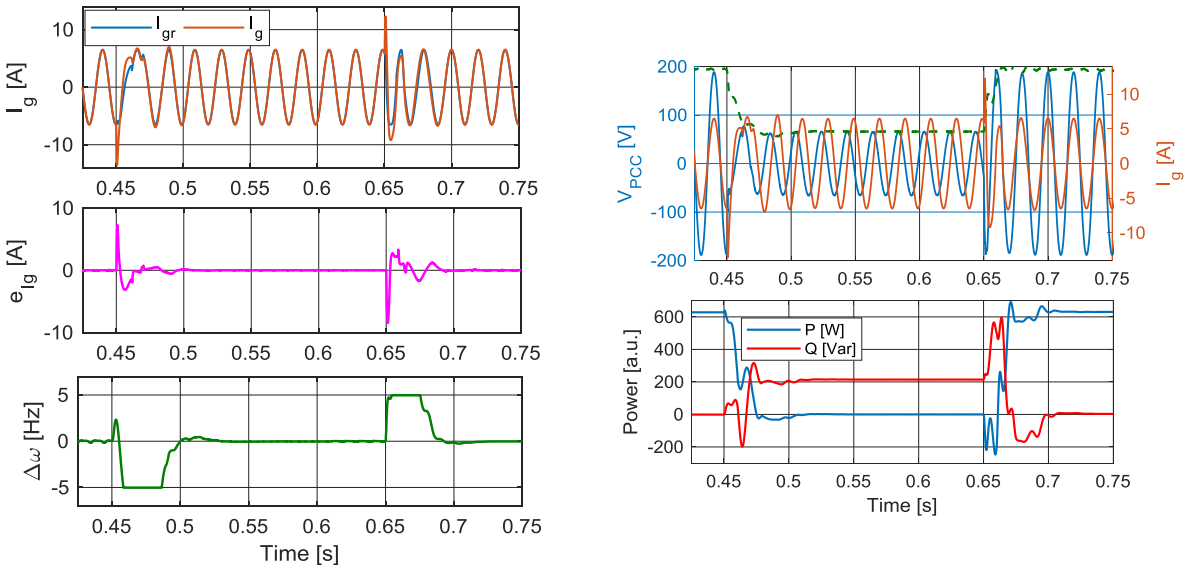


Figure 6.11 FRT response of single-phase grid-connected power converter during 70% sag and -45° PAJ in the grid voltage (V_g) with (i) frequency independent and (ii) frequency-adaptive (with teager energy operator based frequency estimation during the fault inception and recovery) PR current controller,: plot for (a) grid current (I_{gr} and I_g), error in grid current (e_{Ig}), error in SRFPLL estimated frequency ($e_{\Delta\omega}$), and plot for (b) plot for voltage and current measured at PCC point (V_{PCC} and I_g), injected active (P) and reactive power (Q).

The third proposition estimates and feeds the frequency to the PR current controller using the fixed-delay (FD) method during the grid fault having PAJ. Similar to propositions 1 and 2, it also avoids the PLL tuning issue and hence provides robust current controller dynamics and improves the FRT response of the converter. As compared to propositions 1 and 2 the overshoots observed in the active power is slightly higher during fault recovery i.e., 200 W which is around 50 W for the former cases. Apart from this, the response time is almost equal for all the three propositions and lesser than the conventional SRFPLL techniques.

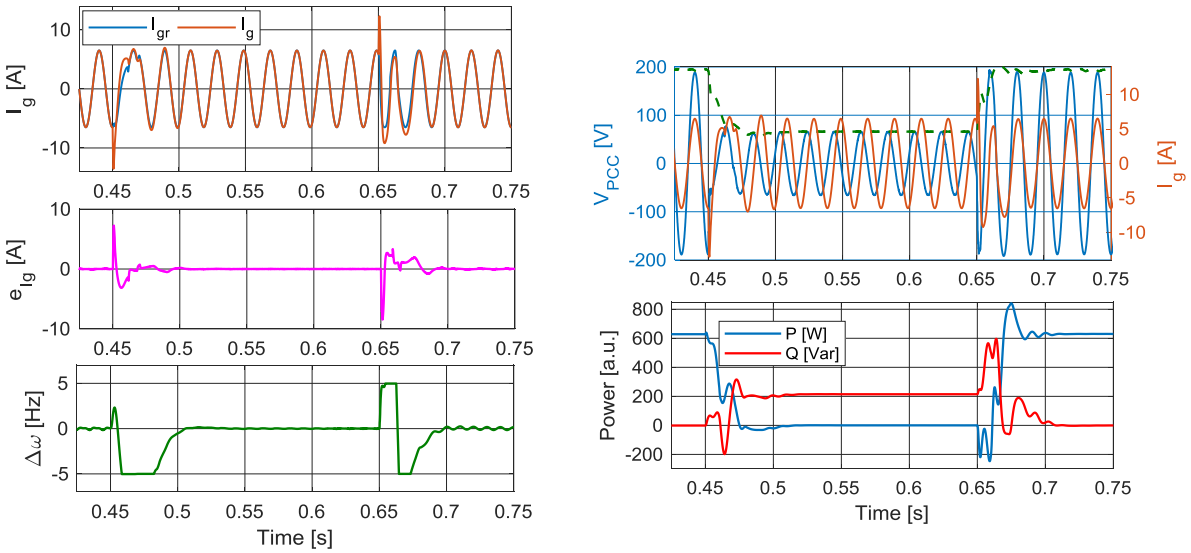


Figure 6.12 FRT response of single-phase grid-connected power converter during 70% sag and -45° PAJ in the grid voltage (V_g) with (i) frequency independent and (ii) frequency-adaptive (with fixed-delay based frequency estimation during the fault inception and recovery) PR current controller,: plot for (a) grid current (I_{gr} and I_g), error in grid current (e_{Ig}), error in SRFPLL estimated frequency ($e_{\Delta\omega}$), and plot for (b) plot for voltage and current measured at PCC point (V_{PCC} and I_g), injected active (P) and reactive power (Q).

A comparison among the frequency-adaptive PR current controller response time using the conventional and proposed hybrid grid synchronization schemes are provided in TABLE 6.2. The comparisons are made during the grid fault with PAJ.

TABLE 6.2 COMPARISON OF FREQUENCY-ADAPTIVE PR CURRENT CONTROLLER RESPONSE TIME DURING FAULT RIDE-THROUGH

Frequency adaptability of the PR controller	Response time
Fed by SOGIPLL (ω_{PLL})	120 ms
Fed by hybrid proposition-I (combination of ω_{PLL} and $\omega_{\alpha\beta}$)	60 ms
Fed by hybrid proposition-II (combination of ω_{PLL} and ω_{teo})	60 ms
Fed by hybrid proposition-III (combination of ω_{PLL} and ω_{FD})	60 ms

6.5 Chapter Summary

This chapter explores the fault ride-through (FRT) of grid-connected single-phase converter. A proportional and resonant (PR) controller is used to regulate the grid current during the FRT. In contrast to proportional and integral (PI) controllers, grid current control using PR controllers avoids any frame transformations. The need for frequency adaptability of the PR current controller is explained during off-nominal grid frequency variations. The frequency to the PR current controller is usually fed by the SRFPLL in SOGIPLL grid synchronization. However, it is shown in the chapter that such frequency feedback from SRFPLL makes the current controller vulnerable to grid faults having PAJs. The FRT of the power converter is highly affected in such cases. To avoid this issue, three enhanced frequency estimators are proposed to feed the PR current controller during the PAJ. They are: a) the arctangent derived frequency, b) teager energy operator estimated frequency, and c) fixed-delay based frequency estimation. All these frequency estimators are free from PLL tuning issues. These frequency estimators follow the proposed hybrid grid synchronization principle to replace the SRFPLL frequency estimation feedback for PR current controller during faults.

The dynamic performance of the proposed enhanced frequency-fed PR current controller during grid fault is investigated using simulation analysis. Their performance is compared with the conventional SOGIPLL grid synchronized power converter where the frequency estimated by SRFPLL is fed to PR current controller. It is revealed that as long as the grid fault involves only voltage sag, the frequency feedback from SRFPLL estimation can be an optimum choice to avoid any steady-state error. However, when PAJ is associated with the grid fault, the dynamics of the PR current controller can only be improved if the frequency estimation is replaced by the proposed techniques. A summary of the current controller performance during FRT with both the conventional and proposed grid synchronization when subjected to various grid faults is provided in TABLE 6.2. '✔' refers to the robust, '✔✔' refers to the robust and recommended, '✖' refers to the poor but can be used, and '✖✖' refers to the poor and not recommended.

TABLE 6.3: SUMMARY OF ADAPTIVE CURRENT CONTROLLER PERFORMANCE OF SINGLE-PHASE CONVERTER WITH THE HYBRID GRID SYNCHRONIZATION TECHNIQUE DURING FAULT RIDE-THROUGH.

	Grid Synchronization Technique				Current Controller for improved FRT	
Fault Type	SOGI + ω_{PLL}	SOGI + $\omega_{\alpha\beta}$	SOGI + ω_{teo}	SOGI + ω_{FD}	PI	*PR
Symmetrical (Voltage Sag)	**✔/✖	NC	NC	NC	NC	✔
Symmetrical (Voltage Sag + PAJ)	✖✖	✔	#✔✔	#✔✔	NC	✔

NC: Not Considered in this Study, **SOGI**: Second-order Generalized Integrator ω_{PLL}: Frequency estimation by PLL, $\omega_{\alpha\beta}$: Frequency estimation by derived arctangent phase-angle, ω_{teo} **:** Frequency estimation by teager energy operator, ω_{FD}: Frequency estimation by Fixed delay method **PI**: Proportional plus Integral, **PR**: Proportional plus Resonant.

*Only frequency-adaptive resonant (R) controller is discussed.

** ✔ for frequency independent PR and ✖ for frequency-adaptive PR controller

Requires only one input signal to estimate the grid frequency with faster dynamics.

Chapter 7

Conclusions and Future Work

This chapter presents an overview of the contributions and related research work that has been carried out in this thesis. The main contributions are addressed in two parts in the thesis. They are: Part I: "*Fault detection technique in grid-connected converters*" which corresponds to Chapter-2 and Part II: "*Improved fault ride-through of power converters using hybrid grid synchronization*" which corresponds to Chapter-3, Chapter-4, Chapter-5 and Chapter-6. The contributions based on the above two parts will be detailed chapter wise in a chronological manner in Section 7.1. To that end, based on the outcome derived from the contributions made in the thesis, future research scope will be detailed briefly in Section 7.2.

7.1 Conclusions

The chapter wise contributions and conclusions drawn in the thesis are as follows:

Chapter-2: It focuses on the fault detection techniques in grid-connected converter applications. It reviews the digital signal processing techniques used for fault detection which are classified as a) Frequency domain techniques, b) Time-frequency domain techniques and, c) Hybrid techniques. In line with the hybrid techniques, it proposes the combination of two digital signal processing techniques: i) Hilbert-Huang Transform (HHT) and, ii) Teager Energy Operator to detect several grid faults. The combined technique is named as "Teager-Huang" technique. With the proposed technique the teager energy of the first intrinsic mode function

(IMF-1) is calculated for fault detection. The HHT mainly provides the instantaneous magnitude and frequency of the IMF-1 which are used for the calculation of the teager energy. The proposed Teager-Huang based fault detection is used to characterize the severity of the grid fault in terms of sag depth and occurrence of different phase-angle jumps (PAJs). Additionally, the seven types of power system faults which include unbalances in both phase voltage magnitude and PAJs are considered to provide a comparative fault energy calculation.

Chapter-3: It explores the loss of grid synchronization (LOS) issue during the fault ride-through (FRT) of grid-connected power converters. The LOS is explained as the result of either large-signal instability or small-signal instability. It is shown that large-signal instability mainly occurs due to the violation of steady-state network conditions i.e., as a result of high amount of reactive current injection during the FRT. In contrast, the LOS due to the small-signal instability is attributed to the inaccurate gain parameter tuning of the synchronous reference frame phase-locked loop (SRFPLL). Accordingly, the damping factor offered by the SRFPLL during the grid faults having higher phase-angle jump (PAJ) is insufficient to avoid LOS. Several test cases are simulated to illustrate the occurrences of LOS during both symmetrical and asymmetrical faults without and with PAJs. The instability phenomena as a result of both large-signal and small-signal instability are demonstrated separately. The understanding gained from this chapter motivates to propose adaptive/hybrid grid synchronization techniques for power converters.

Chapter-4: It begins with a brief summary of the adaptive grid synchronization techniques to improve the FRT of power converters during grid faults proposed in the growing body of literatures. The adaptability is referred to the modification done to improve the gain tuning of the conventional synchronous reference frame phase-locked loop (SRFPLL) grid

synchronization. The control implementations of these techniques are detailed along with their limitations.

In addition to this, as a main contribution of this chapter, a hybrid grid synchronization transition technique is proposed for the improved FRT of power converters during the grid faults having PAJs. Hybrid grid synchronization consists of a hybrid phase-angle estimator for current control of the power converters. The hybrid phase-angle estimator uses the arctangent based phase-angle estimation for grid synchronisation when the grid voltage faces a PAJ during either symmetrical or asymmetrical faults. The peculiarity of the proposed hybrid estimator is that it provides faster estimation by avoiding the design trade-off of SRFPLL loop gain. On the recovery of the fault, it switches back to the SRFPLL estimations to get advantageous features such as accurate frequency tracking and harmonic rejection capability. On the other hand, during asymmetrical grid faults, to enhance the frequency adaptability of the positive sequence extractor, the proposed hybrid grid synchronization transition includes a hybrid frequency estimator. The frequency adaptability is enhanced by replacing SRFPLL frequency estimation with the arctangent derived frequency during the PAJ associated grid faults. The positive sequence extractor used in this thesis is the dual second-order generalized integrator (DSOGI). Both the hybrid frequency and phase-angle estimators are controlled by a common phase-angle error based bump-less transition framework.

In contrast to three-phase hybrid grid synchronization, this chapter also investigates the synchronization issue with single-phase systems where the state-of-the-art technique considered is the second-order generalized integrator phase-locked loop (SOGIPLL). Similar to the DSOGIPLL discussed for three-phase systems, the frequency adaptability of the SOGI is improvised by proposing three PLL free frequency estimators. They are: a) arctangent derived frequency, b) teager energy operator estimated frequency, and c) frequency estimation using fixed-delay technique. All these estimators are proposed to follow the same hybrid grid

synchronization transition principle as discussed for three-phase systems during the grid faults having PAJs. The Chapter-4 ends with a benchmark study of the proposed adaptive and hybrid grid synchronization techniques corresponding to both three-phase and single-phase systems. The benchmarking includes the comparisons with the existing techniques during various grid fault conditions.

Chapter-5: It is dealt with the model development and dynamic performance evaluation of the three-phase grid-connected power converters during the FRT. Initially, the detailed model of the grid-connected converter along with its control functionally at various layers is overviewed. Further, the reduced-order model used for the FRT study under necessary assumptions is explained. This chapter implements the hybrid grid synchronization principle explained in Chapter-4. It explores the FRT of three-phase converters during both symmetrical and asymmetrical grid faults having PAJs. The adaptability of the proposed hybrid grid synchronization along with the robustness in the current controller response during the FRT is investigated. Several test case scenarios like non-severe symmetrical fault with PAJ, severe symmetrical fault with PAJ (that leads to LOS), and asymmetrical faults with PAJs are considered. During the asymmetrical FRT discussions, only the positive sequence current injection during the fault duration is considered in the scope of the chapter.

In case of symmetrical FRT, the inner current controller is implemented in the synchronous reference frame (*dq*-frame) using proportional plus integral controller (PI). On the other hand, during the asymmetrical FRT, two types of current controllers are evaluated with the proposed hybrid grid synchronization. They include: a) proportional plus integral plus second resonant controller (PIR_2) and b) proportional plus resonant controller (PR). The performance enhancement of the proposed adaptive current controller over the conventional techniques during the FRT is presented using both simulation analyses and experimental validations.

Chapter-6: It investigates the FRT of single-phase grid-connected converter synchronised with the proposed adaptive and hybrid grid synchronization technique. The current controller is modelled in the stationary reference frame using proportional plus resonant controller (PR). The frequency adaptability of the PR current controller during the single-phase grid voltage faults having PAJ is enhanced by replacing the SRFPLL frequency estimation with the proposed frequency estimators explained in Chapter-4. The frequency switch that is fed to the PR controller is followed using the hybrid grid synchronization transition principle applied during the FRT of the three-phase power converters.

The dynamics of the proposed enhanced frequency-adaptive PR current controller of the single-phase converter during the FRT is compared with the conventional SOGIPLL grid synchronized power converter. It is revealed that as long as the grid fault involves only voltage sag, the frequency feedback from SRFPLL estimation can be an optimum choice to avoid any steady-state error. However, when PAJ is associated with the grid fault, the dynamics of the PR current controller can be improved by replacing the frequency estimation with the proposed techniques.

7.2 Future Work

The future work of the current research is aimed based on the following research ideas:

i) Fault detection in large inter-connected system

The proposed fault detection technique in Chapter-2 is able to detect several grid faults with and without PAJs in addition to voltage sags. However, the system considered for study includes one converter connected to grid. In real time, the power electronic based power system represents a large inter-connected system. It consists of several renewable energy sources, different feeder impedance, various critical and non critical loads along with complex grid structure. In future, the proposed fault detection can be further explored in such a large interconnected system in which the considered data for fault detraction will be a mix of several grid events. Additionally, suitable fault classifier can be embedded to the proposed fault detection technique to distinguish between the grid fault event and normal events.

ii) FRT study in multi-converter systems

The research work conducted regarding the FRT of the power converter in the scope of the thesis considers the single grid-connected inverter system. This is analogous to single-machine infinite bus system in regards to classical power system. The proposed concept can be extended to grid-connected multi-converter system considering two possible aspects as given below.

a) Heterogeneous grid synchronization

One of the possibilities that can be explored for multi-converter systems is the heterogeneous grid synchronization technique. For instance, one of the converters is synchronized with the conventional second-order SRFPLL or the existing adaptive SRFPLL technique while the other converter deploys the proposed hybrid grid synchronization principle. In such a scenario, the interaction between the grid synchronization techniques and dynamics of the current controller

during the FRT of each converter can be investigated. Additionally, in case of a mesh connected system, such heterogeneous types of synchronization techniques of the converter may affect the inter-area oscillations. This can be further researched as well.

b) Heterogeneous converter controller

In contrast to different grid synchronization unit, the current controller implementation of the power converter can be heterogeneous in nature in multi-converter systems. Thus, the FRT study of the multi-converter system using the proposed hybrid grid synchronization transition with different current controllers can provide a better picture of the efficacy of the proposed technique. Moreover, the optimal location of the converter having the proposed adaptive controller in such multi-converter systems can be investigated.

iii) Comparison with the FRT of Grid-forming converter

During the investigation of FRT of power converter in this thesis (Chapter-3, Chapter-4, Chapter-5 and Chapter-6), the grid-connected converter is considered as grid-following type. It requires a dedicated synchronization unit for control purposes. On the contrary, the grid-connected converters implement the grid-forming mode of control features based on self-synchronization principle. Compared to grid-following mode, grid-forming converters provide better dynamics, frequency and voltage regulation especially when the grid is weak. However, the research on the FRT of these grid-forming converters is in the primitive stage. Thus, it will be interesting to compare the FRT of grid-following of power converter that utilizes the proposed hybrid grid synchronization with that of the grid-forming power converters.

iv) FRT study considering outer-loop control

This thesis considers the inner current control design during the FRT of grid-connected power converters. The DC-link voltage is assumed to be constant in the consideration of reduced-order model. In the future research, the outer-loop control that includes voltage control and/or power controller can be implemented to study the impact of the hybrid grid synchronization on the FRT of the converters. To this end, the influence of source side intermittency (variations in wind power or PV power generation) on the power converters during the FRT can be investigated.

v) Impact of switching of reactive power compensation device on the hybrid grid synchronization

The impact of switching instance of various reactive power compensation device; for instance, the switching ON/OFF of capacitors at the PCC point on the hybrid grid synchronization transition scheme will be researched further.

Appendix

A. Frame Transformations

The measured three-phase voltage and current signals at the point of common coupling is frame transferred from *abc*-to-*αβ* using the Clarke transform as given by (A.1),

i) Clarke Transform (*abc-αβ*)

$$\left[V_{\alpha\beta}/\, I_{\alpha\beta}\right]^T = \begin{bmatrix} V_\alpha/I_\alpha \\ V_\beta/I_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V/I\cos(\omega t+\theta_a) \\ V/I\cos(\omega t-\frac{2\pi}{3}+\theta_b) \\ V/I\cos(\omega t+\frac{2\pi}{3}+\theta_c) \end{bmatrix} \quad \text{(A.1)}$$

$$= \begin{bmatrix} V/I\cos(\omega t+\theta_a) \\ V/I\sin(\omega t+\theta_a) \end{bmatrix}$$

where $V_{\alpha\beta}$ and $I_{\alpha\beta}$ are the *αβ*-components of three-phase signals. V and I are the peak value of the measured signal of each phase.

ii) Park Transform (*αβ-dq*)

The *αβ*-components of three-phase signals (both voltage and current) are frame transferred from *αβ*-to-*dq* for grid synchronization and current control purpose in the synchronous reference frame as given by (A.2).

$$\left[V_{dq}/\, I_{dq}\right]^T = \begin{bmatrix} V_d/I_d \\ V_q/I_q \end{bmatrix}$$

$$= \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin(\theta-2\pi/3) & -\sin\left(\theta+\frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} V/I\cos(\omega t+\theta_a) \\ V/I\cos(\omega t-\frac{2\pi}{3}+\theta_b) \\ V/I\cos(\omega t+\frac{2\pi}{3}+\theta_c) \end{bmatrix} \quad \text{(A.2)}$$

Where V_{dq} and I_{dq} are the *dq*-components of voltage and currents. They are the DC values. θ is the frame transformation angle (obtained from the synchronization unit).

iii) Active (P) and Reactive (Q) Power Calculations

The active ($P_{3\emptyset}$) and reactive power ($Q_{3\emptyset}$) measured during both normal and grid fault conditions for three-phase system both in *abc*-frame and *dq*-frame is given by (A.3a) and (A.3b) respectively.

$$P_{3\emptyset} = \Re[\mathbf{V}_{abc} \times \mathbf{I}_{abc}] = \frac{3}{2}\left[(V_d \times I_d) + (V_q \times I_q)\right] \tag{A.3a}$$

$$Q_{3\emptyset} = \Im[\mathbf{V}_{abc} \times \mathbf{I}_{abc}] = \frac{3}{2}\left[(V_d \times I_q) - (V_q \times I_d)\right] \tag{A.3b}$$

Similarly, for single-phase systems the powers ($P_{1\emptyset}$ and $Q_{1\emptyset}$) are calculated as per (A.4a) and (A.4b),

$$P_{1\emptyset} = \Re[\mathbf{V}_a \times \mathbf{I}_a] = \frac{1}{2}\left[(V_d \times I_d) + (V_q \times I_q)\right] \tag{A.4a}$$

$$Q_{1\emptyset} = \Im[\mathbf{V}_a \times \mathbf{I}_a] = \frac{1}{2}\left[(V_d \times I_q) - (V_q \times I_d)\right] \tag{A.4b}$$

iv) Transfer Functions for Second-order Generalized Integrator (SOGI)

During three-phase grid voltage unbalance or single-phase systems, the second-order generalized integrator (SOGI) is used as pre-filter in this thesis. It acts as a band pass filter (BPF). The transfer function of the *αβ*-components in relation to the input voltage signal are given by (A.5) and (A.6) respectively,

$$G_\alpha(s) = \frac{V_\alpha(s)}{V_a(s)} = \frac{K_{SOGI}\omega_{est}s}{s^2 + K_{SOGI}\omega_{est}s + {\omega_{est}}^2} \tag{A.5}$$

$$G_\beta(s) = \frac{V_\beta(s)}{V_a(s)} = \frac{K_{SOGI}{\omega_{est}}^2}{s^2 + K_{SOGI}\omega_{est}s + {\omega_{est}}^2} \tag{A.6}$$

v) Sequence Component Extractions during Unbalance Grid Voltage

During three-phase asymmetrical faults, the measured voltage signal gets unbalanced. It contains positive ($V_{abc}{}^{+}/\ I_{abc}{}^{+}$), negative ($V_{abc}{}^{-}/\ I_{abc}{}^{-}$) and zero sequence ($V_{abc}{}^{0}/\ I_{abc}{}^{0}$) components. The zero sequence components are not considered in the secondary side of the transformer which is considered as star and not grounded. The extraction of positive and negative sequence components extraction in the *abc*-frame is given by (A.7) and (A.8) respectively. The value of 'a' is 1∠-120°.

$$[V_{abc}{}^{+}/\ I_{abc}{}^{+}]^T = \begin{bmatrix} V_a{}^{+}/I_a{}^{+} \\ V_b{}^{+}/I_b{}^{+} \\ V_c{}^{+}/I_c{}^{+} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} V_a/I_a \\ V_b/I_b \\ V_c/I_c \end{bmatrix} \tag{A.7}$$

$$[V_{abc}{}^{-}/\ I_{abc}{}^{-}]^T = \begin{bmatrix} V_a{}^{-}/I_a{}^{-} \\ V_b{}^{-}/I_b{}^{-} \\ V_c{}^{-}/I_c{}^{-} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix}\begin{bmatrix} V_a/I_a \\ V_b/I_b \\ V_c/I_c \end{bmatrix} \tag{A.8}$$

The sequence component extraction can also be done in the *αβ*-frame which is followed in the thesis as given by (A.9) and (A.10) respectively,

$$\left[V_{\alpha\beta}{}^{+}/\ I_{\alpha\beta}{}^{+}\right]^T = \begin{bmatrix} V_\alpha{}^{+}/I_\alpha{}^{+} \\ V_\beta{}^{+}/I_\beta{}^{+} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix}\left[V_{\alpha\beta}/I_{\alpha\beta}\right]^T \tag{A.9}$$

$$\left[V_{\alpha\beta}{}^{-}/\ I_{\alpha\beta}{}^{-}\right]^T = \begin{bmatrix} V_\alpha{}^{-}/I_\alpha{}^{-} \\ V_\beta{}^{-}/I_\beta{}^{-} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix}\left[V_{\alpha\beta}/I_{\alpha\beta}\right]^T \tag{A.10}$$

The value of 'q' is $e^{-j\frac{\pi}{2}}$.

B. Simulation Model

The simulation model used for the study in this thesis is built using MATLAB®/SIMULINK and PLECS-blockset. The schematic is shown in Figure A.1. The converter model along with the grid model is built using PLECS-blockset in the continuous domain. The measured signals (voltage and current) are discretised. The controllers (grid synchronization and current controller) are implanted in the discrete domain using the discretised signals.

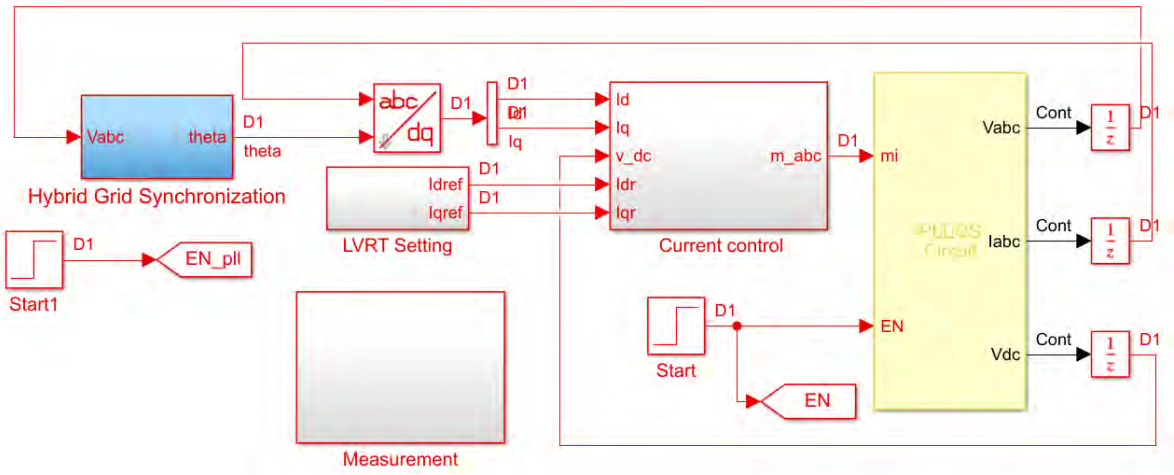


Figure A.1 Simulation model interfacing the continuous domain power converter model (using PLECS) and discrete domain controller (using MATLAB/SIMULINK).

The model developed using PLECS-blockset is expanded and shown in Figure A.2.

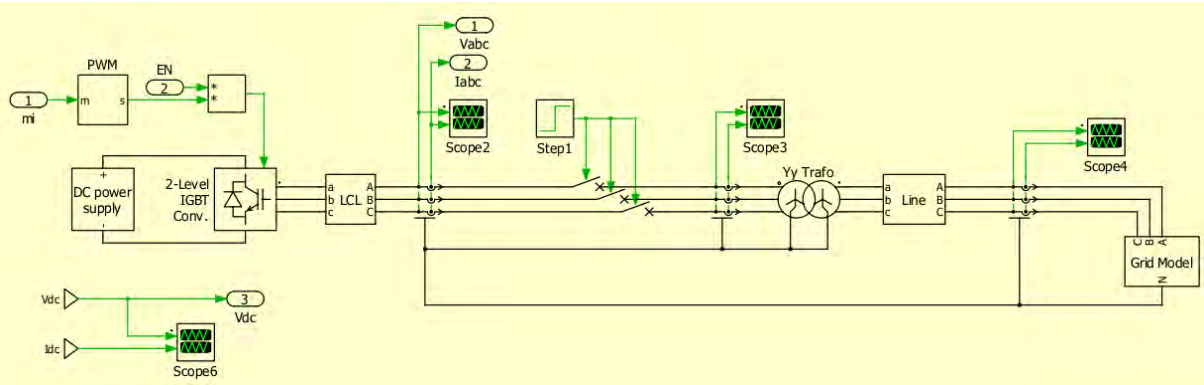


Figure A.2 Detailed simulation model for the continuous domain power converter (using PLECS).

The detailed implementation of the proposed hybrid grid synchronization transition scheme is shown in Figure A.3.

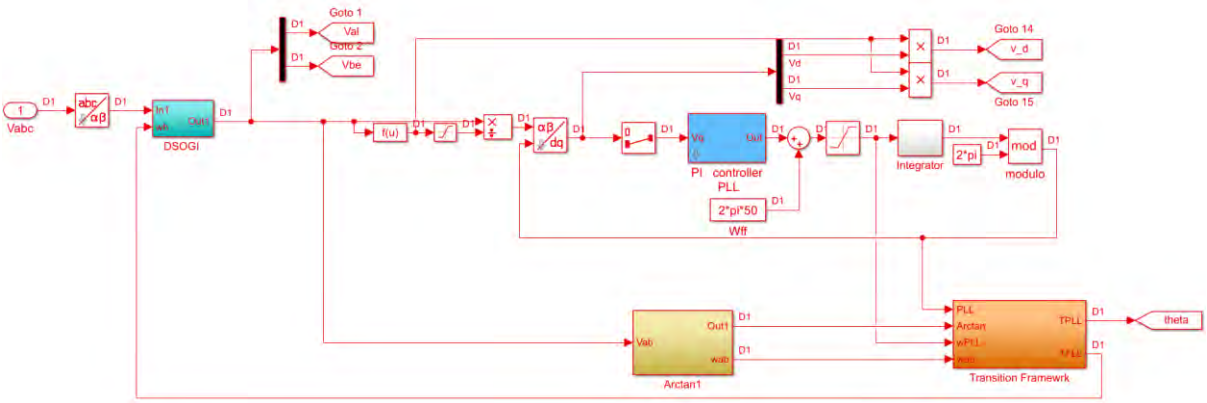


Figure A.3 Detailed simulation model for the discrete domain controller (using MATLAB/SIMULINK).

The current controller implementation in the synchronous reference frame is shown in Figure A.4. The proposed technique does not use voltage feedforward compensation. Hence it is shown in the dotted lines in the figure.

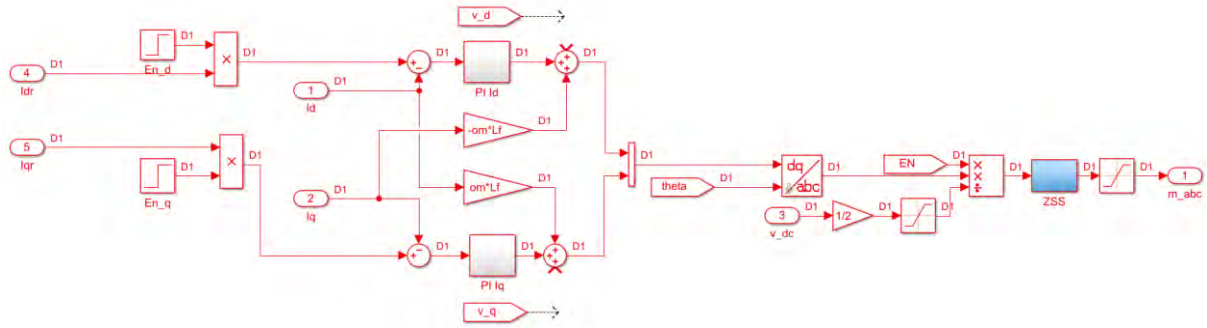


Figure A.4 Detailed simulation model for the discrete current controller (using MATLAB/SIMULINK) with and without voltage feedforward compensation.

C. Experimental Set Up

The performance of the current controller during fault ride-through using the proposed hybrid grid synchronization technique is compared with the SRFPLL technique using laboratory experiments. The schematic of the setup used is shown in Figure A.5.

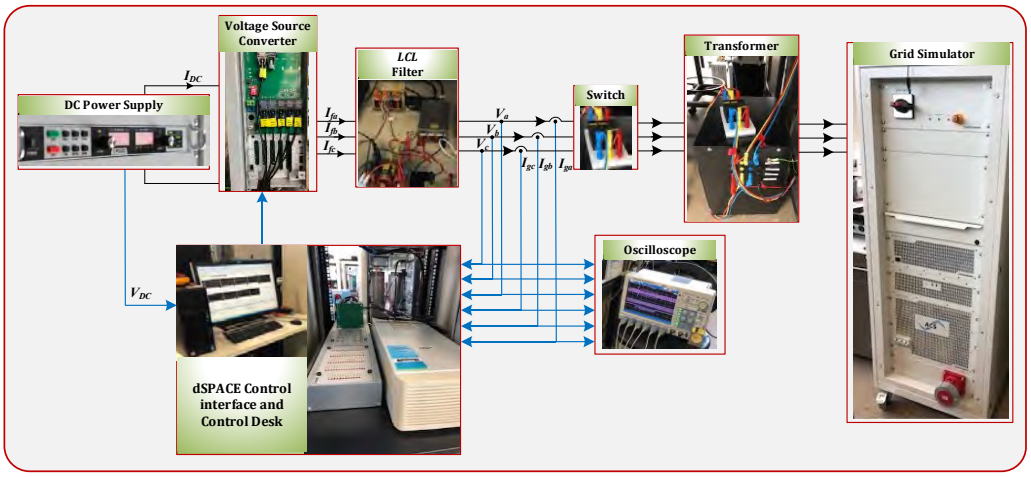


Figure A.5 Detailed hardware component connections to replicate the grid-connected power converter model.

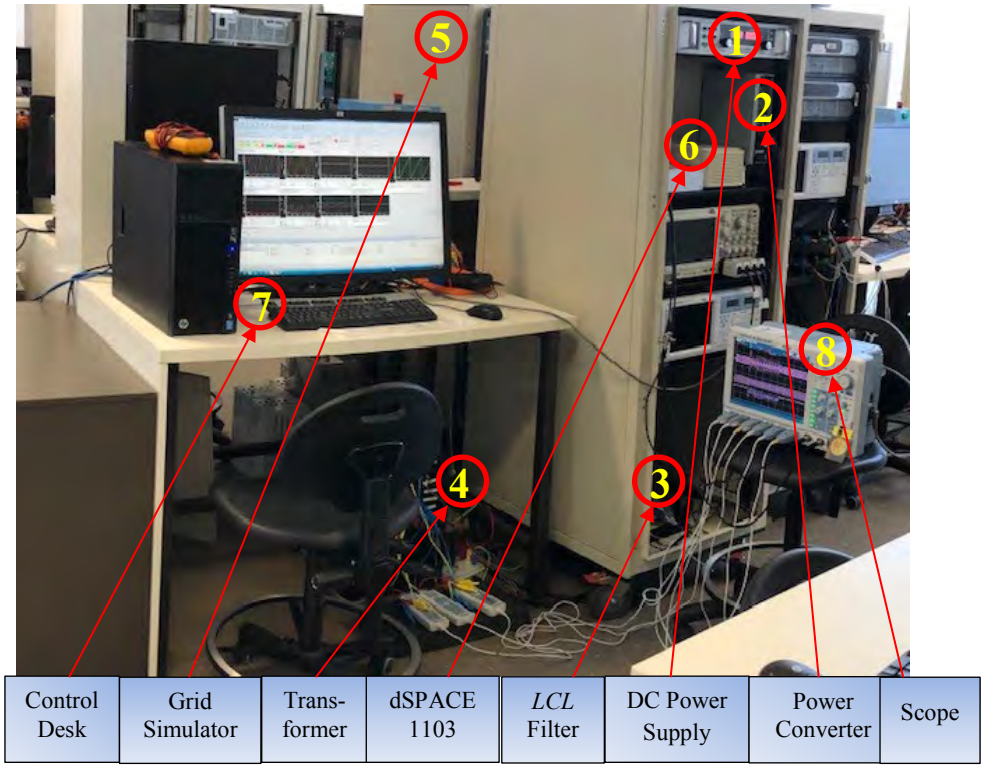


Figure A.6 Testbed used for the experimental validation in the power electronics laboratory of Tyree Energy Technology Building (TETB).

The grid voltage sag (60%) and PAJ (±45°) are programmed in real time using a programmable ac power supply (Regatron TC.ACS 4-quadrant grid simulator). The software model for the current controller in the SRF is interfaced with the Danfoss three-phase converter of 2.2 kW rating with *LCL* filter using a dSPACE1103 (DS1103) control board and a personal computer (PC). The arrangements for the experimental validations in the laboratory (power electronics lab in Tyree Energy Technology Building (TETB) at UNSW) are shown in Figure A.6.

Bibliography

[1] Adam Brown, et al: Renewable Energy: Markets and Prospects by Technology, International Energy Agency Information Paper, 2011.

[2] S. R. Bull, "Renewable energy today and tomorrow," *Proc. IEEE*, vol. 89, no. 8, pp. 1216–1226, Aug. 2001.

[3] B. Kroposki, B. Johnson, Y. Zhang, V. Gevorgian, P. Denholm, B.-M. Hodge, B. Hannegan, "Achieving a 100% renewable grid: operating electric power systems with extremely high levels of variable renewable energy", *IEEE Power Energy Mag*. 15 (2017) 61–73.

[4] B. Wu, Y. Lang, N. Zargari, and S. Kouro, Power Conversion and Control of Wind Energy Systems, 1st ed. Wiley, 2011, ISBN: 978-0-470-59365-3.

[5] https://www.ren21.net/wp-content/uploads/2019/05/gsr_2020_full_report_en.pdf

[6] Byrne J, Kurdgelashvili L, Mathai MV, Kumar A, Yu J, Zhang X, Tian J, Rickerson W. World solar energy review: technology, markets and policies. (May). Center for Energy and Environmental Policy, University of Delaware; 2010.

[7] Brankera K, Pathaka MJM, Pearcea JM. "A review of solar photovoltaic levelized cost of electricity", *Renewable Sustainable Energy Rev* 2011; 15: 4470–82.

[8] Islam MR , Mekhilef S, Saidur R. Progress and recent trends of wind energy technology. Renewable Sustainable Energy Rev 2013; 21:456–68.

[9] G. R. Energy. (2019) Haliade-x offshore wind turbine platform. [Online]. Available: https://www.ge.com/renewable energy/wind-energy/offshore-wind/haliade-x-offshore-turbine.

[10] Simon R. Sinsel, Rhea L. Riemke, Volker H. Hoffmann, Challenges and solution technologies for the integration of variable renewable energy sources—a review, *Renewable Energy*, Volume 145, 2020, Pages 2271-2285, ISSN 0960-1481.

[11] T. C. Green and M. Prodanovic, "Control of inverter-based micro-grids," *Electr. Power Syst. Res. Distrib. Generation*, vol. 77, no. 9, pp. 1204–1213, 2007.

[12] A. K. Sahoo, K. Mahmud, M. Crittenden, J. Ravishankar, S. Padmanaban and F. Blaabjerg, "Communication-less Primary and Secondary Control in Inverter-Interfaced AC Microgrid: An Overview," *IEEE Jour. Emerg. and Select. Topics .Pow. Electron.* [In-press].

[13] F. Katiraei and M. R. Iravani, "Power management strategies for a microgrid with multiple distributed generation units," *IEEE Trans. Power Syst.*, vol. 21, no. 4, pp. 1821–1831, Nov. 2006.

[14] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[15] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of power converters in AC microgrids," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.

[16] M. C. Chandorkar, D. M. Divan, and R. Adapa, "Control of parallel connected inverters in standalone AC supply systems," *IEEE Trans. Ind. Appl.*, vol. 29, no. 1, pp. 136–143, Jan./Feb. 1993.

[17] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 654–664, Mar. 2009.

[18] F. Milano, F. Dörfler, G. Hug, D. J. Hill, and G. Verbi´c, "Foundations and challenges of low-inertia systems," in *Proc. Power Syst. Comput. Conf*. (PSCC), Dublin, Ireland, Jun. 2018, pp. 1–25.

[19] N. Pogaku, M. Prodanovic, and T. C. Green, "Modeling, analysis and testing of autonomous operation of an inverter-based microgrid," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 613–625, Mar. 2007.

[20] L. Zhang, L. Harnefors, and H.-P. Nee, "Power-synchronization control of grid-connected voltage-source converters," *IEEE Trans. Power Syst.*, vol. 25, no. 2, pp. 809–820, May 2010.

[21] F. Baradarani, M. R. D. Zadeh, and M. A. Zamani, "A phase-angle estimation method for synchronization of grid-connected power-electronic converters," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 827–835, Apr. 2015.

[22] B. P. McGrath, D. G. Holmes and J. J. H. Galloway, "Power converter line synchronization using a discrete Fourier transform (DFT) based on a variable sample rate," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 877–884, Jul. 2005.

[23] C. J. Ramos, A. P. Martins, and A. S. Carvalho, "Frequency and phase-angle estimation using ordinary least squares," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5677–5688, Sep. 2015.

[24] H. Song and K. Nam, "Instantaneous phase-angle estimation algorithm under unbalanced voltage-sag conditions," *Proc. Inst. Elect. Eng.*, vol. 147, pp. 409–415, Nov. 2000.

[25] K. J. Lee, J. P. Lee, D. Shin, D. W. Yoo, and H. J. Kim, "A novel grid synchronization PLL method based on adaptive low-pass notch filter for grid-connected PCS," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 292–301, Jan. 2014.

[26] D. Shin, K. J. Lee, J. P. Lee, D. W. Yoo, and H. J. Kim, "Implementation of fault ride-through techniques of grid-connected inverter for distributed energy resources with adaptive low-pass notch PLL," *IEEE Trans. Power Electron*., vol. 30, no. 5, pp. 2859–2871, May 2015.

[27] A. Bagheri, M. Mardaneh, A. Rajaei, A. Rahideh, "Detection of grid voltage fundamental and harmonic components using Kalman filter and generalized averaging method," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1064–1073, Feb. 2016.

[28] Y. F. Wang and Y. W. Li, "A grid fundamental and harmonic component detection method for single-phase systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2204–2213, Jul. 2013.

[29] E. Robles, J. Pou, S. Recio, J. Zaragoza, J. Martin, and P. Ibaez, "Frequency adaptive stationary reference frame grid voltage sequence detector for distributed generation systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4275–4287, Sep. 2011.

[30] S. Chung, "A phase tracking system for three-phase utility interface inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 431–438, May 2000.

[31] M. E. Meral, "Improved phase-locked loop for robust and fast tracking of three phases under unbalanced electric grid conditions," *IET Gener. Transm. Distrib.*, vol. 6, no. 2, pp. 152–160, Feb. 2012.

[32] M. Mirhosseini, J. Pou, V. G. Agelidis, E. Robles, and S. Ceballos, "A three-phase frequency-adaptive phase-locked loop for independent single-phase operation," *IEEE Trans. Power. Electron.*, vol. 29, no. 12, pp. 6255–6259, Dec. 2014.

[33] F. D. Freijedo, A. G. Yepes, O. Lopez, P. Fernandez-Comesana, and J. Doval-Gandoy, "An optimized implementation of phase locked loops for grid applications," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 9, pp. 3110–3119, Sep. 2011.

[34] A. Luna et al., "Grid voltage synchronization for distributed generation systems under grid fault conditions," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3414–3425, Jul./Aug. 2015.

[35] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194–1204, Apr. 2011.

[36] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero, and J. Doval-Gandoy, "An efficient implementation of generalized delayed signal cancellation PLL," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1085–1094, Feb. 2016.

[37] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multi-resonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.

[38] M. Karimi-Ghartemani and M. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *IEEE Trans. Power. Sys*, vol. 19, no. 3, pp. 1263–1270, Aug. 2004.

[39] L. Hadjidemetriou, F. Blaabjerg, and E. Kyriakides, "An adaptive tuning mechanism for phase-locked loop algorithms for faster time performance of interconnected renewable energy sources," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1792–1804, Apr. 2015.

[40] Ö. Göksu, R. Teodorescu, C. L. Bak, F. Iov, and P. C. Kjær, "Instability of wind turbine converters during current injection to low voltage grid faults and PLL frequency based stability solution," *IEEE Trans. Power Syst.*, vol. 29, no. 4, pp. 1683–1691, Jul. 2014.

[41] D. Dong, B. Wen, D. Boroyevich, and P. Mattavelli, "Analysis of phaselocked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 310–321, Jan. 2015.

[42] S. Ma, H. Geng, L. Liu, G. Yang, and B. C. Pal, "Grid-synchronization stability improvement of large scale wind farm during severe grid fault," *IEEE Trans. Power Syst.*, vol. 33, no. 1, pp. 216–226, Jan. 2018.

[43] H. Geng, L. Liu, and R. Li, "Synchronization and reactive current support of PMSG based wind farm during severe grid," *IEEE Trans. Sustain. Energy*, vol. 9, no. 4, pp. 1596–1604, Oct. 2018.

[44] S. Ma, H. Geng, G. Yang, and B. Liu, "Experimental validation of adaptive current injecting method for grid-synchronization improvement of grid tied REGS during short-circuit fault," *in Proc. Int. Power Electron. Conf.*, 2018, pp. 542–546.

[45] X. He, H. Geng, and S. Ma, "Transient stability analysis of grid-tied converters considering PLL's nonlinearity," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 40–49, Mar. 2019.

[46] H. Wu and X. Wang, "Design-oriented transient stability analysis of grid-connected converters with power synchronization control," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6473–6482, Aug. 2019.

[47] H. Wu and X. Wang, "Transient stability impact of the phase-locked loop on grid-connected voltage source converters," *in Proc. Int. Power Electron. Conf.*, 2018, pp. 2673–2680.

[48] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "Systematic approach for transient stability evaluation of grid-tied converters during power system faults," in *Proc. IEEE ECCE*, pp. 5191–5198, Sep. 2019.

[49] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "An overview of assessment methods for synchronization stability of grid-connected converters under severe symmetrical grid faults," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9655–9670, Oct. 2019.

[50] Z. Shuai, C. Shen, X. Liu, Z. Li, Z. J. Shen, "Transient angle stability of virtual synchronous generators using Lyapunov's direct method," *IEEE Trans. Smart Grid*, vol. 10, no. 4, pp. 4648–4661, Jul. 2019.

[51] M. Kabalan, P. Singh, and D. Niebur, "Nonlinear Lyapunov stability analysis of seven models of a DC/AC droop controlled inverter connected to an infinite bus," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 772–781, Jan. 2019.

[52] Q. Hu, L. Fu, F. Ma, and F. Ji, "Large signal synchronizing instability of PLL-based VSC connected to weak AC grid," *IEEE Trans. Power Syst.*, vol. 34, no. 4, pp. 3220–3229, Jul. 2019.

[53] B. Weise, "Impact of k-factor and active current reduction during fault ride-through of generating units connected via voltage-sourced converters on power system stability," IET Renewable Power Gener., vol. 9, no. 1, pp. 25–36, 2015.

[54] R. Teodorescu and F. Blaabjerg, "Flexible control of small wind turbines with grid failure detection operating in stand-alone and grid-connected mode," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1323–1332, Sep. 2004.

[55] V. Diedrichs, A. Beekmann, and S. Adloff, “Loss of (angle) stability of wind power plants - the underestimated phenomenon in case of very low short circuit ratio,” in Proc. 10th *Int. Wind Integr. Workshop*, Aarhus, Denmark, Jul. 2011, pp. 395–402.

[56] R. E. Betz and M. G. Taul, "Identification of Grid Impedance During Severe Faults," 2019 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 1076-1082.

[57] I. Erlich, F. Shewarega, S. Engelhardt, J. Kretschmann, J. Fortmann, and F. Koch, “Effect of wind turbine output current during faults on grid voltage and the transient stability of wind parks,” in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Jul. 2009, pp. 1–8.

[58] H. Wu and X. Wang, "Design-Oriented Transient Stability Analysis of PLL-Synchronized Voltage-Source Converters," in *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3573-3589, April 2020.

[59] H. A. Hamed, A. F. Abdou, E. H. E. Bayoumi and E. E. EL-Kholy, "A fast recovery technique for grid-connected converters after short dips using a hybrid structure PLL," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3056-3068, April 2018.

[60] D. Yang and X. Wang, “Unified modular state-space modeling of grid-connected voltage-source converters,” *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9700–9715, Sep. 2020.

[61] Y. Liao and X. Wang, “Impedance-based stability analysis for interconnected converter systems with open-loop RHP poles,” *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4388–4397, Apr. 2020.

[62] L. Harnefors, M. Bongiorno, and S. Lundberg, “Input-admittance calculation and shaping for controlled voltage-source converters,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323–3334, Dec. 2007.

[63] K. M. Alawasa, Y. A. I. Mohamed, and W. Xu, “Active mitigation of sub-synchronous interactions between PWM voltage-source converters and power networks,” *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 121–134, Jan. 2014.

[64] J. A. Suul, S. D’Arco, P. Rodríguez, and M. Molinas, “Impedance compensated grid synchronisation for extending the stability range of weak grids with voltage source converters,” *IET Generation Transmiss. Distrib.*, vol. 10, no. 6, pp. 1315–1326, May 2016.

[65] J. Fang, X. Li, H. Li, and Y. Tang, “Stability improvement for three-phase grid-connected converters through impedance reshaping in quadrature-axis,” *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8365–8375, Oct. 2018.

[66] X. Zhang, D. Xia, Z. Fu, G. Wang, and D. Xu, “An improved feedforward control method considering PLL dynamics to improve weak grid stability of grid-connected inverters,” *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5143–5151, Sep. 2018.

[67] P. M. Anderson, “Analysis of Faulted Power Systems”, IEEE Press, 1995.

[68] M. H. J. Bollen, in Understanding Power Quality Problems - Voltage Sags and Interruptions. *IEEE Press Series on Power Engineering,* 2000.

[69] J. F. Conroy, R. Watson, "Low-voltage ride-through of a full converter wind turbine with permanent magnet generator," *IET Renewable Power Generation*, vol.1, no.3, pp.182-189, September 2007.

[70] V. Akhmatov, “Full-load Converter Connected Asynchronous Generators for MW Class Wind Turbines,” *Wind Engineering*, vol.29, no. 4, pp. 341-351, June 2005.

[71] M. Molinas, B. Nass, W. Gullvik, T. Undeland, “Control of Wind Turbines with Induction Generators Interfaced to the Grid with Power Electronics Converters,” *Proc. of the International Power Electronics Conference*, Niigata, Japan, 2005.

[72] C. Abbey, G. Joos, "Effect of low voltage ride through (LVRT) characteristic on voltage stability," *IEEE Power Engineering Society General Meeting,* pp. 1901-1907 Vol. 2, 12-16 June 2005.

[73] N. R. Ullah , T. Thiringer and D. Karlsson "Voltage and transient stability support by wind farms complying with the E.ON Netz grid code", *IEEE Trans. Power Syst.*, vol. 22, pp.1647-1656, 2007.

[74] C. Jauch "Transient and dynamic control of a variable speed wind turbine with synchronous generator", *Wind Energy*, 10, (3), pp. 247–269, 2007.

[75] C. Jauch, P. Sørensen, I. Norhem, and C. Rasmussen, "Simulation of the impact of wind power on the transient fault behaviour of the Nordic power system," *Electric Power Syst. Res.*, no. 77, pp. 135–144, 2007.

[76] A. Mullane, G. Lightbody, R. Yacamini, "Wind-turbine fault ride-through enhancement," *IEEE Transactions on Power Systems*, vol.20, no.4, pp. 1929- 1937, Nov. 2005.

[77] N. A. Cutululis, A. D. Hansen, T. J. Larsen, P. E. Sørensen, F. Iov, "Wind turbines structural loads during fault ride-through operation," *in 2008 European Wind Energy Conference and Exhibition* (pp. 77-80), 2008.

[78] P. Brogan, "The stability of multiple, high power, active front end voltage sourced converters when connected to wind farm collector systems." in Proc. 2010 European Power Electronics Conf. 2010.

[79] Al-Shetwi, A.Q., Sujod, M.Z., 2018. Grid-connected photovoltaic power plants: a review of the recent integration requirements in modern grid codes. *Int. J. Energy Res*. 42, 1849–1865.

[80] Perpinias, I., Papanikolaou, N., Tatakis, E., 2015. Fault ride through concept in low voltage distributed photovoltaic generators for various dispersion and penetration scenarios. *Sustain. Energy Technol. Assess*. 12, 15–25.

[81] B. Badrzadeh and A. Halley, "Challenges associated with assessment and testing of fault ride-through compliance of variable power generation in Australian National Electricity Market," *IEEE Trans. Sustain. Energy*, vol. 6, no. 3, pp. 1160–1168, Jul. 2015.

[82] M. S. El Moursi, W. Xiao, and J. L. Kirtley, "Fault ride through capability for grid interfacing large scale PV power plants," *IET Gener., Transmiss. Distrib.*, vol. 7, no. 9, pp. 1027–1036, 2013.

[83] M. Obi and R. Bass, "Trends and challenges of grid-connected photovoltaic systems—A review," *Renewable Sustain. Energy Rev.*, vol. 58, pp. 1082– 1094, May 2016.

[84] H. M. Hasanien, "An adaptive control strategy for low voltage ride through capability enhancement of grid-connected photovoltaic power plants," *IEEE Trans. Power Syst.*, vol. 31, no. 4, pp. 3230–3237, Jul. 2016.

[85] R. Shah, N. Mithulananthan, R. Bansal, and V. Ramachandaramurthy, "A review of key power system stability challenges for large-scale PV integration," *Renew. Sustain. Energy Rev.*, vol. 41, pp. 1423–1436, 2015.

[86] E. Afshari, B. Farhangi, Y. Yang, and S. Farhangi, "A low-voltage ride-through control strategy for three-phase grid-connected PV systems," in *Proc. IEEE Power Energy Conf. Illinois*, Feb. 2017, pp. 1–6.

[87] NERC Disturbance Report, "1,200 MW Fault Induced Solar Photovoltaic Resource Interruption Disturbance Report", June 2017.

[88] Australian Energy Market Operator (AEMO), Black System South Australia 28 September 2016, Tech. Rep. (March, 2017).

[89] Joint NERC and WECC Staff Report, "900 MW Fault Induced Solar Photovoltaic Resource Interruption Disturbance Report", February 2018.

[90] Australian Energy Market Operator (AEMO), Final report- Queensland and South Australia system separation on 25 August 2018, Tech. Rep. (2019).

[91] Mathworks-Inc., "Matlab/Simulink," [Online], http://www.mathworks.com/, 2019.

[92] Plexim-GmbH, "PLECS Toolbox," [Online], http://www.plexim.com/, 2019.

[93] https://magna-power.com/products/magnadc

[94] Danfoss, "Danfoss 5000 series converter," [Online], http://www.danfoss.com/, 2008.

[95] https://www.regatron.com/product/overview/programmable-bidirectional-ac-power-sources/tc-acs-series/

[96] dSPACE-GmbH, "dSPACE - DS1103 controller board," [Online], http://www.dspace.com/ , 2008.

[97] O. Ellabban, H. Abu-Rub, and F. Blaabjerg, "Renewable energy resources: Current status, future prospects and their enabling technology," *Renewable Sustain. Energy Rev.*, vol. 39, pp. 748–764, Nov. 2014.

[98] I. Sadeghkhani et. al. "Transient monitoring function–based fault detection for inverter-interfaced microgrids", *IEEE Trans. Smart Grid*, vol. PP, no. 99, pp. 1-11, September 2016

[99] Hussain, N.; Nasir, M.; Vasquez, J.C.; Guerrero, J.M. Recent Developments and Challenges on AC Microgrids Fault Detection and Protection Systems–A Review. *Energies* 2020, 13, 2149.

[100] Teimourzadeh, S.; Aminifar, F.; Davarpanah, M.; Guerrero, J.M. Macro, protections for micro grids. Toward a New Protection Paradigm Subsequent to Distributed Energy Resource Integration. *IEEE Ind. Electron. Mag*.2016, 10, 6–18.

[101] K. Iizuka, "The Fast Fourier Transform (FFT)," Springer Series in Optical Sciences, vol. 35, pp. 161–179, 2008.

[102] Kumar, D.S.; Srinivasan, D.; Reindl, T. A fast and scalable protection scheme for distribution networks with distributed generation. *IEEE Trans. Power Deliv.* 2015, 31, 67–75.

[103] Chaitanya, B.K.; Soni, A.K.; Yadav, A. Communication assisted fuzzy based adaptive protective relaying scheme for microgrid. *J. Power Technol*. 2018, 98, 57–69.

[104] Kar, S., Ranjan Samantaray, S. A fuzzy rule base approach for intelligent protection of microgrids. *Electr. Power Compon. Syst.* 2015, 43, 2082–2093.

[105] A. Arunan, J. Ravishankar, and E. Ambikairajah, "Improved disturbance detection and load shedding technique for low voltage islanded microgrids," *IET Generation, Transmission & Distribution, vol. 13,* pp. 2162–2172, Apr. 2019.

[106] J. K. Hwang and Y. Liu, "Identification of Interarea Modes from Ringdown Data by Curve-Fitting in the Frequency Domain," *IEEE Trans. Power Sys.*, vol. 32, pp. 842–851, Mar. 2017.

[107] O. Dharmapandit, R. K. Patnaik, and P. K. Dash, "Detection, classification, and location of faults on grid-connected and islanded AC microgrid," *International Transactions on Electrical Energy Systems*, vol. 27, pp. 1–33, Oct.2017.

[108] D. K. Mohanta, P. Gopakumar, and M. J. B. Reddy, "Transmission line fault detection and localisation methodology using PMU measurements," *IET Gener. Transm. Distrib.*, vol. 9, pp. 1033–1042, Aug. 2015.

[109] S. A. Hosseini, N. Amjady, and M. H. Velayati, "A Fourier Based Wavelet Approach Using Heisenberg's Uncertainty Principle and Shannon's Entropy Criterion to Monitor Power System Small Signal Oscillations," *IEEE Trans. Power Sys.*, vol. 30, pp. 3314–3326, Nov. 2015.

[110] Dash, P. et al.: Power quality analysis using s-transform, *IEEE Trans. Power Deliv.*, 18 (2), 2003, pp. 406-411.

[111] Kar, S.; Samantaray, S.R., "Time-frequency transform-based differential scheme for microgrid protection." *IET Gener. Transm. Distrib.* 2014, 8, 310–320.

[112] C. M. Leavey, M. N. James, J. Summerscales, and R. Sutton, "An introduction to wavelet transforms: A tutorial approach," Insight: Non-Destructive Testing and Condition Monitoring, vol. 45, pp. 344–353, May 2003.

[113] M. S. Manikandan, S. R. Samantaray, and I. Kamwa, "Detection and classification of power quality disturbances using sparse signal decomposition on hybrid dictionaries," *IEEE Trans. Instrument. and Measur.*, vol. 64, pp. 27–38, Jan. 2015.

[114] Abdelgayed, T.S.; Morsi,W.G.; Sidhu, T.S. A new approach for fault classification in microgrids using optimal wavelet functions matching pursuit. *IEEE Trans. Smart Grid* 2017, 9, 4838–4846.

[115] Mishra, D.P.; Samantaray, S.R.; Joos, G. A combined wavelet and data-mining based intelligent protection scheme for microgrid. *IEEE Trans. Smart Grid* 2015, 7, 2295–2304.

[116] Dehghani, M.; Khooban, M.H.; Niknam, T. Fast fault detection and classification based on a combination of wavelet singular entropy theory and fuzzy logic in distribution lines in the presence of distributed generations. *Int. J. Electr. Power Energy Syst.* 2016, 78, 455–462.

[117] Saleh, S.A.; Ahshan, R.; Abu-Khaizaran, M.S.; Alsayid, B.; Rahman, M. Implementing and Testing d-q WPT-Based Digital Protection for Microgrid Systems. *IEEE Trans. Ind. Appl.* 2013, 50, 2173–2185.

[118] Saleh, S. Signature-coordinated digital multirelay protection for microgrid systems, *IEEE Trans. Power Electron.* 2013, 29, 4614–4623.

[119] De Apráiz, M. et al.: A real-time method for time-frequency detection of transient disturbances in voltage supply systems, *Electr. Power Syst. Res.*, 108, 2014, pp. 103-112.

[120] Joorabian, M. et al.: Harmonic estimation in a power system using a novel hybrid Least Squares-Adaline algorithm. *Electr. Power Syst. Res.*, 79 (1), 2009, pp. 107-116.

[121] Abdelsalam, A. A. et al.: Characterization of power quality disturbances using hybrid technique of linear Kalman filter and fuzzy-expert system, *Electr. Power Syst. Res.*, 83 (1), 2012, pp. 41-50.

[122] Dash, P. K., Chilukuri, M. V.: Hybrid S-transform and Kalman filtering approach for detection and measurement of short duration disturbances in power networks, *IEEE Trans.I nstrum. Meas.*, 53 (2), 2004, pp. 588-596.

[123] A. Sahoo, A. Arunan, K. Mahmud, J. Ravishankar, M. Nizami, and M. Hossain, "Teager-Huang based Fault Detection in Inverter-interfaced AC Microgrid," in *2019 IEEE International Conference on Environment and Electrical Engineering* and *2019 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe)*, 2019, pp. 1-5: IEEE.

[124] D. A. Kaiser and J. F. Kaiser, "Estimation of power systems amplitudes, frequencies, and phase characteristics using energy operators," in 2012 *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 930–937.

[125] M. Pineda-Sanchez et al., "Application of the Teager–Kaiser energy operator to the fault diagnosis of induction motors," *IEEE Trans. energy Convers.*, vol. 28, no. 4, pp. 1036–1044, 2013.

[126] J. Kumar and P. Jena, "Fault detection during power swing using Teager-Kaiser energy operator," in 2016 IEEE 6th *International Conference on Power Systems* (ICPS), 2016, pp. 1–6.

[127] I. Kamwa, A. K. Pradhan, and G. Joos, "Robust detection and analysis of power system oscillations using the Teager-Kaiser energy operator," *IEEE Trans. Power Syst.*, vol. 26, no. 1, pp. 323–333, 2011.

[128] H. Xiao, J. Wei, H. Liu, Q. Li, Y. Shi, and T. Zhang, "Identification method for power system low-frequency oscillations based on improved VMD and Teager–Kaiser energy operator," *IET Gener. Transm. Distrib.*, vol. 11, no. 16, pp. 4096–4103, 2017.

[129] K. Thattai, A. Sahoo, and J. Ravishankar, "Teager Energy Operator Based Fault Detection and Classification Technique for Converter Dominated Autonomous AC Microgrid," in IECON 2018-44th *Annual Conference of the IEEE Industrial Electronics Society, 2018*, pp. 294– 299.

[130] A. Khoshnami and I. Sadeghkhani, “Fault detection for PV systems using Teager–Kaiser energy operator,” Electron. Lett., vol. 54, no. 23, pp. 1342–1344, 2018.

[131] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, “Tuning of phase-locked loops for power converters under distorted utility conditions,” *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039–2047, Nov. 2009.

[132] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, and A. Bakhshai, “Problems of startup and phase jumps in PLL systems,” *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1830–1838, Apr. 2012.

[133] R. Zhang, M. Cardinal, P. Szczesny, and M. Dame, “A grid simulator with control of single-phase power converters in D-Q rotating frame,” in Proc. *IEEE Power Electron. Spec. Conf.*, 2002, pp. 1431–1436.

[134] A. Roshan, R. Burgos, A. C. Baisden, F. Wang, and D. Boroyevich, “A D-Q frame controller for a full-bridge single phase inverter used in small distributed power generation systems,” in *Proc. IEEE APEC*, Feb. 2007, pp. 641–647.

[135] M. Saitou and T. Shimizu, “Generalized theory of instantaneous active and reactive powers in single-phase circuits based on Hilbert transform,” in *Proc. 33rd Annu. IEEE PESC*, Jun. 2002, pp. 1419–1424.

[136] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, “A new single-phase PLL structure based on second order generalized integrator,” in *Proc. 37th IEEE PESC*, Jun. 2006, pp. 1–6.

[137] P. Rodriguez, A. Luna, R. Munoz-Aguilar, I. Etxeberria-Otadui, R. Teodorescu, and F. Blaabjerg, “A stationary reference frame grid synchronization system for three-phase grid-connected power converters under adverse grid conditions,” *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 99–112, Jan. 2012.

[138] H. Wu and X. Wang, “An adaptive phase-locked loop for the transient stability enhancement of grid-connected voltage source converters,” in *Proc. IEEE Energy Convers. Congr*. Expo., 2018, pp. 5892–5898.

[139] M. Ciobotaru, “Reliable grid condition detection and control of single phase distributed power generation systems,” Ph.D. dissertation, Dept. Energy Technol., Aalborg Univ., Aalborg, Denmark, 2009.

[140] S. Rajan, S. Wang and R. Inkol, "Efficient Approximations for the Four-Quadrant Arctangent Function," 2006 *Canadian Conference on Electrical and Computer Engineering*, Ottawa, Ont., 2006, pp. 1043-1046.

[141] S. Golestan, J. M. Guerrero, and J. C. Vasquez, “An open-loop grid synchronization approach for single-phase application,” *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5548-5555, Jul. 2018.

[142] Sahoo, A.; Mahmud, K.; Ciobotaru, M.; Ravishankar, J., “Adaptive Grid Synchronization Technique for Single-phase Inverters in AC Microgrid,” *In Proceedings of the 2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 29 September–3 October 2019; pp. 4441–4446.

[143] F. Xiao, L. Dong, L. Li, and X. Liao, “A novel open-loop frequency estimation method for single-phase grid synchronization under distorted conditions,” *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 5, no. 3, pp. 1487–1493, Sep. 2017.

[144] Z.-X. Zou and M. Liserre, ‘‘Modeling phase-locked loop-based synchronization in grid-interfaced converters,’’ *IEEE Trans. Energy Convers.*, vol. 35, no. 1, pp. 394–404, Mar. 2020.

[145] R. Chiumeo, A. Porrino, L. Garbero, L. Tenti, and M. D. Nigris, “The italian power quality monitoring system of the MV network results of the measurements of voltage dips after 3 years campaign,” in *Proc. 20th Int. Conf. Exhib. Elect. Distrib.*, 1, 2009, pp. 1–4.

[146] L. Harnefors, X. Wang, A. Yepes, and F. Blaabjerg, “Passivity-based stability assessment of grid-connected VSCs - an overview,” *IEEE Jour. Emer. Select. Top. Power Electron.*, vol. 4, no. 1, pp. 116-125, Mar. 2016.

[147] S. Golestan, A. Vidal, A. G. Yepes, J. M. Guerrero, J. C. Vasquez, and J. Doval-Gandoy, “A true open-loop synchronization technique,” *IEEE Trans. Ind. Informat.*, vol. 12, no. 3, pp. 1093–1103, Jun. 2016.

[148] J. Wang, Y. L. Song, and A. Monti, “A study of feedforward control on stability of grid-parallel inverter with various grid impedance,” in *Proc. IEEE Power Electron. Distrib. Gener. Syst.*, Jun. 24–27, 2014, pp. 1–8.

[149] J. Xu, S. Xie and T. Tang, "Evaluations of current control in weak grid case for grid-connected LCL-filtered inverter," *IET Power Electron.*, vol. 6, no. 2, pp. 227-234, Feb. 2013.

[150] J. Xiao, H. Lin and T. Hua, "A study of voltage feedforward under weak grid conditions," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, Mar. 17-21, 2019, pp. 3045- 3050.

[151] J. Xu, S. Xie, Q. Qian and B. Zhang, "Adaptive Feedforward Algorithm Without Grid Impedance Estimation for Inverters to Suppress Grid Current Instabilities and Harmonics Due to Grid Impedance and Grid Voltage Distortion," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7574-7586, Sept. 2017.

[152] T. Erika and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron.,* vol. 18, pp. 888-895, 2003.

[153] "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems - Redline," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992) - Redline,* pp. 1-213, 2014.

[154] S. Jayalath and M. Hanif, “Generalized LCL-filter design algorithm forgrid-connected voltage-source inverter,” *IEEE Trans. Ind. Electron.*, vol.64, no. 3, pp. 1905–1915, Mar. 2017.

[155] J. Fang, P. Lin, H. Li, Y. Yang, and Y. Tang, “An improved virtual inertia control for three-phase voltage source converters connected to a weak grid,” *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8660–8670, Sep. 2019.

[156] A. Etxegarai, P. Eguia, E. Torres, A. Iturregi, and V. Valverde, “Review of grid connection requirements for generation assets in weak power grids,” *Renewable and Sustainable Energy Reviews*, vol. 41, pp. 1501–1514, 2015.

[157] S. Grunau and F. W. Fuchs, “Effect of wind-energy power injection into weak grids,” *European Wind Energy Conference and Exhibition* 2012, EWEC 2012, vol. 2, pp. 1150–1156, 01/01 2012.

[158] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.,* vol. 18, pp. 814-822, 2003.

[159] S. Zhou et al., “An improved design of current controller for LCL-type grid-connected converter to reduce negative effect of PLL in weak grid,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 648–663, Jun. 2018.

[160] M. N. I. Sarkar, L. G. Meegahapola, and M. Datta, “Reactive power management in renewable rich power grids: A review of grid-codes, renewable generators, support devices, control strategies and optimization algorithms,” *IEEE Access*, vol. 6, pp. 41458–41489, 2018.

[161] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. Loh, “Proportional-resonant controllers and filters for grid-connected voltage-source converters,” *IEE Proc.–Electric Power Appl.*, vol. 153, no. 5, pp. 750–762, Sep. 2006.

[162] Y. Yang, K. Zhou, and F. Blaabjerg, "Enhancing the frequency adaptability of periodic current controllers with a fixed sampling rate for grid-connected power converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7273–7285, Oct. 2016.

[163] D. Barater, G. Buticchi, A. S. Crinto, G. Franceschini and E. Lorenzani, "Unipolar PWM strategy for transformerless PV grid-connected converters," *IEEE Trans. Energy Convers.*,vol.27, no.4, pp. 835-843, Dec. 2012.

[164] Akagi, H., Watanabe, E.H., Aredes, M.: 'Instantaneous power theory and applications to power conditioning' (John Wiley & Sons, 2007, vol. 31).

[165] Saitou, M., Shimizu, T.: 'Generalized theory of instantaneous active and reactive powers in single-phase circuits based on Hilbert transform'. *Proc. of PESC*, 2002, vol. 3, pp. 1419–1424.

[166] A. Sahoo, J. Ravishankar, M. Ciobotaru, P. Sajeevikumar, "Improved Low Voltage Ride-Through Performance of Single-phase Power Converters using Hybrid Grid Synchronization," in *(IECON) 2020-46th Annual Conference of the IEEE Industrial Electronics Society*, IEEE.